74HC132-Q100; 74HCT132-Q100

Quad 2-input NAND Schmitt trigger

Rev. 3 — 1 December 2015 Product data sheet

1. General description

The 74HC132-Q100; 74HCT132-Q100 is a quad 2-input NAND gate with Schmitt-trigger inputs. Inputs include clamp diodes. This enables the use of current limiting resistors to interface inputs to voltages in excess of V_{CC}. Schmitt trigger inputs transform slowly changing input signals into sharply defined jitter-free output signals.

This product has been qualified to the Automotive Electronics Council (AEC) standard Q100 (Grade 1) and is suitable for use in automotive applications.

2. Features and benefits

- Automotive product qualification in accordance with AEC-Q100 (Grade 1)
  - Specified from –40 °C to +85 °C and from –40 °C to +125 °C
- Complies with JEDEC standard no. 7A
- ESD protection:
  - MIL-STD-883, method 3015 exceeds 2000 V
  - HBM JESD22-A114F exceeds 2000 V
  - MM JESD22-A115-A exceeds 200 V (C = 200 pF, R = 0 Ω)
- Multiple package options

3. Applications

- Wave and pulse shapers
- Astable multivibrators
- Monostable multivibrators

sales@prom-elec.com / ООО ПРОМЭЛЕКТРОНИКА

4. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74HC132D-Q100	–40 °C to +125 °C	SO14	plastic small outline package; 14 leads; body width 3.9 mm	SOT108-1
74HCT132D-Q100				
74HC132PW-Q100	–40 °C to +125 °C	TSSOP14	plastic thin shrink small outline package; 14 leads; body width 4.4 mm	SOT402-1
74HCT132PW-Q100				

5. Functional diagram

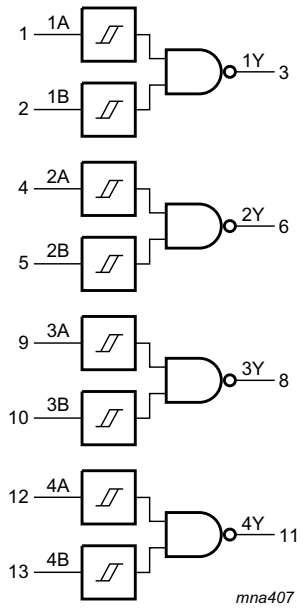


Fig 1. Logic symbol

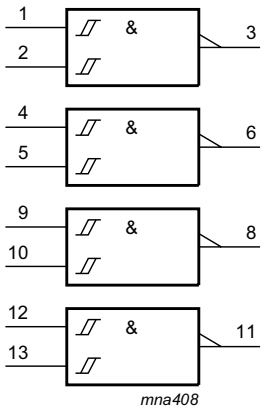


Fig 2. IEC logic symbol

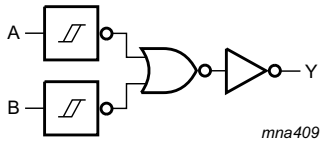


Fig 3. Logic diagram (one Schmitt trigger)

All information provided in this document is subject to legal disclaimers.

© NXP Semiconductors N.V. 2015. All rights reserved.

6. Pinning information

6.1 Pinning

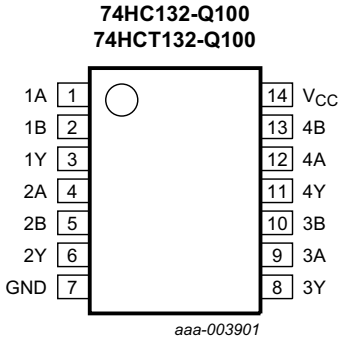


Fig 4. Pin configuration SO14 and TSSOP14

6.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
1A to 4A	1, 4, 9, 12	data input
1B to 4B	2, 5, 10, 13	data input
1Y to 4Y	3, 6, 8, 11	data output
GND	7	ground (0 V)
V_{CC}	14	supply voltage

7. Functional description

Table 3. Function table[1]

Input		Output
nA	**nB**	**nY**
L	L	H
L	H	H
H	L	H
H	H	L

[1] H = HIGH voltage level; L = LOW voltage level; X = don't care.

All information provided in this document is subject to legal disclaimers.

© NXP Semiconductors N.V. 2015. All rights reserved.

8. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{CC}	supply voltage			–0.5	+7	V
I_{IK}	input clamping current	$V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V	[1]	-	±20	mA
I_{OK}	output clamping current	$V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V	[1]	-	±20	mA
I_O	output current	-0.5 V $< V_O < V_{CC} + 0.5$ V		-	±25	mA
I_{CC}	supply current			-	50	mA
I_{GND}	ground current			–50	-	mA
T_{stg}	storage temperature			–65	+150	°C
P_{tot}	total power dissipation		[2]	-	500	mW

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] For SO14 package: P_{tot} derates linearly with 8 mW/K above 70 °C.
For TSSOP14 packages: P_{tot} derates linearly with 5.5 mW/K above 60 °C.

9. Recommended operating conditions

Table 5. Recommended operating conditions

Voltages are referenced to GND (ground = 0 V)

Symbol	Parameter	Conditions	74HC132-Q100			74HCT132-Q100			Unit
			Min	Typ	Max	Min	Typ	Max	
V_{CC}	supply voltage		2.0	5.0	6.0	4.5	5.0	5.5	V
V_I	input voltage		0	-	V_{CC}	0	-	V_{CC}	V
V_O	output voltage		0	-	V_{CC}	0	-	V_{CC}	V
T_{amb}	ambient temperature		–40	+25	+125	–40	+25	+125	°C

All information provided in this document is subject to legal disclaimers.

© NXP Semiconductors N.V. 2015. All rights reserved.

10. Static characteristics

Table 6. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	25 °C			–40 °C to +85 °C		–40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
74HC132-Q100										
V_{OH}	HIGH-level output voltage	$V_I = V_{T+}$ or V_{T-}								
		$I_O = -20\ \mu A$; $V_{CC} = 2.0\ V$	1.9	2.0	-	1.9	-	1.9	-	V
		$I_O = -20\ \mu A$; $V_{CC} = 4.5\ V$	4.4	4.5	-	4.4	-	4.4	-	V
		$I_O = -20\ \mu A$; $V_{CC} = 6.0\ V$	5.9	6.0	-	5.9	-	5.9	-	V
		$I_O = -4.0\ mA$; $V_{CC} = 4.5\ V$	3.98	4.32	-	3.84	-	3.7	-	V
		$I_O = -5.2\ mA$; $V_{CC} = 6.0\ V$	5.48	5.81	-	5.34	-	5.2	-	V
V_{OL}	LOW-level output voltage	$V_I = V_{T+}$ or V_{T-}								
		$I_O = 20\ \mu A$; $V_{CC} = 2.0\ V$	-	0	0.1	-	0.1	-	0.1	V
		$I_O = 20\ \mu A$; $V_{CC} = 4.5\ V$	-	0	0.1	-	0.1	-	0.1	V
		$I_O = 20\ \mu A$; $V_{CC} = 6.0\ V$	-	0	0.1	-	0.1	-	0.1	V
		$I_O = 4.0\ mA$; $V_{CC} = 4.5\ V$	-	0.15	0.26	-	0.33	-	0.4	V
		$I_O = 5.2\ mA$; $V_{CC} = 6.0\ V$	-	0.16	0.26	-	0.33	-	0.4	V
I_I	input leakage current	$V_I = V_{CC}$ or GND; $V_{CC} = 6.0\ V$	-	-	±0.1	-	±1.0	-	±1.0	μA
I_{CC}	supply current	$V_I = V_{CC}$ or GND; $I_O = 0\ A$; $V_{CC} = 6.0\ V$	-	-	2.0	-	20	-	40	μA
C_I	input capacitance		-	3.5	-	-	-	-	-	pF
74HCT132-Q100										
V_{OH}	HIGH-level output voltage	$V_I = V_{T+}$ or V_{T-}; $V_{CC} = 4.5\ V$								
		$I_O = -20\ \mu A$	4.4	4.5	-	4.4	-	4.4	-	V
		$I_O = -4.0\ mA$	3.98	4.32	-	3.84	-	3.7	-	V
V_{OL}	LOW-level output voltage	$V_I = V_{T+}$ or V_{T-}; $V_{CC} = 4.5\ V$								
		$I_O = 20\ \mu A$;	-	0	0.1	-	0.1	-	0.1	V
		$I_O = 4.0\ mA$;	-	0.15	0.26	-	0.33	-	0.4	V
I_I	input leakage current	$V_I = V_{CC}$ or GND; $V_{CC} = 5.5\ V$	-	-	±0.1	-	±1.0	-	±1.0	μA
I_{CC}	supply current	$V_I = V_{CC}$ or GND; $I_O = 0\ A$; $V_{CC} = 5.5\ V$	-	-	2.0	-	20	-	40	μA
ΔI_{CC}	additional supply current	per input pin; $V_I = V_{CC} - 2.1\ V$; $I_O = 0\ A$; other inputs at V_{CC} or GND; $V_{CC} = 4.5\ V$ to $5.5\ V$	-	30	108	-	135	-	147	μA
C_I	input capacitance		-	3.5	-	-	-	-	-	pF

All information provided in this document is subject to legal disclaimers.

© NXP Semiconductors N.V. 2015. All rights reserved.

11. Dynamic characteristics

Table 7. Dynamic characteristics

GND = 0 V; C_L = 50 pF; for load circuit see Figure 6.

Symbol	Parameter	Conditions		25 °C			–40 °C to +125 °C		Unit
				Min	Typ	Max	Max (85 °C)	Max (125 °C)	
74HC132-Q100									
t_{pd}	propagation delay	nA, nB to nY; see Figure 5	[1]						
		V_{CC} = 2.0 V		-	36	125	155	190	ns
		V_{CC} = 4.5 V		-	13	25	31	38	ns
		V_{CC} = 5.0 V; C_L = 15 pF		-	11	-	-	-	ns
		V_{CC} = 6.0 V		-	10	21	26	32	ns
t_t	transition time	see Figure 5	[2]						
		V_{CC} = 2.0 V		-	19	75	95	110	ns
		V_{CC} = 4.5 V		-	7	15	19	22	ns
		V_{CC} = 6.0 V		-	6	13	16	19	ns
C_{PD}	power dissipation capacitance	per package; V_I = GND to V_{CC}	[3]	-	24	-	-	-	pF
74HCT132-Q100									
t_{pd}	propagation delay	nA, nB to nY; see Figure 5	[1]						
		V_{CC} = 4.5 V		-	20	33	41	50	ns
		V_{CC} = 5.0 V; C_L = 15 pF		-	17	-	-	-	ns
t_t	transition time	V_{CC} = 4.5 V; see Figure 5	[2]	-	7	15	19	22	ns
C_{PD}	power dissipation capacitance	per package; V_I = GND to V_{CC} – 1.5 V	[3]	-	20	-	-	-	pF

[1] t_{pd} is the same as t_{PHL} and t_{PLH}.

[2] t_t is the same as t_{THL} and t_{TLH}.

[3] C_{PD} is used to determine the dynamic power dissipation (P_D in μW):

$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:

f_i = input frequency in MHz;

f_o = output frequency in MHz;

C_L = output load capacitance in pF;

V_{CC} = supply voltage in V;

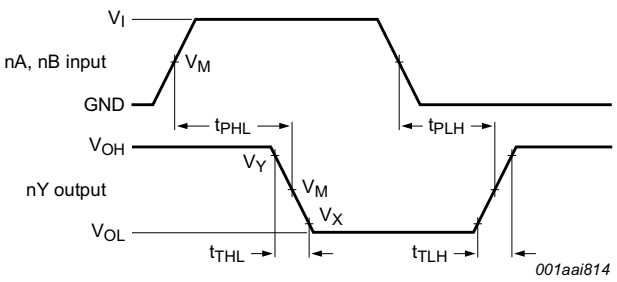
N = number of inputs switching;

$\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.

All information provided in this document is subject to legal disclaimers.

© NXP Semiconductors N.V. 2015. All rights reserved.

12. Waveforms



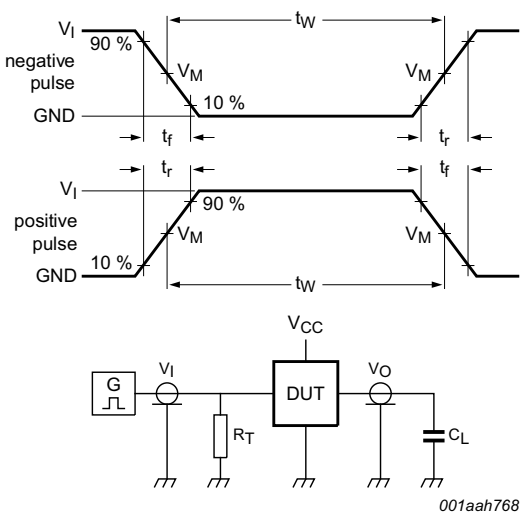
Measurement points are given in Table 8.

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig 5. Input to output propagation delays

Table 8. Measurement points

Type	Input	Output		
	V_M	V_M	V_X	V_Y
74HC132-Q100	$0.5V_{CC}$	$0.5V_{CC}$	$0.1V_{CC}$	$0.9V_{CC}$
74HCT132-Q100	1.3 V	1.3 V	$0.1V_{CC}$	$0.9V_{CC}$



Test data is given in Table 9.

Definitions test circuit:

R_T = termination resistance should be equal to output impedance Z_o of the pulse generator.

C_L = load capacitance including jig and probe capacitance.

Fig 6. Test circuit for measuring switching times

All information provided in this document is subject to legal disclaimers.

© NXP Semiconductors N.V. 2015. All rights reserved.

Table 9. Test data

Type	Input		Load	Test
	V_I	t_r, t_f	C_L	
74HC132-Q100	V_{CC}	6.0 ns	15 pF, 50 pF	t_{PLH}, t_{PHL}
74HCT132-Q100	3.0 V	6.0 ns	15 pF, 50 pF	t_{PLH}, t_{PHL}

13. Transfer characteristics

Table 10. Transfer characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V); see Figure 7 and Figure 8.

Symbol	Parameter	Conditions	T_{amb} = 25 °C			T_{amb} = –40 °C to +85 °C		T_{amb} = –40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
74HC132-Q100										
V_{T+}	positive-going threshold voltage	V_{CC} = 2.0 V	0.7	1.18	1.5	0.7	1.5	0.7	1.5	V
		V_{CC} = 4.5 V	1.7	2.38	3.15	1.7	3.15	1.7	3.15	V
		V_{CC} = 6.0 V	2.1	3.14	4.2	2.1	4.2	2.1	4.2	V
V_{T-}	negative-going threshold voltage	V_{CC} = 2.0 V	0.3	0.63	1.0	0.3	1.0	0.3	1.0	V
		V_{CC} = 4.5 V	0.9	1.67	2.2	0.9	2.2	0.9	2.2	V
		V_{CC} = 6.0 V	1.2	2.26	3.0	1.2	3.0	1.2	3.0	V
V_H	hysteresis voltage	V_{CC} = 2.0 V	0.2	0.55	1.0	0.2	1.0	0.2	1.0	V
		V_{CC} = 4.5 V	0.4	0.71	1.4	0.4	1.4	0.4	1.4	V
		V_{CC} = 6.0 V	0.6	0.88	1.6	0.6	1.6	0.6	1.6	V
74HCT132-Q100										
V_{T+}	positive-going threshold voltage	V_{CC} = 4.5 V	1.2	1.41	1.9	1.2	1.9	1.2	1.9	V
		V_{CC} = 5.5 V	1.4	1.59	2.1	1.4	2.1	1.4	2.1	V
V_{T-}	negative-going threshold voltage	V_{CC} = 4.5 V	0.5	0.85	1.2	0.5	1.2	0.5	1.2	V
		V_{CC} = 5.5 V	0.6	0.99	1.4	0.6	1.4	0.6	1.4	V
V_H	hysteresis voltage	V_{CC} = 4.5 V	0.4	0.56	-	0.4	-	0.4	-	V
		V_{CC} = 5.5 V	0.4	0.60	-	0.4	-	0.4	-	V

14. Transfer characteristics waveforms

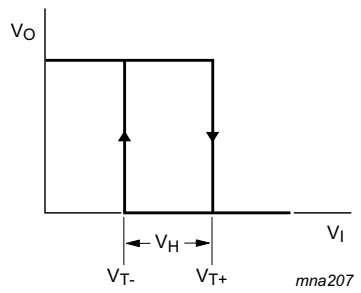


Fig 7. Transfer characteristics

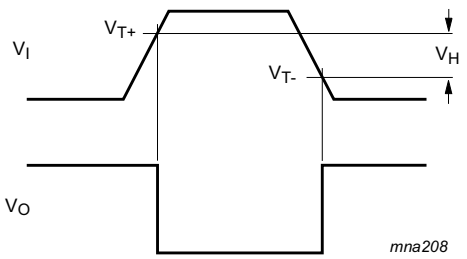
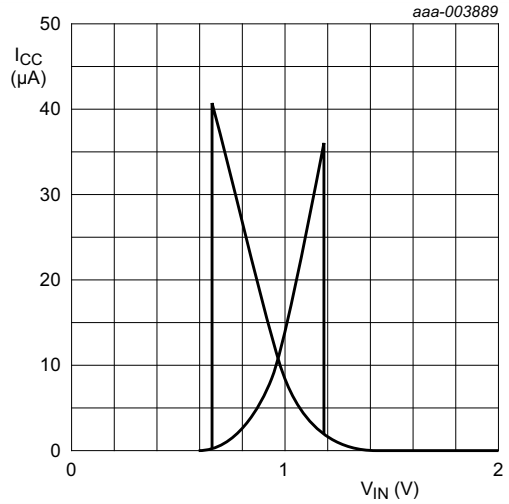


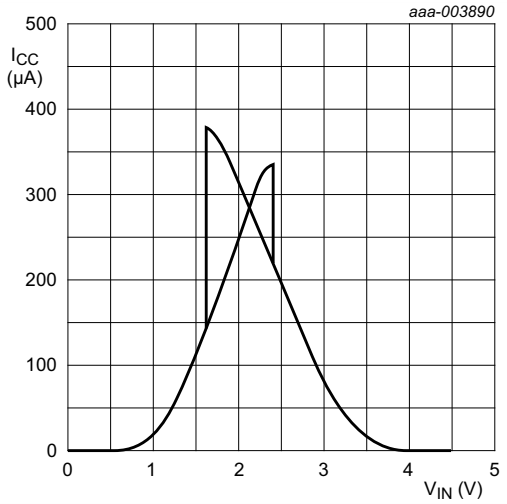
Fig 8. Transfer characteristics definitions

All information provided in this document is subject to legal disclaimers.

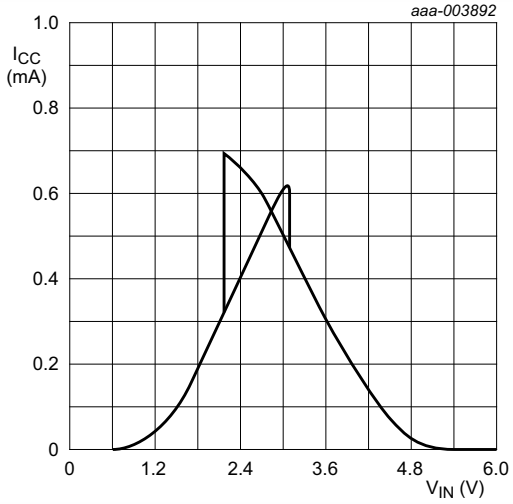
© NXP Semiconductors N.V. 2015. All rights reserved.



a. V_{CC} = 2.0 V



b. V_{CC} = 4.5 V

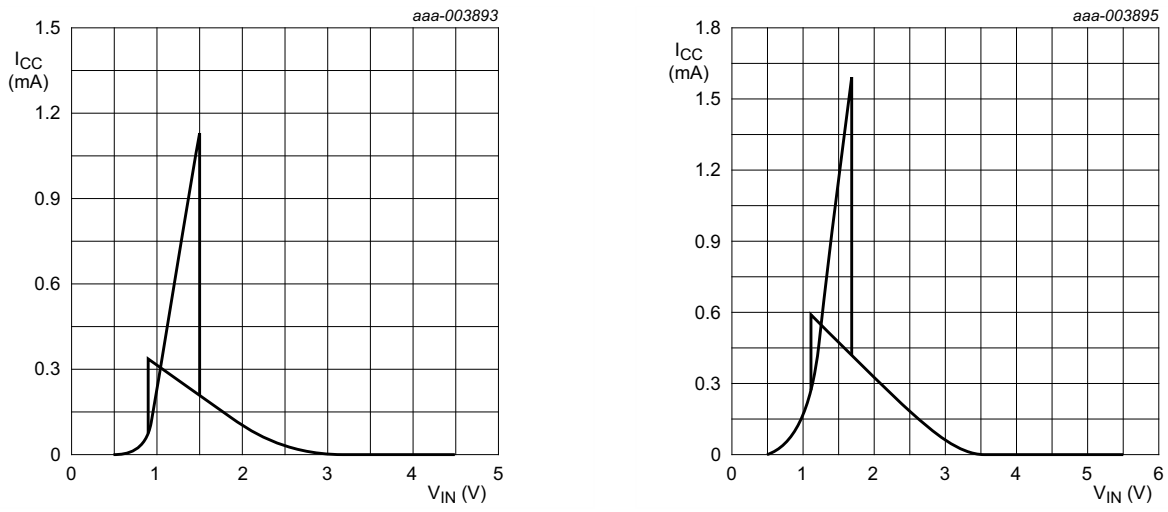


c. V_{CC} = 6.0 V

Fig 9. Typical 74HC132-Q100 transfer characteristics

All information provided in this document is subject to legal disclaimers.

© NXP Semiconductors N.V. 2015. All rights reserved.



a. V_{CC} = 4.5 V

b. V_{CC} = 5.5 V

Fig 10. Typical 74HCT132-Q100 transfer characteristics

15. Application information

The slow input rise and fall times cause additional power dissipation, this can be calculated using the following formula:

$P_{add} = f_i \times (t_r \times \Delta I_{CC(AV)} + t_f \times \Delta I_{CC(AV)}) \times V_{CC}$ where:

P_{add} = additional power dissipation (μW);

f_i = input frequency (MHz);

t_r = rise time (ns); 10 % to 90 %;

t_f = fall time (ns); 90 % to 10 %;

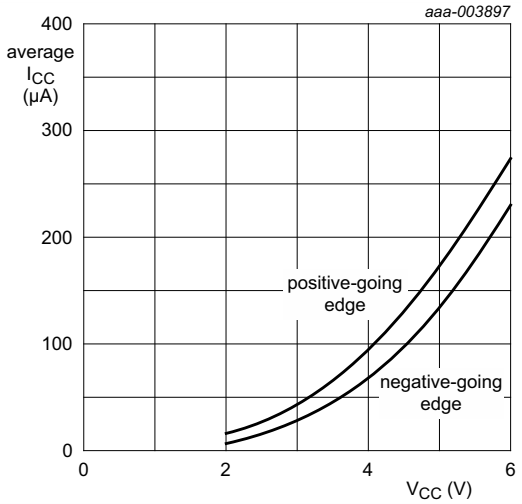
$\Delta I_{CC(AV)}$ = average additional supply current (μA).

Average $\Delta I_{CC(AV)}$ differs with positive or negative input transitions, as shown in Figure 11 and Figure 12.

An example of a relaxation circuit using the 74HC132-Q100; 74HCT132-Q100 is shown in Figure 13.

All information provided in this document is subject to legal disclaimers.

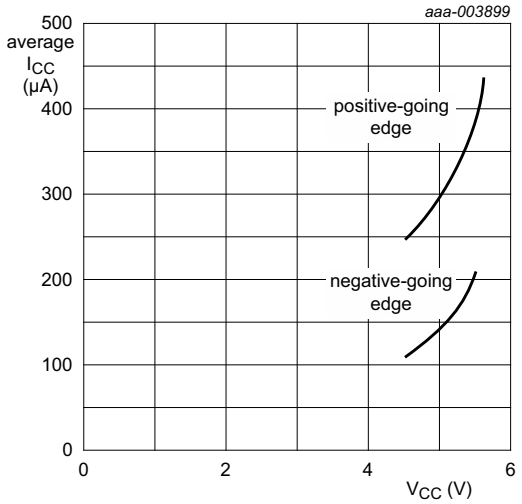
© NXP Semiconductors N.V. 2015. All rights reserved.



(1) Positive-going edge.

(2) Negative-going edge.

Fig 11. Average additional supply current as a function of V_{CC} for 74HC132-Q100; linear change of VI between 0.1VCC to 0.9VCC.



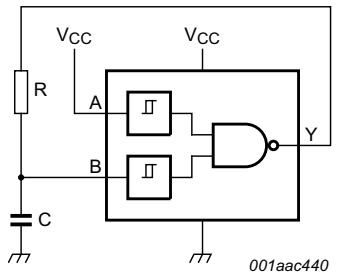
(1) Positive-going edge.

(2) Negative-going edge.

Fig 12. Average additional supply current as a function of V_{CC} for 74HCT132-Q100; linear change of VI between 0.1VCC to 0.9VCC.

All information provided in this document is subject to legal disclaimers.

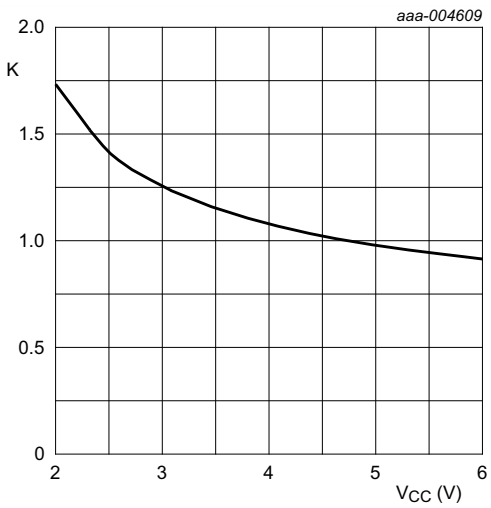
© NXP Semiconductors N.V. 2015. All rights reserved.



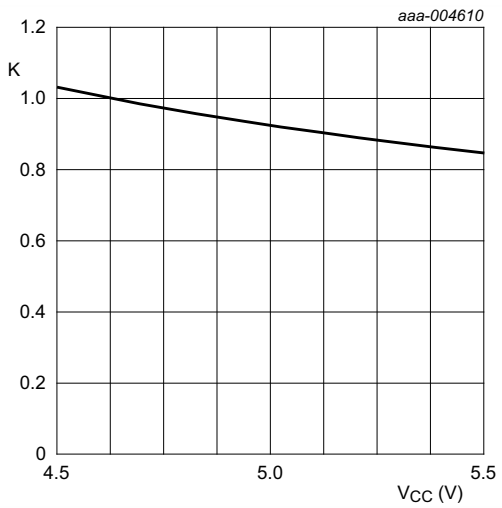
For 74HC132-Q100 and 74HCT132-Q100: $f = \frac{1}{T} \approx \frac{1}{K \times RC}$

For K-factor see Figure 14

Fig 13. Relaxation oscillator



K-factor for 74HC132-Q100



K-factor for 74HCT132-Q100

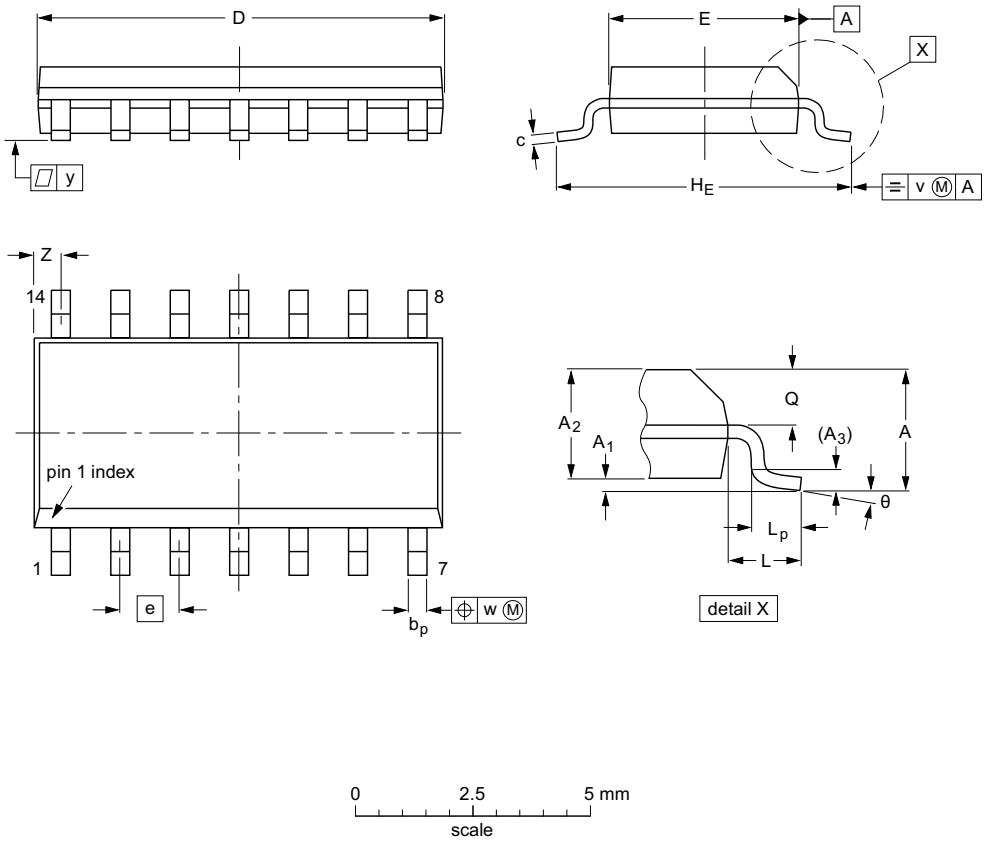
Fig 14. Typical K-factor for relaxation oscillator

All information provided in this document is subject to legal disclaimers.

© NXP Semiconductors N.V. 2015. All rights reserved.

16. Package outline

SO14: plastic small outline package; 14 leads; body width 3.9 mm **SOT108-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D(1)	E(1)	e	H_E	L	L_p	Q	v	w	y	Z(1)	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	8.75 8.55	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.35 0.34	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	

Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

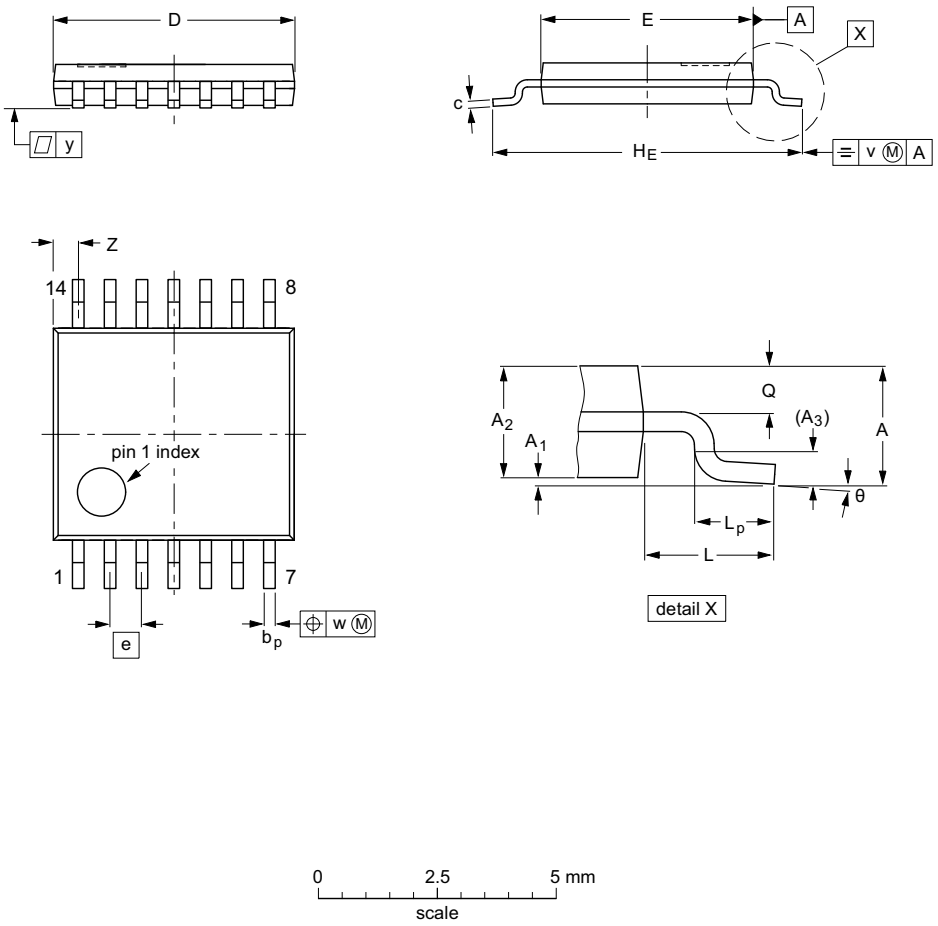
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT108-1	076E06	MS-012				~~99-12-27~~ 03-02-19

Fig 15. Package outline SOT108-1 (SO14)

All information provided in this document is subject to legal disclaimers.

© NXP Semiconductors N.V. 2015. All rights reserved.

TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm **SOT402-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (2)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.72 0.38	8° 0°

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT402-1		MO-153				~~99-12-27~~ 03-02-18

Fig 16. Package outline SOT402-1 (TSSOP14)

All information provided in this document is subject to legal disclaimers.

© NXP Semiconductors N.V. 2015. All rights reserved.

17. Abbreviations

Table 11. Abbreviations

Acronym	Description
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model
MIL	Military

18. Revision history

Table 12. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74HC_HCT132_Q100 v.3	20151201	Product data sheet	-	74HC_HCT132_Q100 v.2
Modifications:	• General description changed.			
74HC_HCT132_Q100 v.2	20120813	Product data sheet	-	74HC_HCT132_Q100 v.1
Modifications:	• Figure 14 added (typical K-factor for relaxation oscillator).			
74HC_HCT132_Q100 v.1	20120712	Product data sheet	-	-

All information provided in this document is subject to legal disclaimers.

© NXP Semiconductors N.V. 2015. All rights reserved.

19. Legal information

19.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

19.2 Definitions

Draft — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

Short data sheet — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

Product specification — The information and data provided in a Product data sheet shall define the specification of the product as agreed between NXP Semiconductors and its customer, unless NXP Semiconductors and customer have explicitly agreed otherwise in writing. In no event however, shall an agreement be valid in which the NXP Semiconductors product is deemed to offer functions and qualities beyond those described in the Product data sheet.

19.3 Disclaimers

Limited warranty and liability — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. NXP Semiconductors takes no responsibility for the content in this document if provided by an information source outside of NXP Semiconductors.

In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory.

Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the *Terms and conditions of commercial sale* of NXP Semiconductors.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use in automotive applications — This NXP Semiconductors product has been qualified for use in automotive applications. Unless otherwise agreed in writing, the product is not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors and its suppliers accept no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Customers are responsible for the design and operation of their applications and products using NXP Semiconductors products, and NXP Semiconductors accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the NXP Semiconductors product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products.

NXP Semiconductors does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using NXP Semiconductors products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). NXP does not accept any liability in this respect.

Limiting values — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) will cause permanent damage to the device. Limiting values are stress ratings only and (proper) operation of the device at these or any other conditions above those given in the Recommended operating conditions section (if present) or the Characteristics sections of this document is not warranted. Constant or repeated exposure to limiting values will permanently and irreversibly affect the quality and reliability of the device.

Terms and conditions of commercial sale — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at http://www.nxp.com/profile/terms, unless otherwise agreed in a valid written individual agreement. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. NXP Semiconductors hereby expressly objects to applying the customer's general terms and conditions with regard to the purchase of NXP Semiconductors products by customer.

All information provided in this document is subject to legal disclaimers.

© NXP Semiconductors N.V. 2015. All rights reserved.

No offer to sell or license — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

Export control — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from competent authorities.

Translations — A non-English (translated) version of a document is for reference only. The English version shall prevail in case of any discrepancy between the translated and English versions.

19.4 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

20. Contact information

For more information, please visit: **http://www.nxp.com**

For sales office addresses, please send an email to: **salesaddresses@nxp.com**

All information provided in this document is subject to legal disclaimers.

© NXP Semiconductors N.V. 2015. All rights reserved.

21. Contents

1 General description 1
2 Features and benefits 1
3 Applications 1
4 Ordering information 2
5 Functional diagram 2
6 Pinning information 3
6.1 Pinning 3
6.2 Pin description 3
7 Functional description 3
8 Limiting values 4
9 Recommended operating conditions 4
10 Static characteristics 5
11 Dynamic characteristics 6
12 Waveforms 7
13 Transfer characteristics 8
14 Transfer characteristics waveforms 8
15 Application information 10
16 Package outline 13
17 Abbreviations 15
18 Revision history 15
19 Legal information 16
19.1 Data sheet status 16
19.2 Definitions 16
19.3 Disclaimers 16
19.4 Trademarks 17
20 Contact information 17
21 Contents 18

Please be aware that important notices concerning this document and the product(s) described herein, have been included in section 'Legal information'.

© NXP Semiconductors N.V. 2015. All rights reserved.

For more information, please visit: http://www.nxp.com
For sales office addresses, please send an email to: salesaddresses@nxp.com

Date of release: 1 December 2015
Document identifier: 74HC_HCT132_Q100