A5970D

Up to 1 A step-down switching regulator for automotive applications

Datasheet - production data

SO-8

Features

- Qualified following the AEC-Q100 requirements (see PPAP for more details)
- 1 A DC output current
- Operating input voltage from 4 V to 36 V
- 3.3 V / (± 2%) reference voltage
- Output voltage adjustable from 1.235 V to V_{IN}
- Low dropout operation: 100% duty cycle
- 250 kHz Internally fixed frequency
- Voltage feed-forward
- Zero load current operation
- Internal current limiting
- Inhibit for zero current consumption
- Synchronization
- Protection against feedback disconnection
- Thermal shutdown

Applications

- Dedicated to automotive applications

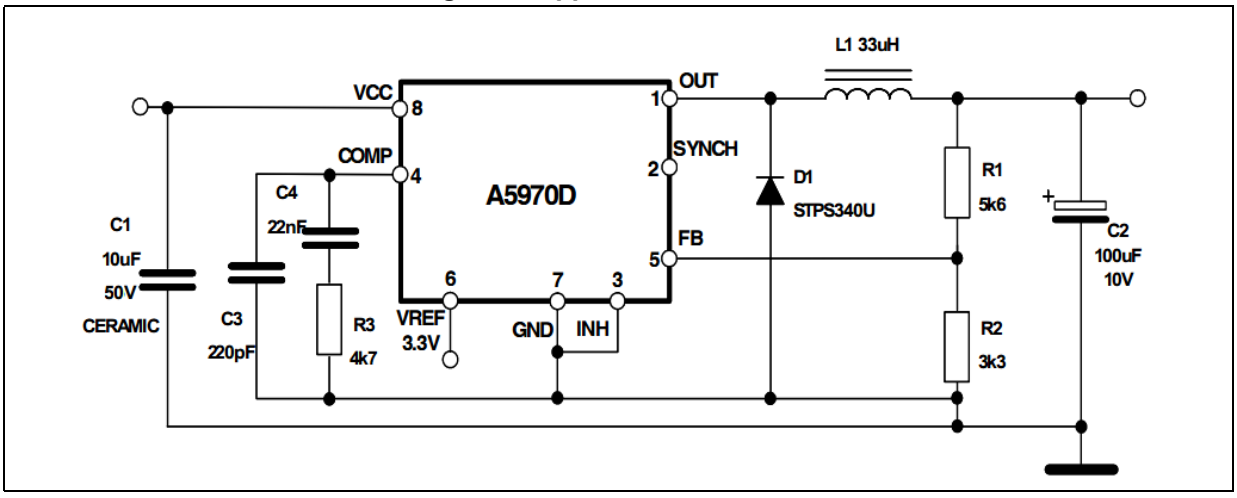
Description

The A5970D is a step-down monolithic power switching regulator with a minimum switch current limit of 1.35 A so it is able to deliver up to 1 A DC current to the load depending on the application conditions. The output voltage can be set from 1.235 V to V_{IN}.

The device uses an internal p-channel DMOS transistor (with a typical $R_{DS(on)}$ of 250 mΩ) as switching element to minimize the size of the external components.

An internal oscillator fixes the switching frequency at 250 kHz. Having a minimum input voltage of 4 V only it fits the automotive applications requiring the device operation even in cold crank conditions. Pulse by pulse current limit with the internal frequency modulation offers an effective constant current short-circuit protection.

Figure 1. Application schematic



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Contents

1 Pin settings 4

1.1 Pin connection 4

1.2 Pin description 4

2 Electrical data 5

2.1 Maximum ratings 5

2.2 Thermal data 5

3 Electrical characteristics 6

4 Datasheet parameters over the temperature range 8

5 Functional description 9

5.1 Power supply and voltage reference 9

5.2 Voltages monitor 10

5.3 Oscillator and synchronization 10

5.4 Current protection 11

5.5 Error amplifier 12

5.6 PWM comparator and power stage 13

5.7 Inhibit function 14

5.8 Thermal shutdown 14

6 Additional features and protection 15

6.1 Feedback disconnection 15

6.2 Output overvoltage protection 15

6.3 Zero load 15

7 Closing the loop 16

7.1 Error amplifier and compensation network 17

7.2 LC filter 18

7.3 PWM comparator 19

8 Application information 21
8.1 Component selection 21
8.2 Layout considerations 24
8.3 Thermal considerations 24
8.4 Short-circuit protection 26
8.5 Application circuit 29
8.6 Positive buck-boost regulator 31
8.7 Negative buck-boost regulator 33
8.8 Synchronization example 34
8.9 Compensation network with MLCC at the output 34
8.10 External SOFT_START network 35

9 Typical characteristics 36

10 Package information 38
10.1 SO-8 package information 38

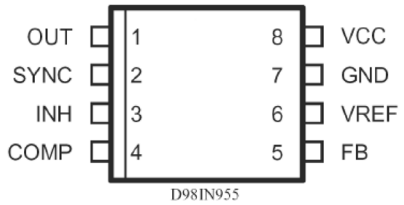
11 Order codes 40

12 Revision history 40

1 Pin settings

1.1 Pin connection

Figure 2. Pin connection (top view)



1.2 Pin description

Table 1. Pin description

No.	Pin	Description
1	OUT	Regulator output.
2	SYNCH	Master/slave synchronization.
3	INH	A logical signal (active high) disables the device. If INH not used, the pin must be grounded. When it is open, an internal pull-up disables the device.
4	COMP	E/A output for frequency compensation.
5	FB	Feedback input. Connecting directly to this pin results in an output voltage of 1.23 V. An external resistive divider is required for higher output voltages.
6	VREF	3.3 V V_{REF}. No cap is requested for stability.
7	GND	Ground.
8	VCC	Unregulated DC input voltage.

2 Electrical data

2.1 Maximum ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_8	Input voltage	40	V
V_1	OUT pin DC voltage OUT pin peak voltage at Δt = 0.1 μs	-1 to 40 -5 to 40	V V
I_1	Maximum output current	Int. limit.	
V_4, V_5	Analog pins	4	V
V_3	INH	-0.3 to V_{CC}	V
V_2	SYNCH	-0.3 to 4	V
P_{TOT}	Power dissipation at $T_A \leq 70$ °C	0.6	W
T_J	Operating junction temperature range	-40 to 150	°C
T_{STG}	Storage temperature range	-55 to 150	°C

2.2 Thermal data

Table 3. Thermal data

Symbol	Parameter	Value	Unit
R_{thJA}	Maximum thermal resistance junction ambient	120(1)	°C/W

1. Package mounted on evaluation board.

3 Electrical characteristics

T_J = -40 °C to 125 °C, V_{CC} = 12 V, unless otherwise specified.

Table 4. Electrical characteristics

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
V_{CC}	Operating input voltage range		4		36	V
$R_{DS(on)}$	MOSFET on resistance			0.250	0.5	Ω
I_L	Maximum limiting current(1)	V_{CC} = 5 V	1.35	1.87	2.25	A
		V_{CC} = 5 V, T_J = 25 °C	1.5	1.87	2.25	
f_{SW}	Switching frequency		212	250	280	kHz
	Duty cycle		0		100	%
Dynamic characteristics (see test circuit).						
V_5	Voltage feedback	4.4 V < V_{CC} < 36 V	1.198	1.235	1.272	V
η	Efficiency	V_0 = 5 V, V_{CC} = 12 V		90		%
DC characteristics						
I_{qop}	Total operating quiescent current			3	5	mA
I_q	Quiescent current	Duty cycle = 0; V_{FB} = 1.5 V			2.5	mA
$I_{qst\text{-}by}$	Total standby quiescent current	V_{inh} > 2.2 V		50	100	µA
		V_{CC} = 36 V; V_{inh} > 2.2 V		80	150	µA
Inhibit						
	INH threshold voltage	Device ON			0.8	V
		Device OFF	2.2			V
Error amplifier						
V_{OH}	High level output voltage	V_{FB} = 1 V	3.5			V
V_{OL}	Low level output voltage	V_{FB} = 1.5 V			0.4	V
$I_{o\ source}$	Source output current	V_{COMP} = 1.9 V; V_{FB} = 1 V	190	300		µA
$I_{o\ sink}$	Sink output current	V_{COMP} = 1.9 V; V_{FB}=1.5 V	1	1.5		mA
I_b	Source bias current			2.5	4	µA
	DC open loop gain	R_L = ∞	50	65		dB
gm	Transconductance	I_{COMP} = -0.1 mA to 0.1 mA; V_{COMP} = 1.9 V		2.3		mS
Synch function						
	High input voltage	V_{CC} = 4.4 to 36 V	2.5		V_{REF}	V
	Low input voltage	V_{CC} = 4.4 to 36 V			0.74	V
	Slave synch current	V_{synch} = 0.74 V(2) V_{synch} = 2.33 V	0.11 0.21		0.25 0.45	mA

Table 4. Electrical characteristics (continued)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
	Master output amplitude	I_{source} = 3 mA	2.75	3		V
	Output pulse width	no load, V_{synch} = 1.65 V	0.20	0.35		µs
Reference section						
	Reference voltage	I_{REF} = 0 to 5 mA V_{CC} = 4.4 V to 36 V	3.2	3.3	3.399	V
	Line regulation	I_{REF} = 0 mA V_{CC} = 4.4 V to 36 V		5	10	mV
	Load regulation	I_{REF} = 0 mA		8	15	mV
	Short-circuit current		5	18	35	mA

1. With T_J = 85 °C, I_{lim_min} = 1.5 A, assured by design, characterization and statistical correlation.
2. Guaranteed by design.

4 Datasheet parameters over the temperature range

The 100% of the population in the production flow is tested at three different ambient temperatures (-40 °C, +25 °C, +125 °C) to guarantee the datasheet parameters inside the junction temperature range (-40 °C, +125 °C).

The device operation is so guaranteed when the junction temperature is inside the (-40 °C, +150 °C) temperature range. The designer can estimate the silicon temperature increase respect to the ambient temperature evaluating the internal power losses generated during the device operation (please refer to *Section 2.2*).

However the embedded thermal protection disables the switching activity to protect the device in case the junction temperature reaches the T_{SHTDWN} (+150 °C ± 10 °C) temperature.

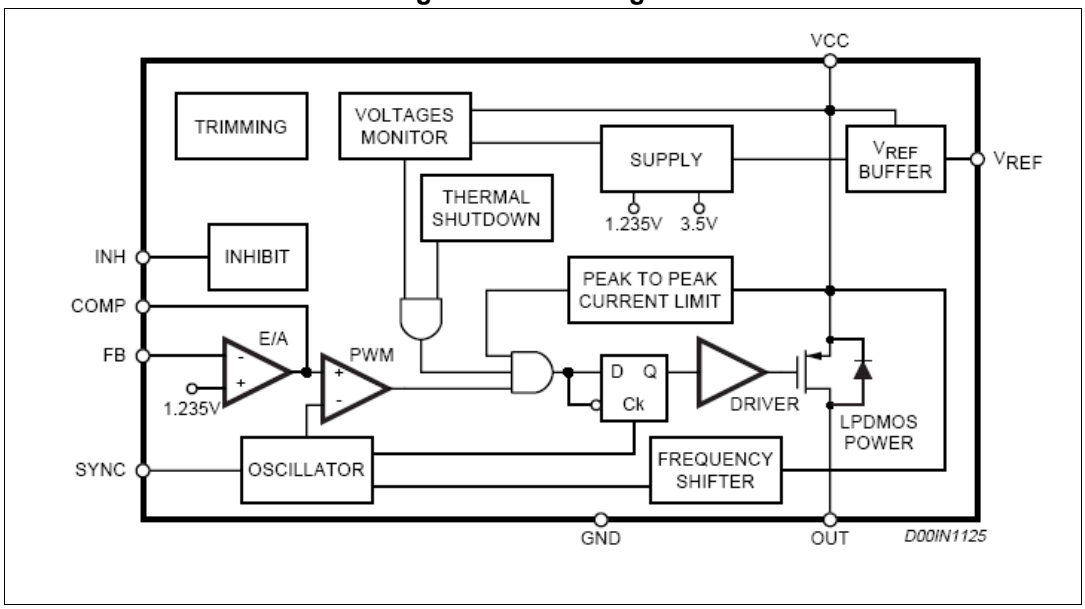
All the datasheet parameters can be guaranteed to a maximum junction temperature of +125 °C to avoid triggering the thermal shutdown protection during the testing phase because of self-heating.

5 Functional description

The main internal blocks are shown in the device block diagram in *Figure 3*. They are:

- A voltage regulator supplying the internal circuitry. From this regulator, a 3.3 V reference voltage is externally available.
- A voltage monitor circuit which checks the input and the internal voltages.
- A fully integrated sawtooth oscillator with a frequency of 250 kHz ± 15%, including also the voltage feed forward function and an input/output synchronization pin.
- Two embedded current limitation circuits which control the current that flows through the power switch. The pulse-by-pulse current limit forces the power switch OFF cycle by cycle if the current reaches an internal threshold, while the frequency shifter reduces the switching frequency in order to significantly reduce the duty cycle.
- A transconductance error amplifier.
- A pulse width modulator (PWM) comparator and the relative logic circuitry necessary to drive the internal power.
- A high side driver for the internal P-MOS switch.
- An inhibit block for standby operation.
- A circuit to implement the thermal protection function.

Figure 3. Block diagram



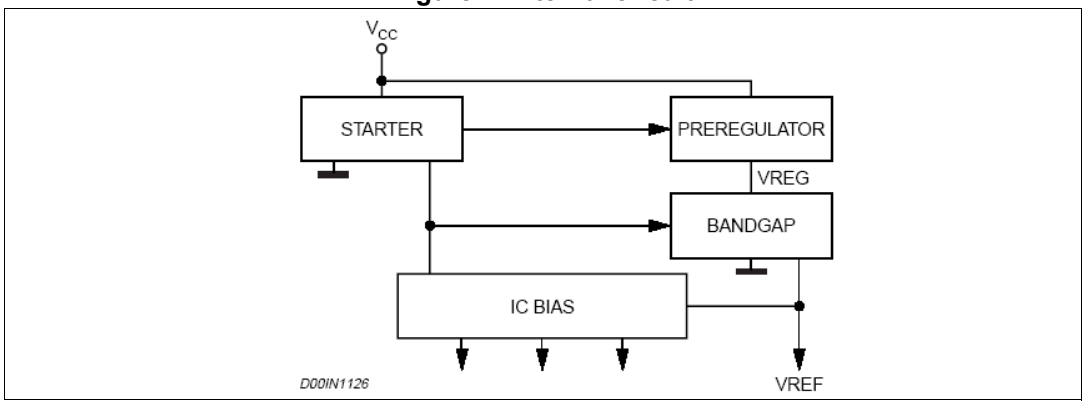
5.1 Power supply and voltage reference

The internal regulator circuit (shown in *Figure 4*) consists of a start-up circuit, an internal voltage pre-regulator, the bandgap voltage reference and the bias block that provides current to all the blocks. The starter supplies the start-up currents to the entire device when the input voltage goes high and the device is enabled (inhibit pin connected to ground). The pre-regulator block supplies the bandgap cell with a pre-regulated voltage V_{REG} that has a very low supply voltage noise sensitivity.

5.2 Voltages monitor

An internal block continuously senses the V_{cc}, V_{ref} and V_{bg}. If the voltages go higher than their thresholds, the regulator begins operating. There is also a hysteresis on the V_{CC} (UVLO).

Figure 4. Internal circuit



5.3 Oscillator and synchronization

Figure 5 shows the block diagram of the oscillator circuit.

The clock generator provides the switching frequency of the device, which is internally fixed at 250 kHz. The frequency shifter block acts to reduce the switching frequency in case of strong overcurrent or short-circuit . The clock signal is then used in the internal logic circuitry and is the input of the ramp generator and synchronizer blocks.

The ramp generator circuit provides the sawtooth signal, used for PWM control and the internal voltage feed-forward, while the synchronizer circuit generates the synchronization signal. The device also has a synchronization pin which can work both as master and slave.

Beating frequency noise is an issue when more than one voltage rail is on the same board. A simple way to avoid this issue is to operate all the regulators at the same switching frequency.

The synchronization feature of a set of the A5970D is simply get connecting together their SYNCH pin. The device with highest switching frequency will be the MASTER and it provides the synchronization signal to the others. Therefore the SYNCH is a I/O pin to deliver or recognize a frequency signal. The synchronization circuitry is powered by the internal reference (V_{REF}) so a small filtering capacitor ($\geq$ 100 nF) connected between the V_{REF} pin and the signal ground of the master device is suggested for its proper operation. However when a set of synchronized devices populates a board it is not possible to know in advance the one working as master, so the filtering capacitor have to be designed for whole set of devices.

When one or more devices are synchronized to an external signal, its amplitude have to be in comply with specifications given in the *Table 4 on page 6*. The frequency of the synchronization signal must be, at a minimum, higher than the maximum guaranteed natural switching frequency of the device (275 kHz, see *Table 4*) while the duty cycle of the synchronization signal can vary from approximately 10% to 90%. The small capacitor under the V_{REF} pin is required for this operation.

Figure 5. Oscillator circuit block diagram

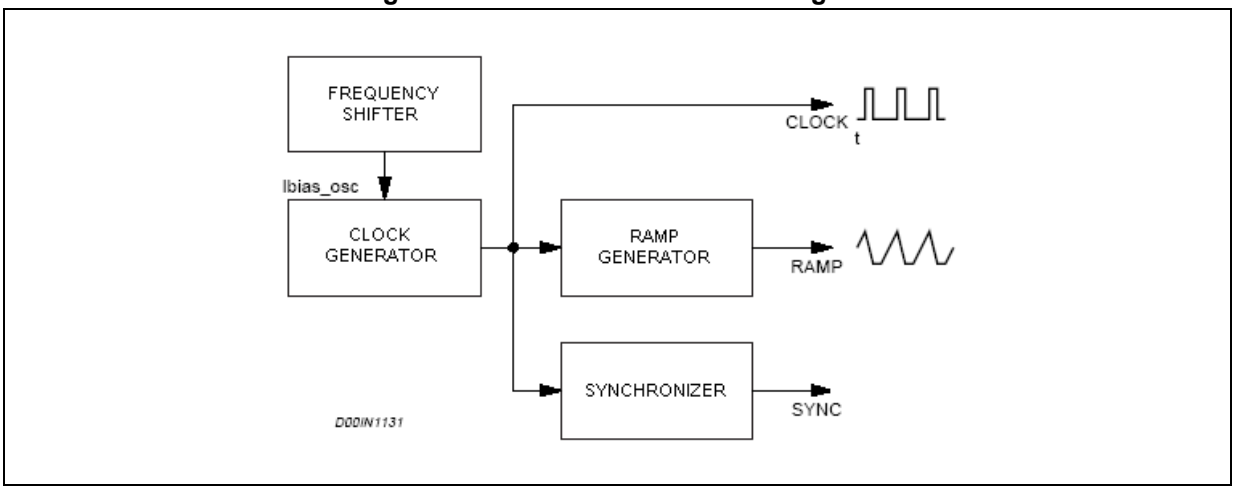
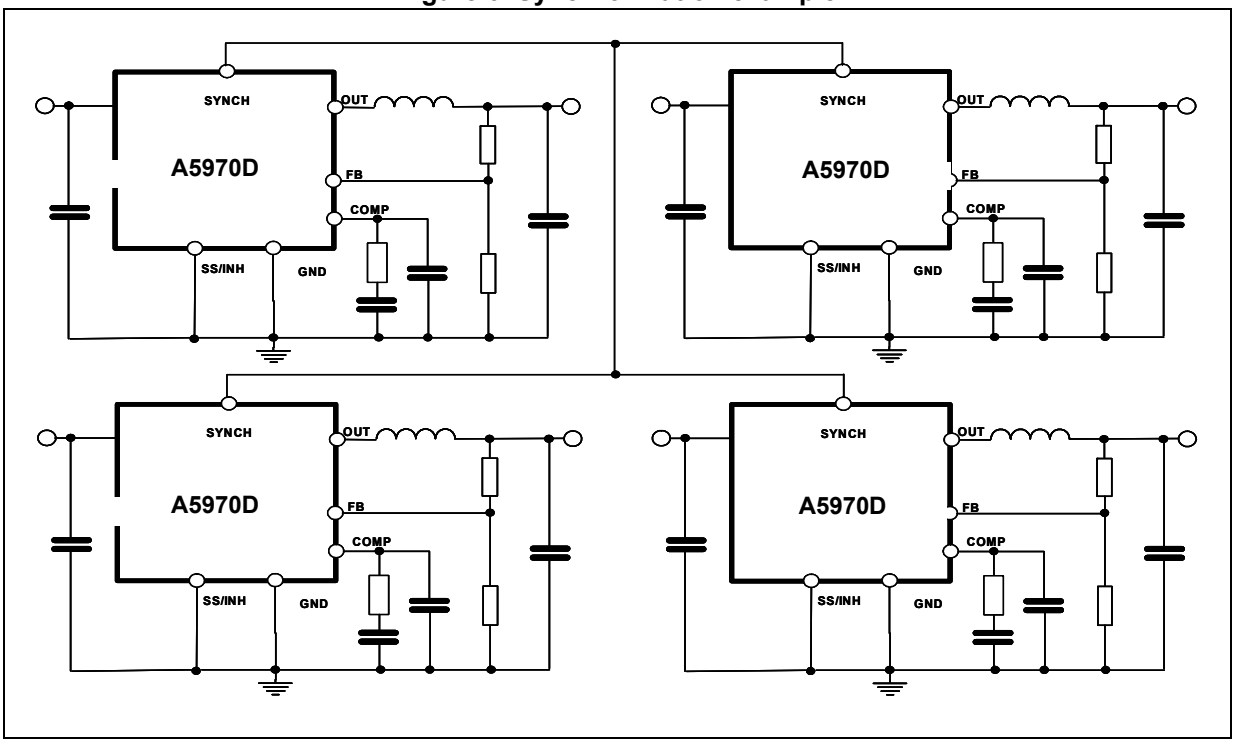


Figure 6. Synchronization example



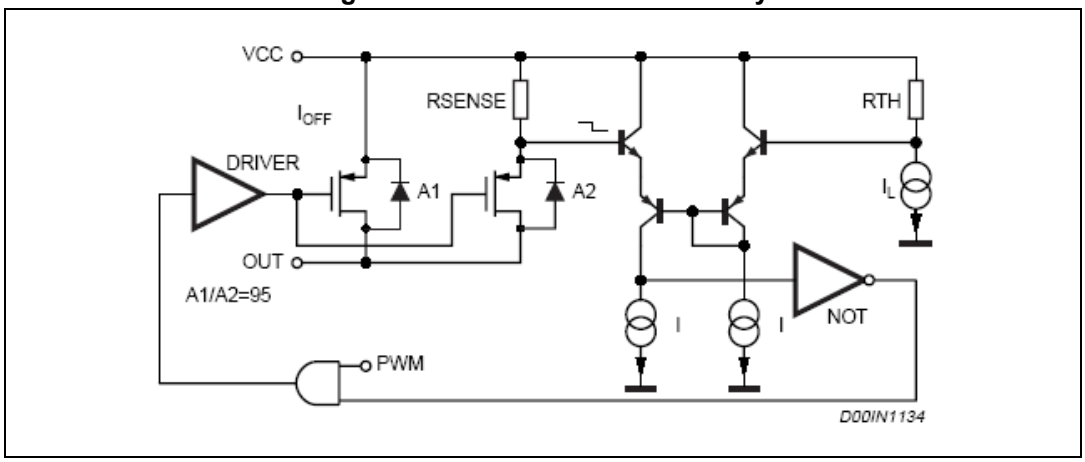
5.4 Current protection

The A5970D device features two types of current limit protection: pulse-by-pulse and frequency foldback.

The schematic of the current limitation circuitry for the pulse-by-pulse protection is shown in *Figure 7*. The output power PDMOS transistor is split into two parallel PDMOS transistors. The smallest one includes a resistor in series, R_{SENSE}. The current is sensed through R_{SENSE} and if it reaches the threshold, the mirror becomes unbalanced and the PDMOS is switched off until the next falling edge of the internal clock pulse. Due to this reduction of the

ON time, the output voltage decreases. Since the minimum switch ON time necessary to sense the current in order to avoid a false overcurrent signal is too short to obtain a sufficiently low duty cycle at 250 kHz (see *Section 8.4 on page 26*), the output current in strong overcurrent or short-circuit conditions could be not properly limited. For this reason the switching frequency is also reduced, thus keeping the inductor current under its maximum threshold. The frequency shifter (*Figure 5*) functions based on the feedback voltage. As the feedback voltage decreases (due to the reduced duty cycle), the switching frequency decreases also.

Figure 7. Current limitation circuitry



5.5 Error amplifier

The voltage error amplifier is the core of the loop regulation. It is a transconductance operational amplifier whose non inverting input is connected to the internal voltage reference (1.235 V), while the inverting input (FB) is connected to the external divider or directly to the output voltage. The output (COMP) is connected to the external compensation network. The uncompensated error amplifier has the following characteristics:

Table 5. Uncompensated error amplifier characteristics

Description	Values
Transconductance	2300 µS
Low frequency gain	65 dB
Minimum sink/source voltage	1500 µA/300 µA
Output voltage swing	0.4 V/3.65 V
Input bias current	2.5 µA

The error amplifier output is compared to the oscillator sawtooth to perform PWM control.

5.6 PWM comparator and power stage

This block compares the oscillator sawtooth and the error amplifier output signals to generate the PWM signal for the driving stage.

The power stage is a highly critical block, as it functions to guarantee a correct turn ON and turn OFF of the PDMOS. The turn ON of the power element, or more accurately, the rise time of the current at turn ON, is a very critical parameter. At a first approach, it appears that the faster the rise time, the lower the turn ON losses.

However, there is a limit introduced by the recovery time of the recirculation diode.

In fact, when the current of the power element is equal to the inductor current, the diode turns OFF and the drain of the power is able to go high. But during its recovery time, the diode can be considered a high value capacitor and this produces a very high peak current, responsible for numerous problems:

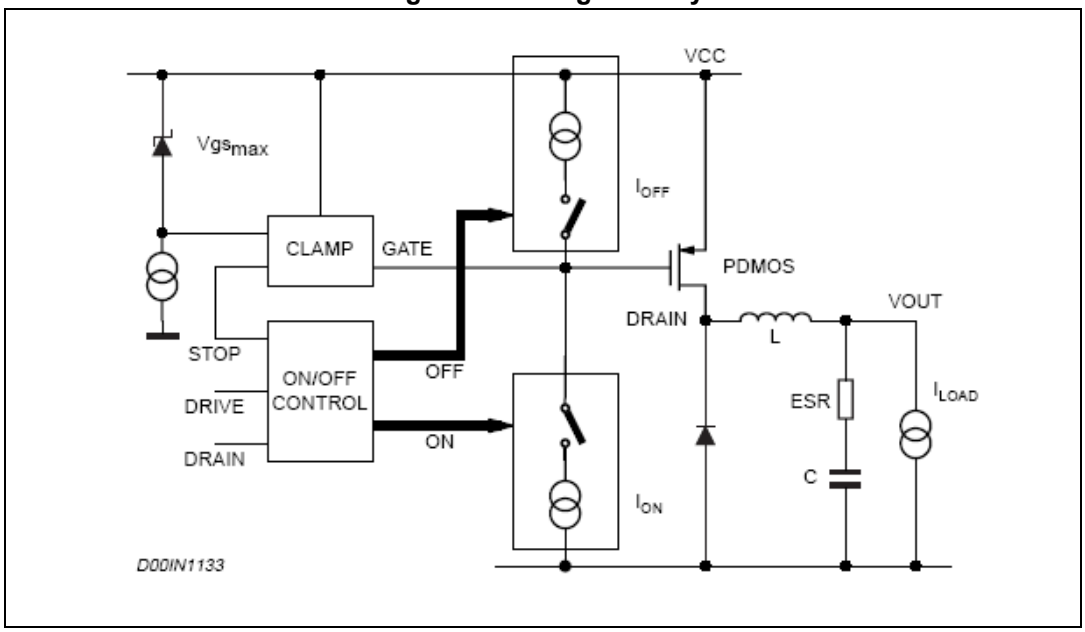
- Spikes on the device supply voltage that cause oscillations (and thus noise) due to the board parasites.
- Turn ON overcurrent leads to a decrease in the efficiency and system reliability.
- Major EMI problems.
- Shorter freewheeling diode life.

The fall time of the current during turn OFF is also critical, as it produces voltage spikes (due to the parasites elements of the board) that increase the voltage drop across the PDMOS.

In order to minimize these problems, a new driving circuit topology has been used and the block diagram is shown in *Figure 8*. The basic idea is to change the current levels used to turn the power switch ON and OFF, based on the PDMOS and the gate clamp status.

This circuitry allows the power switch to be turned OFF and ON quickly and addresses the freewheeling diode recovery time problem. The gate clamp is necessary to ensure that V_{GS} of the internal switch does not go higher than V_{GS}max. The ON/OFF Control block protects against any cross conduction between the supply line and ground.

Figure 8. Driving circuitry



5.7 Inhibit function

The inhibit feature is used to put the device in standby mode. With the INH pin higher than 2.2 V the device is disabled and the power consumption is reduced to less than 100 µA. With the INH pin lower than 0.8 V, the device is enabled. If the INH pin is left floating, an internal pull up ensures that the voltage at the pin reaches the inhibit threshold and the device is disabled. The pin is also V_{CC} compatible.

5.8 Thermal shutdown

The shutdown block generates a signal that turns OFF the power stage if the temperature of the chip goes higher than a fixed internal threshold (150 ± 10 °C). The sensing element of the chip is very close to the PDMOS area, ensuring fast and accurate temperature detection. A hysteresis of approximately 20 °C keeps the device from turning ON and OFF continuously.

6 Additional features and protection

6.1 Feedback disconnection

If the feedback is disconnected, the duty cycle increases towards the maximum allowed value, bringing the output voltage close to the input supply. This condition could destroy the load.

To avoid this hazardous condition, the device is turned OFF if the feedback pin is left floating.

6.2 Output overvoltage protection

Overvoltage protection, or OVP, is achieved by using an internal comparator connected to the feedback, which turns OFF the power stage when the OVP threshold is reached. This threshold is typically 30% higher than the feedback voltage.

When a voltage divider is required to adjust the output voltage (*Figure 15 on page 27*), the OVP intervention will be set at:

Equation 1

$$V_{OVP} = 1.3 \bullet \frac{R_1 + R_2}{R_2} \bullet V_{FB}$$

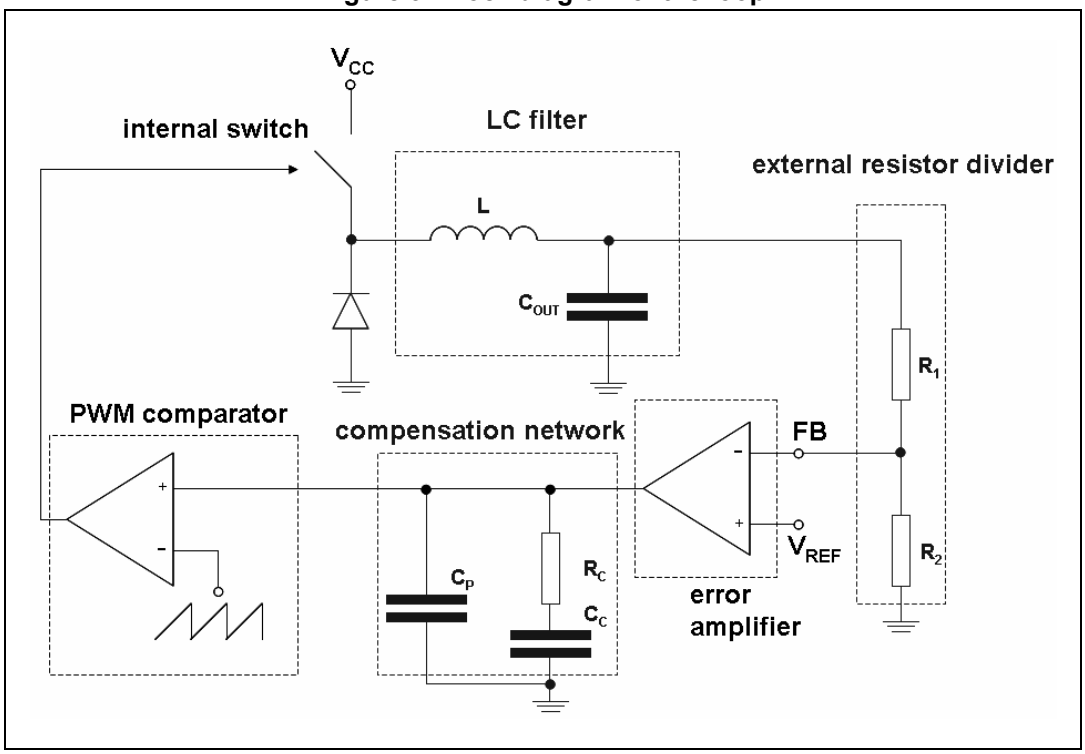
Where R_1 is the resistor connected between the output voltage and the feedback pin, and R_2 is between the feedback pin and ground.

6.3 Zero load

Due to the fact that the internal power is a PDMOS, no boostrap capacitor is required and so the device works properly even with no load at the output. In this case it works in burst mode, with a random burst repetition rate.

7 Closing the loop

Figure 9. Block diagram of the loop



7.1 Error amplifier and compensation network

The output L-C filter of a step-down converter contributes with 180 degrees phase shift in the control loop. For this reason a compensation network between the COMP pin and GROUND is added. The simplest compensation network together with the equivalent circuit of the error amplifier are shown in *Figure 10*. R_C and C_C introduce a pole and a zero in the open loop gain. CP does not significantly affect system stability but it is useful to reduce the noise of the COMP pin.

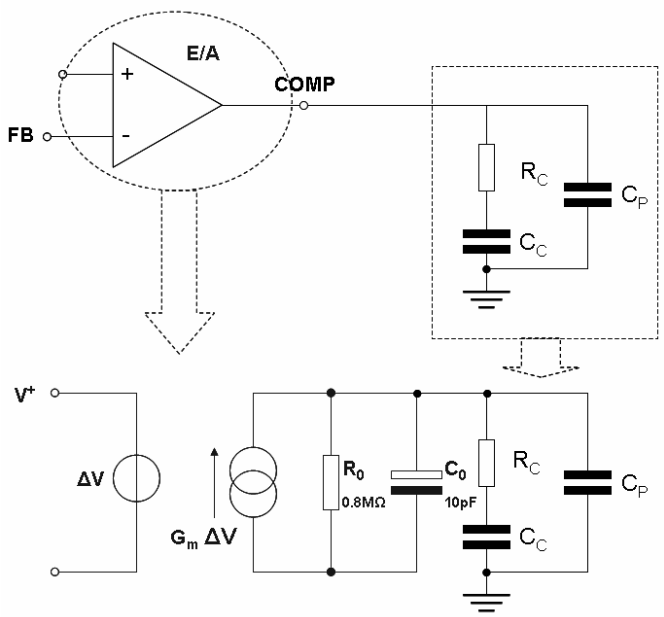
The transfer function of the error amplifier and its compensation network is:

Equation 2

$$A_0(s) = \frac{A_{V0} \bullet (1 + s \bullet R_c \bullet C_c)}{s^2 \bullet R_0 \bullet (C_0 + C_p) \bullet R_c \bullet C_c + s \bullet (R_0 \bullet C_c + R_0 \bullet (C_0 + C_p) + R_c \bullet C_c) + 1}$$

Where $A_{vo} = G_m \cdot R_o$

Figure 10. Error amplifier equivalent circuit and compensation network



The poles of this transfer function are (if $C_c >> C_0 + C_P$):

Equation 3

$$F_{P1} = \frac{1}{2 \bullet \pi \bullet R_0 \bullet C_c}$$

Equation 4

$$F_{P2} = \frac{1}{2 \bullet \pi \bullet R_c \bullet (C_0 + C_p)}$$

whereas the zero is defined as:

Equation 5

$$F_{Z1} = \frac{1}{2 \bullet \pi \bullet R_c \bullet C_c}$$

F_{P1} is the low frequency which sets the bandwidth, while the zero F_{Z1} is usually put near to the frequency of the double pole of the L-C filter (see below). F_{P2} is usually at a very high frequency.

7.2 LC filter

The transfer function of the L-C filter is given by:

Equation 6

$$A_{LC}(s) = \frac{R_{LOAD} \bullet (1 + ESR \bullet C_{OUT} \bullet s)}{s^2 \bullet L \bullet C_{OUT} \bullet (ESR + R_{LOAD}) + s \bullet (ESR \bullet C_{OUT} \bullet R_{LOAD} + L) + R_{LOAD}}$$

where R_{LOAD} is defined as the ratio between V_{OUT} and I_{OUT}.

If R_{LOAD} >> ESR, the previous expression of A_{LC} can be simplified and becomes:

Equation 7

$$A_{LC}(s) = \frac{1 + ESR \bullet C_{OUT} \bullet s}{L \bullet C_{OUT} \bullet s^2 + ESR \bullet C_{OUT} \bullet s + 1}$$

The zero of this transfer function is given by:

Equation 8

$$F_O = \frac{1}{2 \bullet \pi \bullet ESR \bullet C_{OUT}}$$

F_0 is the zero introduced by the ESR of the output capacitor and it is very important to increase the phase margin of the loop.

The poles of the transfer function can be calculated through the following expression:

Equation 9

$$F_{PLC1,2} = \frac{-ESR \bullet C_{OUT} \pm \sqrt{(ESR \bullet C_{OUT})^2 - 4 \bullet L \bullet C_{OUT}}}{2 \bullet L \bullet C_{OUT}}$$

In the denominator of A_{LC} the typical second order system equation can be recognized:

Equation 10

$$s^2 + 2 \bullet \delta \bullet \omega_n \bullet s + \omega^2_n$$

If the damping coefficient δ is very close to zero, the roots of the equation become a double root whose value is ω_n.

Similarly for A_{LC} the poles can usually be defined as a double pole whose value is:

Equation 11

$$F_{PLC} = \frac{1}{2 \bullet \pi \bullet \sqrt{L \bullet C_{OUT}}}$$

7.3 PWM comparator

The PWM gain is given by the following formula:

Equation 12

$$G_{PWM}(s) = \frac{V_{cc}}{(V_{OSCMAX} - V_{OSCMIN})}$$

where V_{OSCMAX} is the maximum value of a sawtooth waveform and V_{OSCMIN} is the minimum value. A voltage feed forward is implemented to ensure a constant GPWM. This is obtained by generating a sawtooth waveform directly proportional to the input voltage V_{CC}.

Equation 13

$$V_{OSCMAX} - V_{OSCMIN} = K \bullet V_{CC}$$

Where *K* is equal to 0.076. Therefore the PWM gain is also equal to:

Equation 14

$$G_{PWM}(s) = \frac{1}{K} = \text{const}$$

This means that even if the input voltage changes, the error amplifier does not change its value to keep the loop in regulation, thus ensuring a better line regulation and line transient response.

In summary, the open loop gain can be expressed as:

Equation 15

$$G(s) = G_{PWM}(s) \bullet \frac{R_2}{R_1 + R_2} \bullet A_O(s) \bullet A_{LC}(s)$$

Example 1

Considering R_C = 4.7 kΩ, C_C = 22 nF and C_P = 220 pF, the poles and zeroes of A_0 are:

F_{P1} = 9 Hz

F_{P2} = 150 kHz

F_{Z1} = 1.5 kHz

If L = 33 µH, C_{OUT} = 100 µF and ESR = 80 mΩ, the poles and zeroes of A_{LC} become:

F_{PLC} = 2.7 kHz

F_{ZESR} = 19.89 kHz

Finally R_1 = 5.6 kΩ and R_2 = 3.3 kΩ.

The gain and phase bode diagrams are plotted respectively in *Figure 11* and *Figure 12*.

Figure 11. Module plot

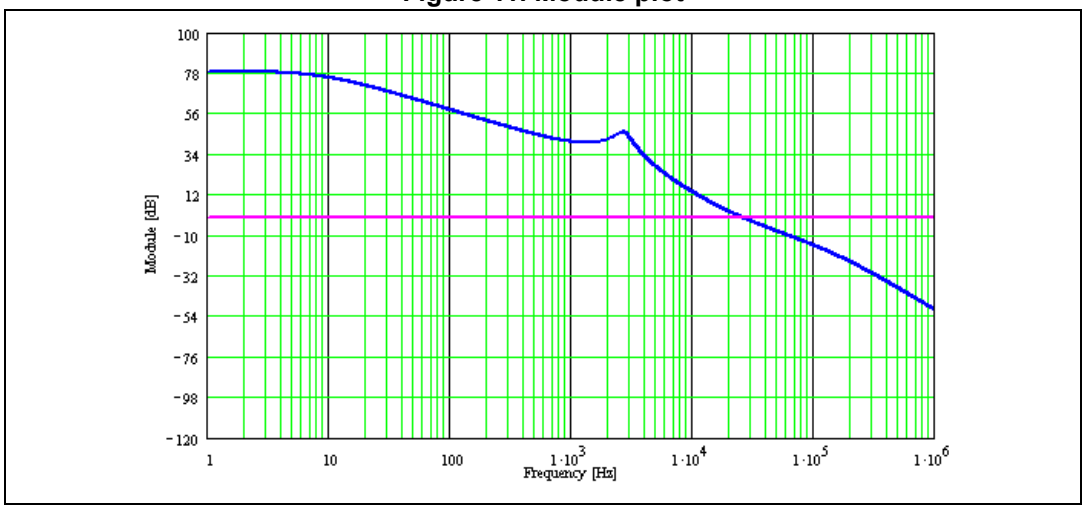
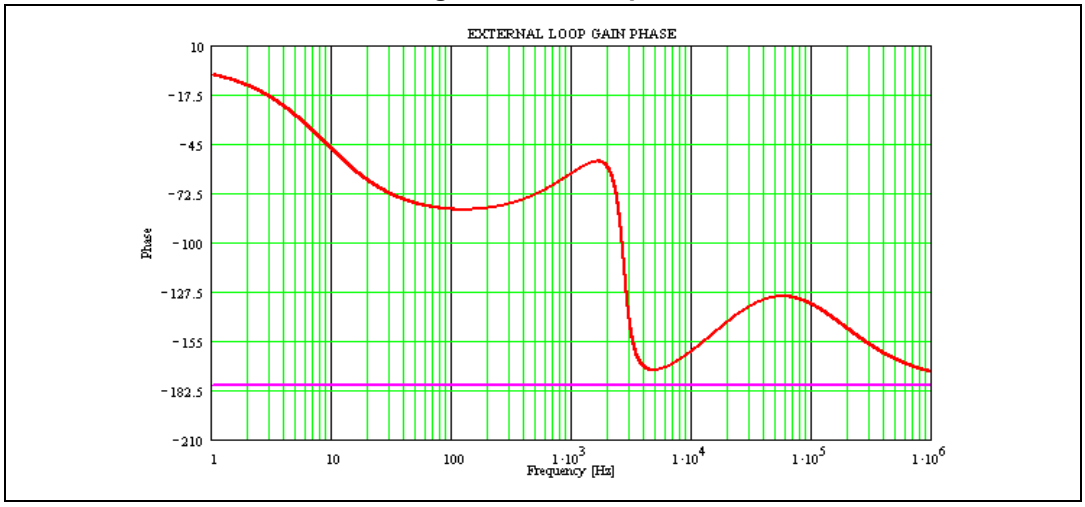


Figure 12. Phase plot



The cut-off frequency and the phase margin are:

Equation 16

$$F_C = 25KHz \quad \text{Phase margin} = 40°$$

8 Application information

8.1 Component selection

- Input capacitor

The input capacitor must be able to support the maximum input operating voltage and the maximum RMS input current.

Since step-down converters draw current from the input in pulses, the input current is squared and the height of each pulse is equal to the output current. The input capacitor has to absorb all this switching current, which can be up to the load current divided by two (worst case, with duty cycle of 50%). For this reason, the quality of these capacitors has to be very high to minimize the power dissipation generated by the internal ESR, thereby improving system reliability and efficiency. The critical parameter is usually the RMS current rating, which must be higher than the RMS input current. The maximum RMS input current (flowing through the input capacitor) is:

Equation 17

$$I_{RMS} = I_O \bullet \sqrt{D - \frac{2 \bullet D^2}{\eta} + \frac{D^2}{\eta^2}}$$

Where η is the expected system efficiency, D is the duty cycle and I_O is the output DC current. This function reaches its maximum value at D = 0.5 and the equivalent RMS current is equal to I_O divided by 2 (considering η = 1). The maximum and minimum duty cycles are:

Equation 18

$$D_{MAX} = \frac{V_{OUT} + V_F}{V_{INMIN} - V_{SW}}$$

and

Equation 19

$$D_{MIN} = \frac{V_{OUT} + V_F}{V_{INMAX} - V_{SW}}$$

Where V_F is the freewheeling diode forward voltage and V_{SW} the voltage drop across the internal PDMOS. Considering the range D_{MIN} to D_{MAX}, it is possible to determine the max. IRMS going through the input capacitor.

Capacitors that can be considered are:

Electrolytic capacitors:

These are widely used due to their low price and their availability in a wide range of RMS current ratings.

The only drawback is that, considering ripple current rating requirements, they are physically larger than other capacitors.

Ceramic capacitors:

If available for the required value and voltage rating, these capacitors usually have a higher RMS current rating for a given physical dimension (due to very low ESR).

The drawback is the considerably high cost.

Tantalum capacitors:

Very good, small tantalum capacitors with very low ESR are becoming more available. However, they can occasionally burn if subjected to very high current during charge.

Therefore, it is better to avoid this type of capacitor for the input filter of the device. They can, however, be subjected to high surge current when connected to the power supply.

Table 6. List of ceramic capacitors for the A5970D

Manufacturer	Series	Capacitor value (µF)	Rated voltage (V)
TAIYO YUDEN	UMK325BJ106MM-T	10	50
MURATA	GRM42-2 X7R 475K 50	4.7	50

High dv/dt voltage spikes on the input side can be critical for DC/DC converters. A good power layout and input voltage filtering help to minimize this issue. In addition to the above considerations, a 1 µF/50 V ceramic capacitor as close as possible to the VCC and GND pins is always suggested to adequately filter VCC spikes.

- Output capacitor

The output capacitor is very important to meet the output voltage ripple requirement.

Using a small inductor value is useful to reduce the size of the choke but it increases the current ripple. So, to reduce the output voltage ripple, a low ESR capacitor is required. Nevertheless, the ESR of the output capacitor introduces a zero in the open loop gain, which helps to increase the phase margin of the system. If the zero goes to a very high frequency, its effect is negligible. For this reason, ceramic capacitors and very low ESR capacitors in general should be avoided.

Tantalum and electrolytic capacitors are usually a good choice for this purpose. A list of some tantalum capacitor manufacturers is provided in *Table 7: Output capacitor selection*.

Table 7. Output capacitor selection

Manufacturer	Series	Cap. value (µF)	Rated voltage (V)	ESR (mΩ)
Sanyo POSCAP(1)	TAE	100 to 470	4 to 16	25 to 35
	THB/C/E	100 to 470	4 to 16	25 to 55
AVX	TPS	100 to 470	4 to 35	50 to 200
KEMET	T494/5	100 to 470	4 to 20	30 to 200
Sprague	595D	220 to 390	4 to 20	160 to 650

1. POSCAP capacitors have some characteristics which are very similar to tantalum.

- Inductor

The inductor value is very important as it fixes the ripple current flowing through the output capacitor. The ripple current is usually fixed at 20 - 40% of I_{omax}, which is 0.2 - 0.4 A with $I_O$max = 1 A. The approximate inductor value is obtained using the following formula:

Equation 20

$$L = \frac{(V_{IN} - V_{OUT})}{\Delta I} \bullet T_{ON}$$

where T_{ON} is the ON time of the internal switch, given by D · T. For example, with V_{OUT} = 3.3 V, V_{IN} = 12 V and ΔI_O = 0.3 A, the inductor value is about 33 µH. The peak current through the inductor is given by:

Equation 21

$$I_{PK} = I_O + \frac{\Delta I}{2}$$

and it can be observed that if the inductor value decreases, the peak current (which must be lower than the current limit of the device) increases. So, when the peak current is fixed, a higher inductor value allows a higher value for the output current. In *Table 8* some inductor manufacturers are listed.

Table 8. Inductor selection

Manufacturer	Series	Inductor value (µH)	Saturation current (A)
Coilcraft	DO3316T	15 to 33	2.0 to 3.0
Coiltronics	UP1B	22 to 33	2.0 to 2.4
BI	HM76-3	15 to 33	2.5 to 3.3
Epcos	B82476	15 to 33	2 to 3
Wurth Elektronik	74456115	15 to 33	2.5 to 3

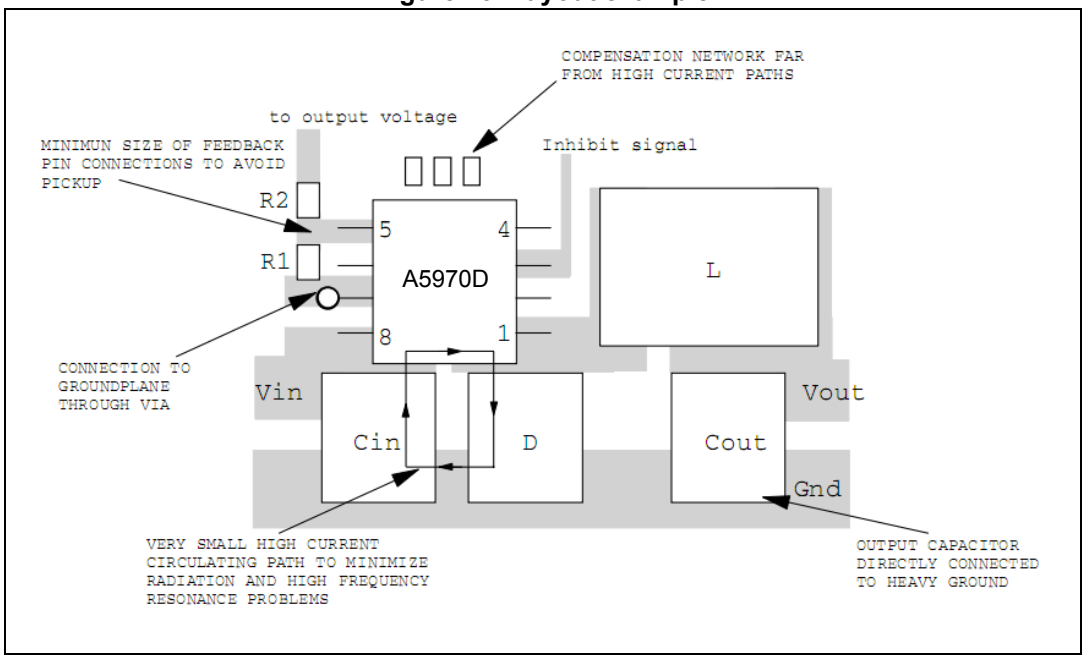
8.2 Layout considerations

The layout of switching DC-DC converters is very important to minimize noise and interference. Power-generating portions of the layout are the main cause of noise and so high switching current loop areas should be kept as small as possible and lead lengths as short as possible.

High impedance paths (in particular the feedback connections) are susceptible to interference, so they should be as far as possible from the high current paths. An layout example is provided in *Figure 13*.

The input and output loops are minimized to avoid radiation and high frequency resonance problems. The feedback pin connections to the external divider are very close to the device to avoid pick-up noise.

Figure 13. Layout example



8.3 Thermal considerations

The dissipated power of the device is tied to three different sources:

- Conduction losses due to the not insignificant R_{DSON}, which are equal to:

Equation 22

$$P_{ON} = R_{DSON} \bullet (I_{OUT})^2 \bullet D$$

Where *D* is the duty cycle of the application. Note that the duty cycle is theoretically given by the ratio between V_{OUT} and V_{IN}, but in practice it is substantially higher than this value to compensate for the losses in the overall application. For this reason, the switching losses related to the R_{DSON} increases compared to an ideal case.

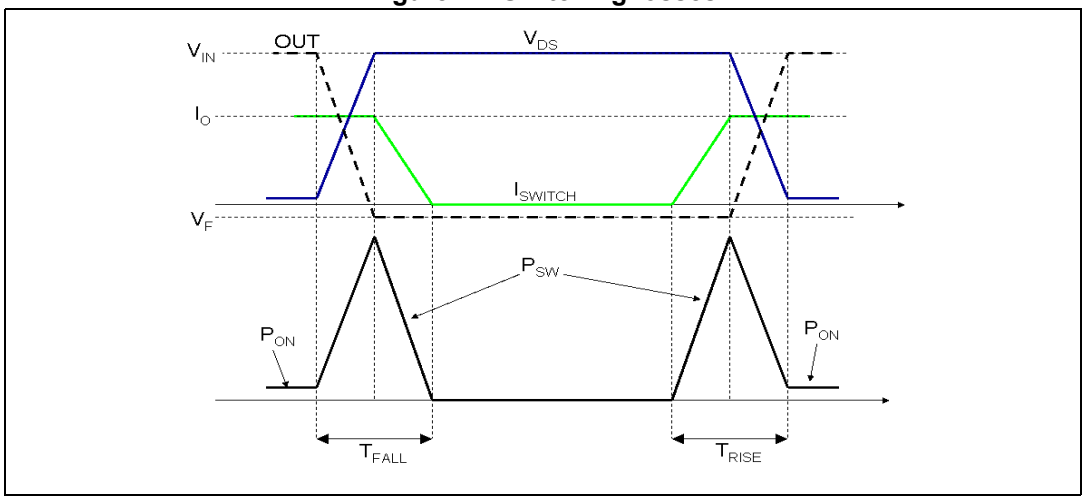
- Switching losses due to turning ON and OFF. These are derived using the following equation:

Equation 23

$$P_{SW} = V_{IN} \bullet I_{OUT} \bullet \frac{(T_{ON} + T_{OFF})}{2} \bullet F_{SW} = V_{IN} \bullet I_{OUT} \bullet T_{SW} \bullet F_{SW}$$

Where T_{RISE} and T_{FALL} represent the switching times of the power element that cause the switching losses when driving an inductive load (see *Figure 14*). T_{SW} is the equivalent switching time.

Figure 14. Switching losses



- Quiescent current losses.

Equation 24

$$P_Q = V_{IN} \bullet I_Q$$

Where I_Q is the quiescent current.

Example 2

- V_{IN} = 12 V
- V_{OUT} = 3.3 V
- I_{OUT} = 1 A

$R_{DS(on)}$ has a typical value of 0.25 at 25 °C and increases up to a maximum value of 0.5 at 150 °C. We can consider a value of 0.4 Ω.

T_{SW} is approximately 70 ns.

I_Q has a typical value of 2.5 mA at V_{IN} = 12 V.

The overall losses are:

Equation 25

$$P_{TOT} = R_{DSON} \bullet (I_{OUT})^2 \bullet D + V_{IN} \bullet I_{OUT} \bullet T_{SW} \bullet F_{SW} + V_{IN} \bullet I_Q =$$
$$= 0.4 \bullet 1^2 \bullet 0.3 + 12 \bullet 1 \bullet 70 \bullet 10^{-9} \bullet 250 \bullet 10^3 + 12 \bullet 2.5 \bullet 10^{-3} \cong 0.36W$$

The junction temperature of the device will be:

Equation 26

$$T_J = T_A + Rth_{J-A} \bullet P_{TOT}$$

Where T_A is the ambient temperature and Rth_{J-A} is the thermal resistance junction to ambient. Considering that the device is mounted on board with a good ground plane, that it has a thermal resistance junction to ambient (Rth_{J-A}) of about 120 °C/W, and an ambient temperature of about 70 °C:

Equation 27

$$T_J = 70 + 0.36 \bullet 120 \cong 110°C$$

8.4 Short-circuit protection

In overcurrent protection mode, when the peak current reaches the current limit, the device reduces the T_{ON} down to its minimum value (approximately 250 nsec) and the switching frequency to approximately one third of its nominal value even when synchronized to an external signal (see *Section 5.4: Current protection on page 11*). In these conditions, the duty cycle is strongly reduced and, in most applications, this is enough to limit the current to ILIM. In any event, in case of heavy short-circuit at the output (V_O = 0 V) and depending on the application conditions (V_{cc} value and parasitic effect of external components) the current peak could reach values higher than ILIM. This can be understood considering the inductor current ripple during the ON and OFF phases:

- ON phase

Equation 28

$$\Delta I_{L\,TON} = \frac{V_{IN} - V_{out} - (DCR_L + R_{DSON}) \cdot I}{L}(T_{ON})$$

- OFF phase

Equation 29

$$\Delta I_{L\,TOFF} = \frac{-(V_D + V_{out} + DCR_L \bullet I)}{L}(T_{OFF})$$

where V_D is the voltage drop across the diode, DCR_L is the series resistance of the inductor.

In short-circuit conditions V_{OUT} is negligible so during T_{OFF} the voltage across the inductor is very small as equal to the voltage drop across parasitic components (typically the DCR of the inductor and the V_{FW} of the free wheeling diode) while during T_{ON} the voltage applied the inductor is instead maximized as approximately equal to V_{IN}.

So *Equation 28* and *Equation 29* in overcurrent conditions can be simplified to:

Equation 30

$$\Delta I_{L\,TON} = \frac{V_{IN} - (DCR_L + R_{DSON}) \cdot I}{L}(T_{ON\,MIN}) \cong \frac{V_{IN}}{L}(250ns)$$

considering T_{ON} that has been already reduced to its minimum.

Equation 31

$$\Delta I_{L\ TOFF} = \frac{-(V_D + V_{out} + DCR_L \bullet I)}{L}(3 \cdot T_{SW}) \cong \frac{-(V_D + V_{out} + DCR_L \bullet I)}{L}(12\mu s)$$

considering that f_{SW} has been already reduced to one third of the nominal.

In case a short-circuit at the output is applied and V_{IN} = 12 V the inductor current is controlled in most of the applications (see *Figure 15*). When the application must sustain the short-circuit condition for an extended period, the external components (mainly the inductor and diode) must be selected based on this value.

In case the V_{IN} is very high, it could occur that the ripple current during T_{OFF} (*Equation 31*) does not compensate the current increase during T_{ON} (*Equation 30*). The *Figure 17* shows an example of a power up phase with $V_{IN} = V_{IN\ MAX}$ = 36 V where $\Delta_{IL\ TON} > \Delta_{IL\ TOFF}$ so the current escalates and the balance between *Equation 30* and *Equation 31* occurs at a current slightly higher than the current limit. This must be taken into account in particular to avoid the risk of an abrupt inductor saturation.

Figure 15. Short-circuit current V_{IN} = 12 V

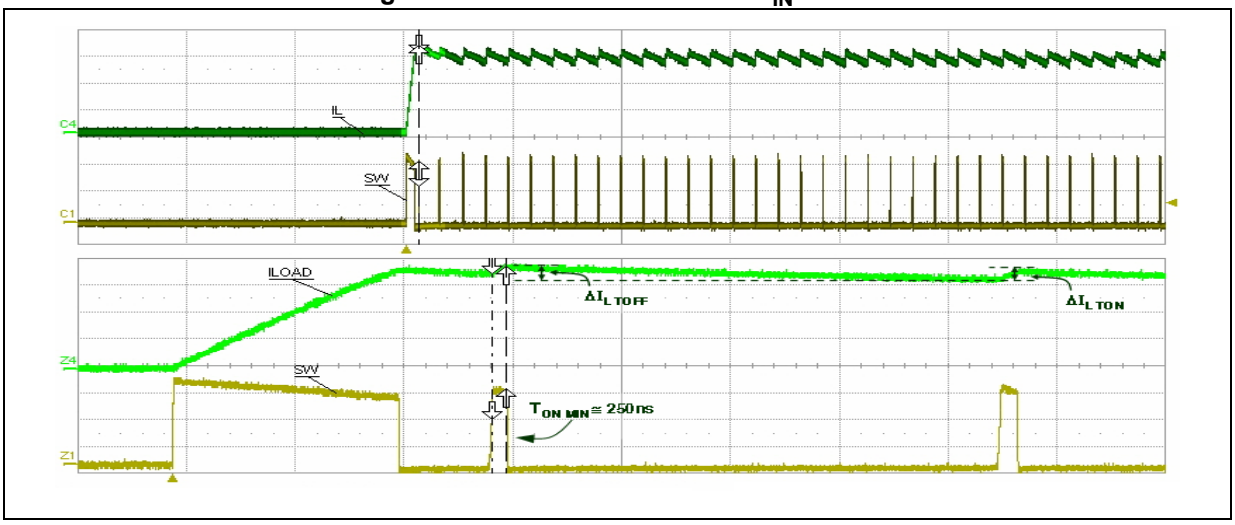


Figure 16. Short-circuit current V_{IN} = 24 V

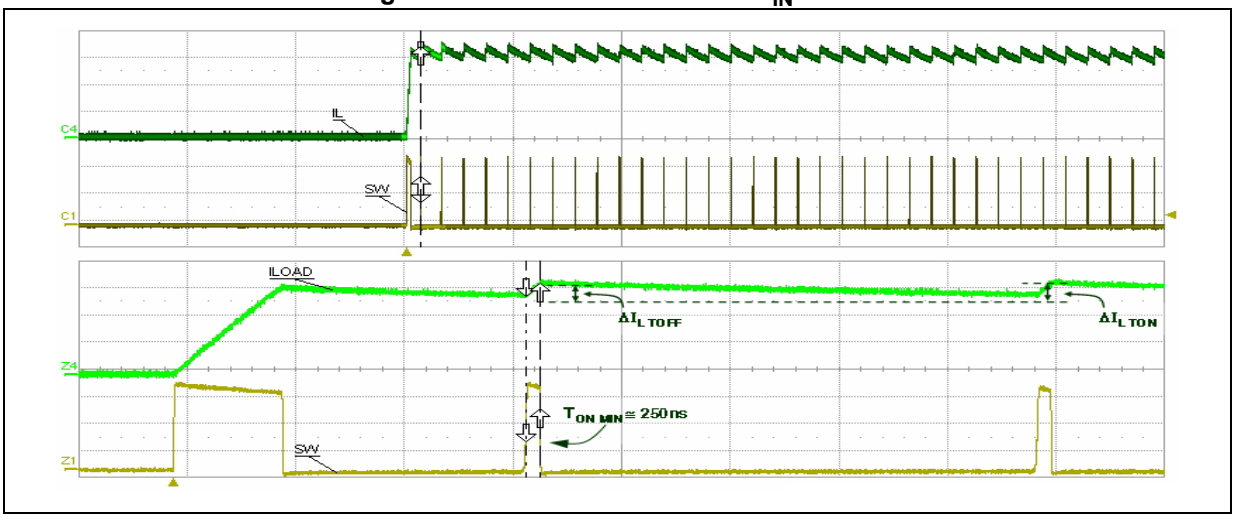
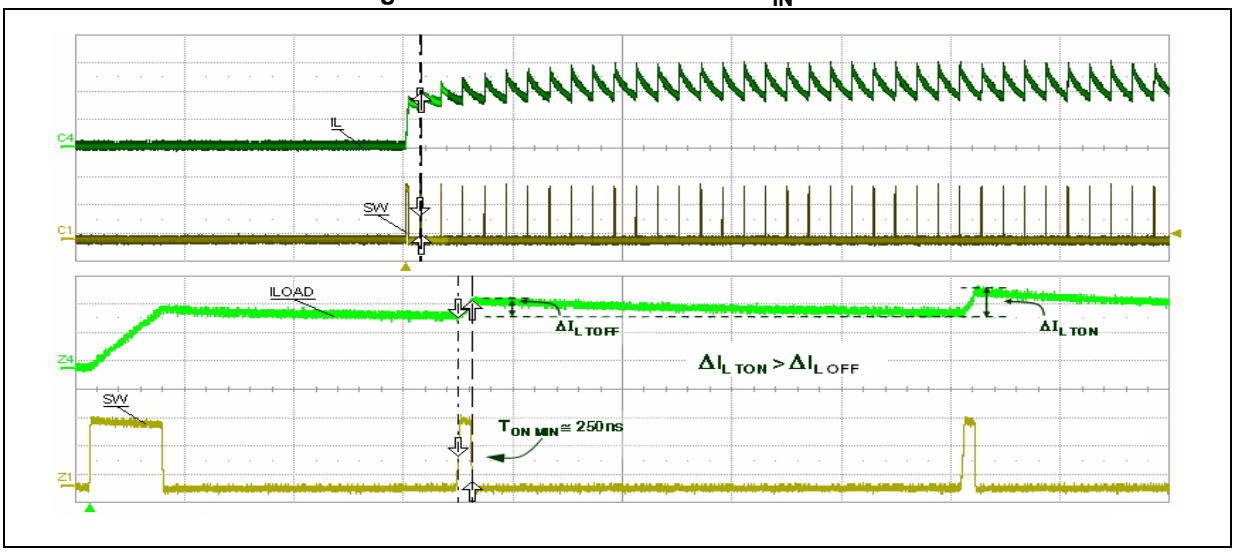


Figure 17. Short-circuit current V_{IN} = 36 V



8.5 Application circuit

Figure 18 shows the evaluation board application circuit, where the input supply voltage, V_{CC}, can range from 4 V to 36 V and the output voltage is adjustable from 1.235 V to 6.3 V due to the voltage rating of the output capacitor.

Figure 18. Evaluation board application circuit

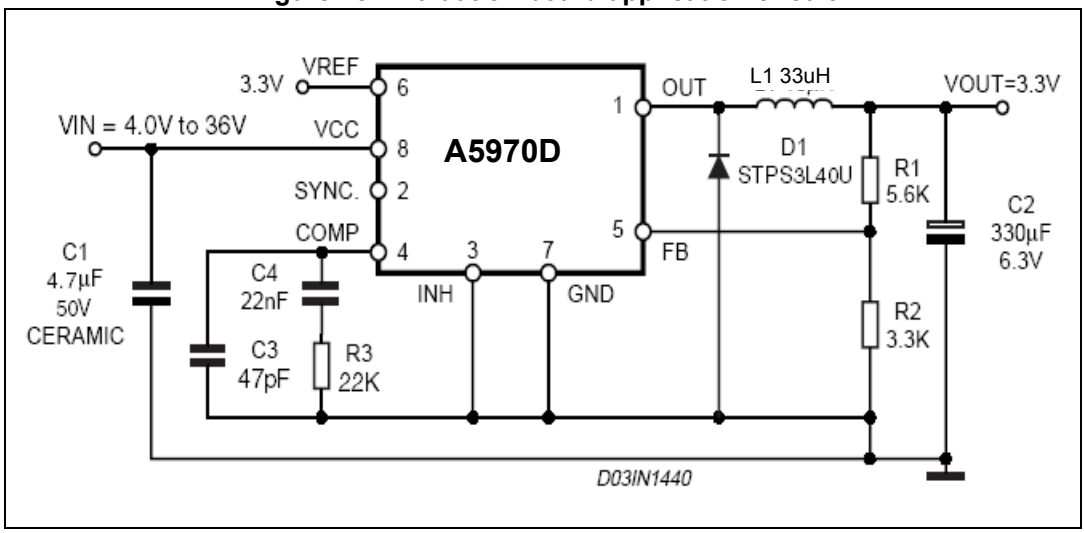


Table 9. Component list

Reference	Part number	Description	Manufacturer
C1	GRM42-2 X7R 475K 50	4.7 µF, 50 V	Murata
C2	POSCAP 6TAE330ML	330 µF, 6.3 V	Sanyo
C3	C1206C221J5GAC	47 pF, 5%, 50 V	KEMET
C4	C1206C223K5RAC	22 nF, 10%, 50 V	KEMET
R1		5.6 kΩ, 1%, 0.1 W 0603	Neohm
R2		3.3 kΩ, 1%, 0.1 W 0603	Neohm
R3		22 kΩ, 1%, 0.1 W 0603	Neohm
D1	STPS3L40U	2 A, 40 V	STMicroelectronics
L1	DO3316T-333MLD	33 µH, 2.1 A	Coilcraft

Figure 19. PCB layout (component side)

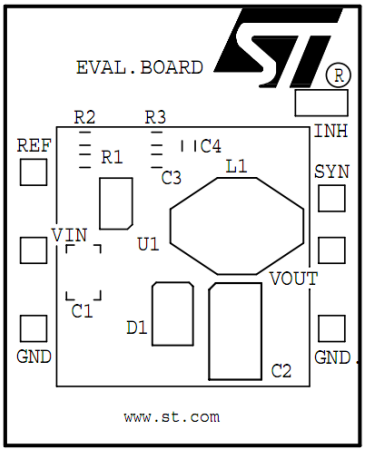


Figure 20. PCB layout (bottom side)

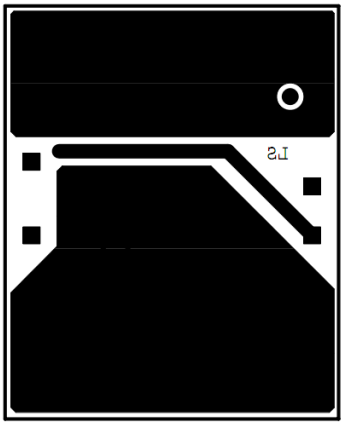
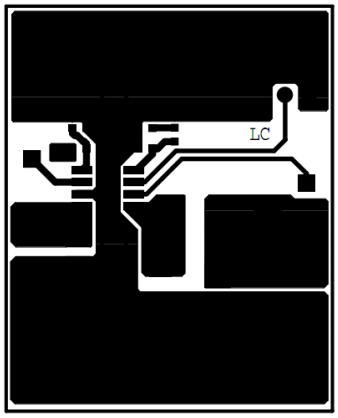


Figure 21. PCB layout (front side)



8.6 Positive buck-boost regulator

The device can be used to implement a step-up/down converter with a positive output voltage.

The output voltage is given by:

Equation 32

$$V_{OUT} = V_{IN} \cdot \frac{D}{1-D}$$

where the ideal duty cycle D for the buck boost converter is:

Equation 33

$$D = \frac{V_{OUT}}{V_{IN} + V_{OUT}}$$

However, due to power losses in the passive elements, the real duty cycle is always higher than this. The real value (that can be measured in the application) should be used in the following formulas.

The peak current flowing in the embedded switch is:

Equation 34

$$I_{SW} = \frac{I_{LOAD}}{1-D} + \frac{I_{RIPPLE}}{2} = \frac{I_{LOAD}}{1-D} + \frac{V_{IN}}{2 \cdot L} \cdot \frac{D}{f_{SW}}$$

while its average current is equal to:

Equation 35

$$I_{SW} = \frac{I_{LOAD}}{1-D}$$

This is due to the fact that the current flowing through the internal power switch is delivered to the output only during the OFF phase.

The switch peak current must be lower than the minimum current limit of the overcurrent protection (see *Table 4: Electrical characteristics on page 6* for details) while the average current must be lower than the rated DC current of the device.

As a consequence, the maximum output current is:

Equation 36

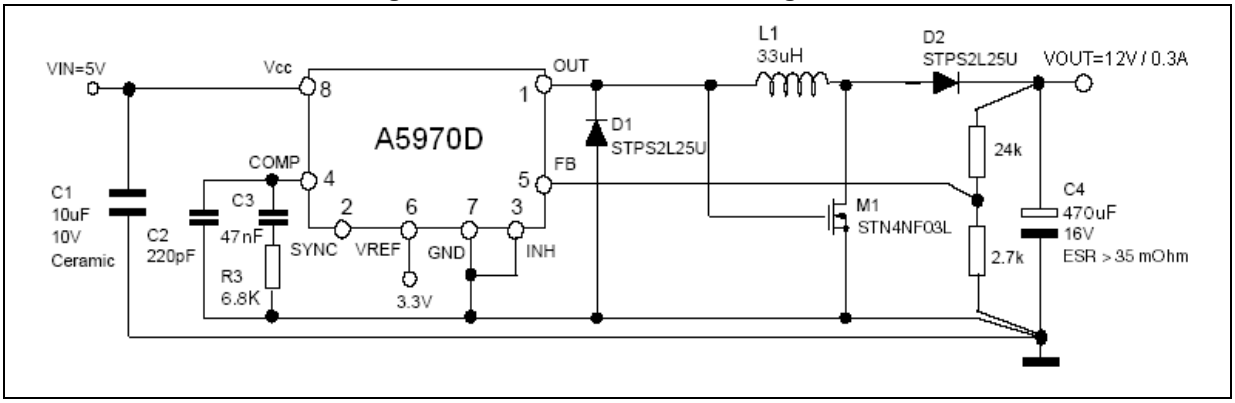
$$I_{OUT\ MAX} \cong I_{SW\ MAX} \cdot (1-D)$$

where $I_{SW\ MAX}$ represents the rated current of the device.

The current capability is reduced by the term (1 - D) and so, for example, with a duty cycle of 0.5, and considering an average current through the switch of 1 A, the maximum output current deliverable to the load is 0.5 A.

Figure 22 shows the schematic circuit of this topology for a 12 V output voltage and 5 V input.

Figure 22. Positive buck-boost regulator



8.7 Negative buck-boost regulator

In *Figure 23*, the schematic circuit for a standard buck-boost topology is shown. The output voltage is:

Equation 37

$$V_{OUT} = -V_{IN} \cdot \frac{D}{1-D}$$

where the ideal duty cycle D for the buck boost converter is:

Equation 38

$$D = \frac{-V_{OUT}}{V_{IN} - V_{OUT}}$$

The considerations given in *Section 8.6* for the real duty cycle are still valid here.

Also the *Equation 34* till *Equation 36* can be used to calculate the maximum output current.

So, as an example, considering the conversion V_{IN} = 12 V to V_{OUT} = -5 V, I_{LOAD} = 0.2 A:

Equation 39

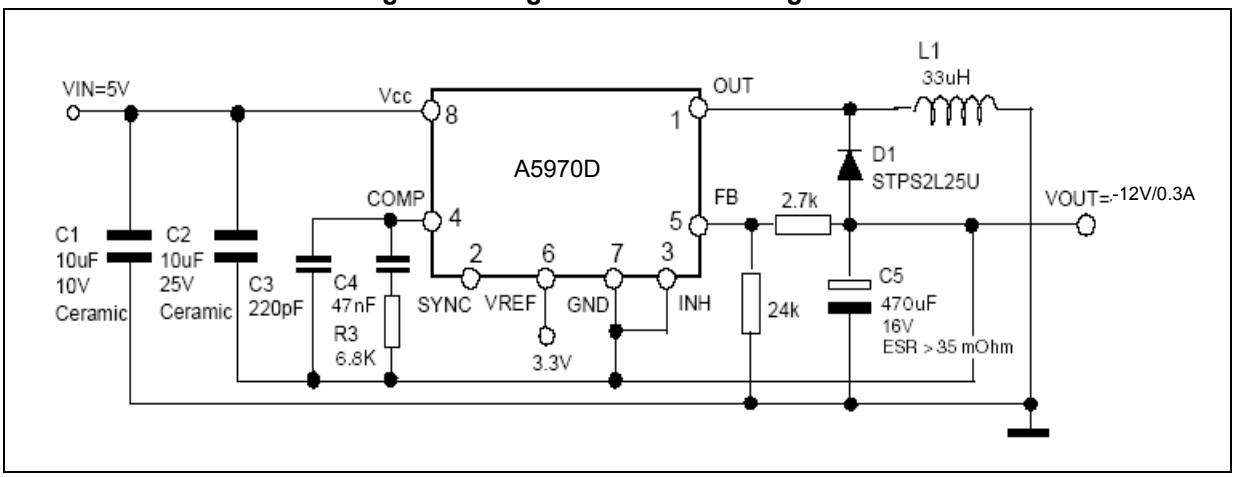
$$D = \frac{5}{5+12} = 0.706$$

Equation 40

$$I_{SW} = \frac{I_{LOAD}}{1-D} = \frac{0.2}{1-0.706} = 0.7A$$

An important thing to take into account is that the ground pin of the device is connected to the negative output voltage. Therefore, the device is subjected to a voltage equal to V_{IN} - V_O, which must be lower than 36 V (the maximum operating input voltage).

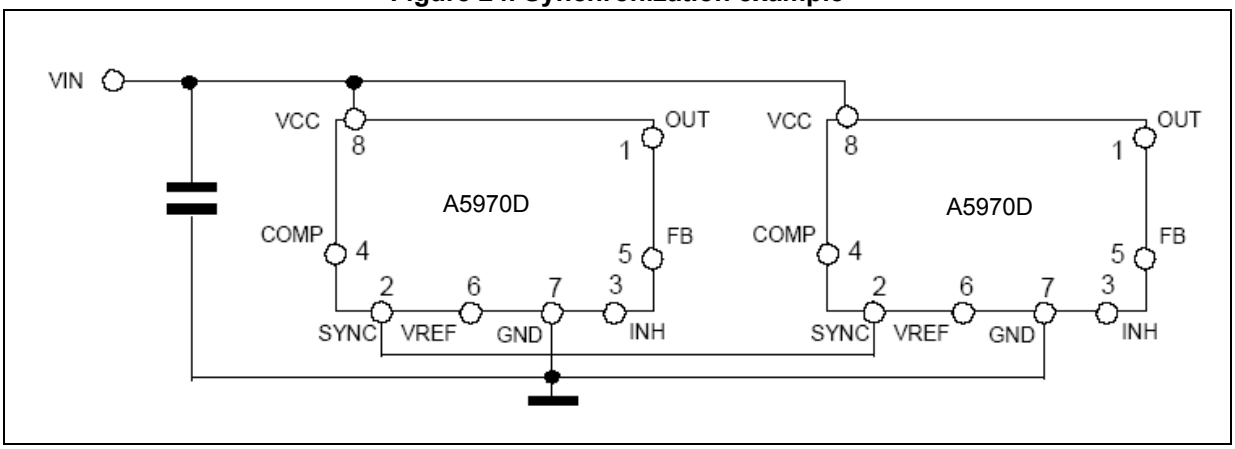
Figure 23. Negative buck-boost regulator



8.8 Synchronization example

See *Section 5.3: Oscillator and synchronization on page 10* for details.

Figure 24. Synchronization example



8.9 Compensation network with MLCC at the output

MLCCs (multiple layer ceramic capacitor) with values in the range of 10 µF - 22 µF and rated voltages in the range of 10 V - 25 V are available today at relatively low cost from many manufacturers.

These capacitors have very low ESR values (a few mΩ) and thus are occasionally used for the output filter in order to reduce the voltage ripple and the overall size of the application.

However, a very low ESR value affects the compensation of the loop (see *Section 7: Closing the loop on page 16*) and in order to keep the system stable, a more complicated compensation network may be required. However, due to the architecture of the internal error amplifier the bandwidth with this compensation is limited.

That is why output capacitors with a not negligible ESR are suggested. The selection of the output capacitor have to guarantee that the zero introduced by this component is inside the designed system bandwidth and close to the frequency of the double pole introduced by the LC filter. A general rule for the selection of this compound for the system stability is provided in *Equation 41*.

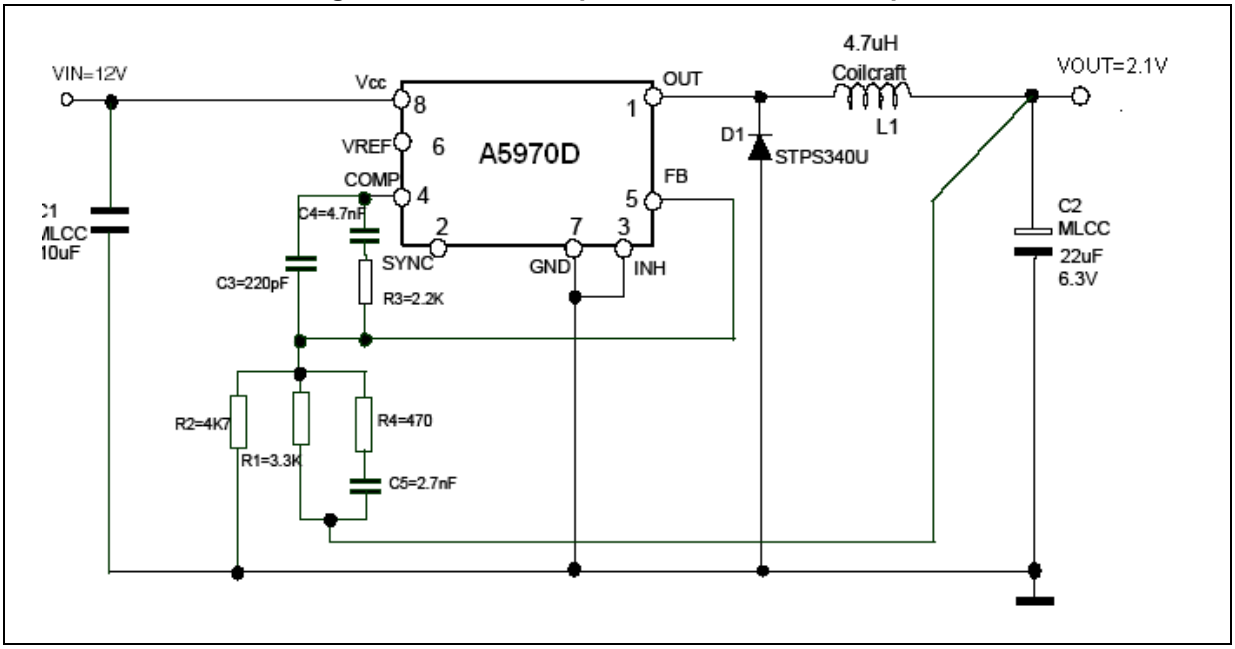
Equation 41

$$f_{Z\,ESR} = \frac{1}{2 \cdot \pi \cdot ESR \cdot C_{OUT}} < \text{bandwidth}$$

$$f_{LC} < f_{Z\,ESR} < 10 \cdot f_{LC}$$

Figure 25 shows an example of a compensation network stabilizing the system with ceramic capacitors at the output (the optimum component value depends on the application).

Figure 25. MLCC compensation network example

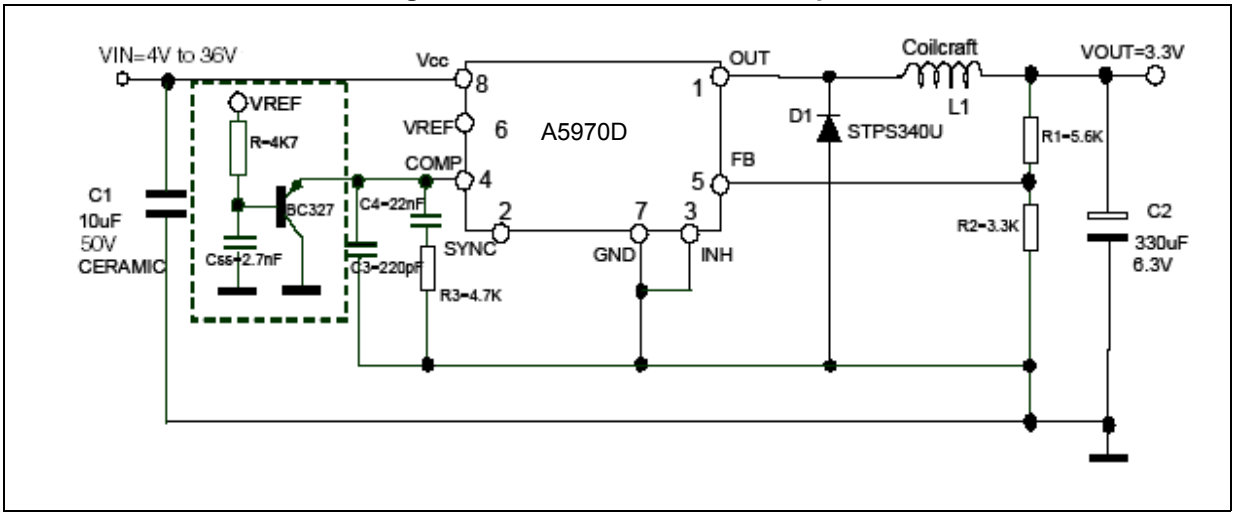


8.10 External SOFT_START network

At a startup the device can quickly increase the current up to the current limit in order to charge the output capacitor. If soft ramp-up of the output voltage is required, an external soft-start network can be implemented as shown in *Figure 26*. The capacitor C is charged up to an external reference through R and the BJT clamps the COMP pin.

This clamps the duty cycle, limiting the slew rate of the output voltage.

Figure 26. Soft-start network example



9 Typical characteristics

Figure 27. Line regulation

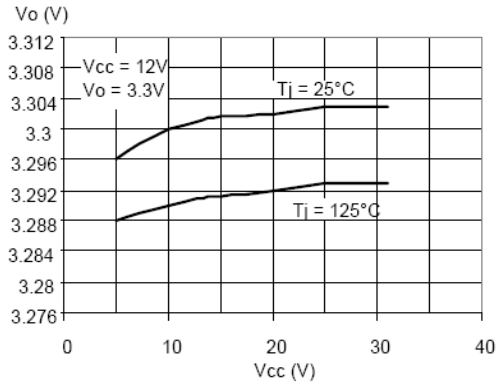


Figure 28. Load regulation

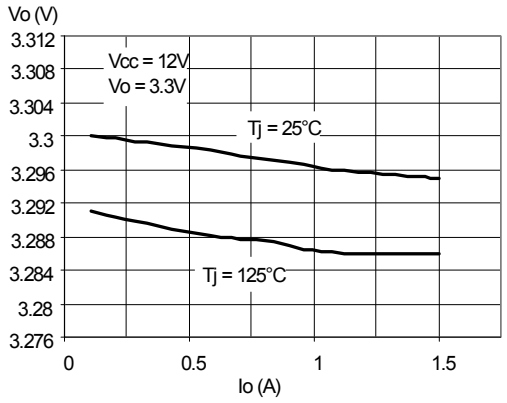


Figure 29. Output voltage vs. junction temperature

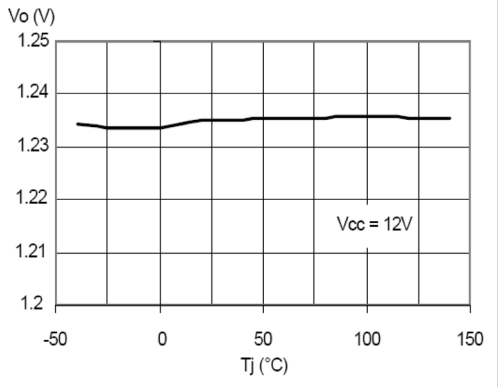


Figure 30. Switching frequency vs. junction temperature

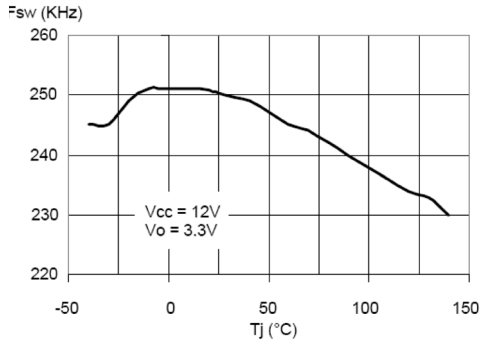


Figure 31. Quiescent current vs. junction temperature

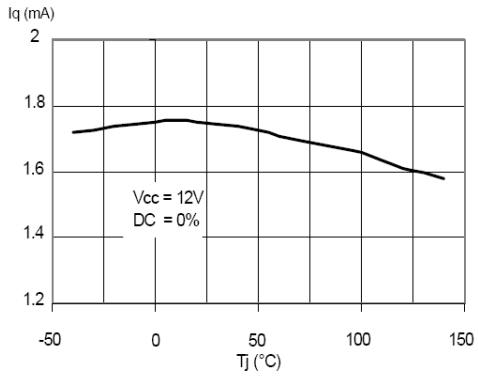


Figure 32. Shutdown current vs. junction temperature

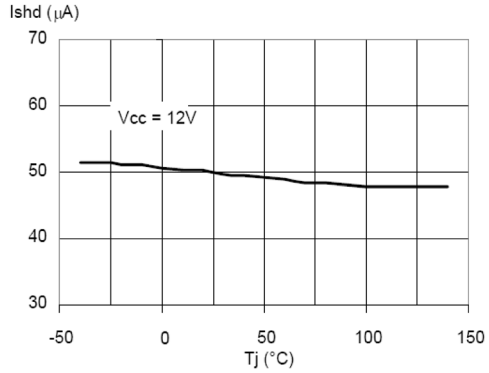


Figure 33. Junction temperature vs. output current - V_{IN} = 5 V

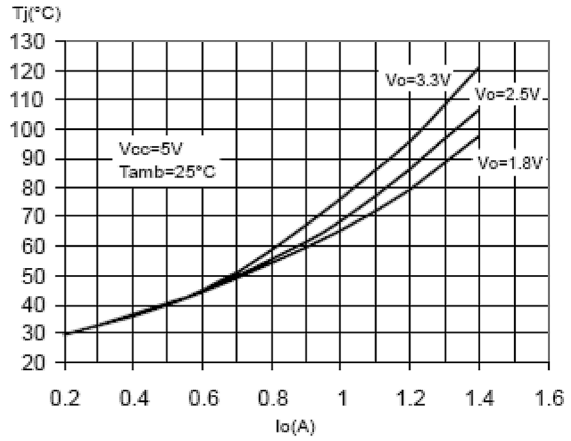


Figure 34. Junction temperature vs. output current - V_{IN} = 12 V

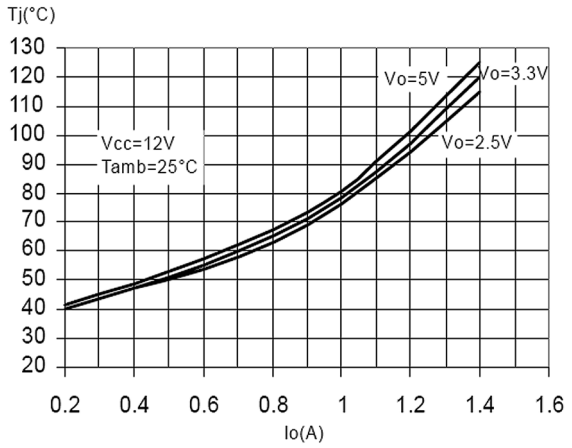


Figure 35. Efficiency vs. output current - V_{IN} = 5 V

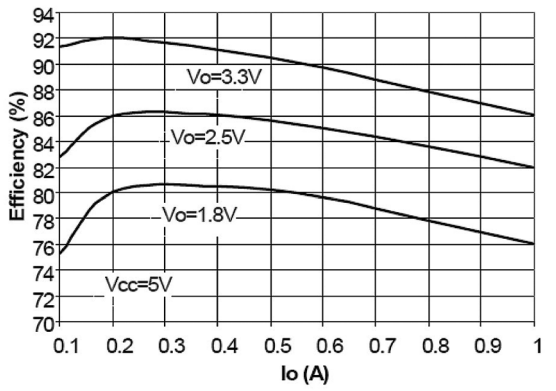
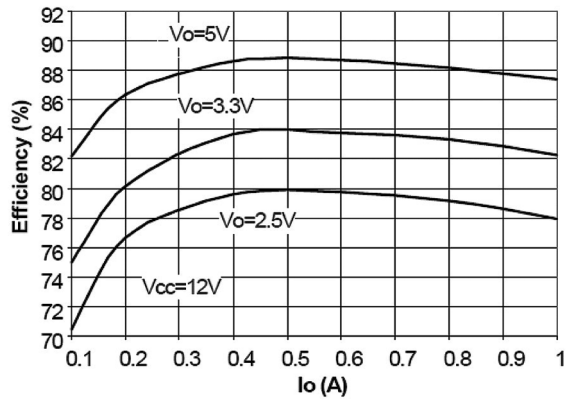


Figure 36. Efficiency vs. output current - V_{IN} = 12 V



10 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

10.1 SO-8 package information

Figure 37. SO-8 package outline

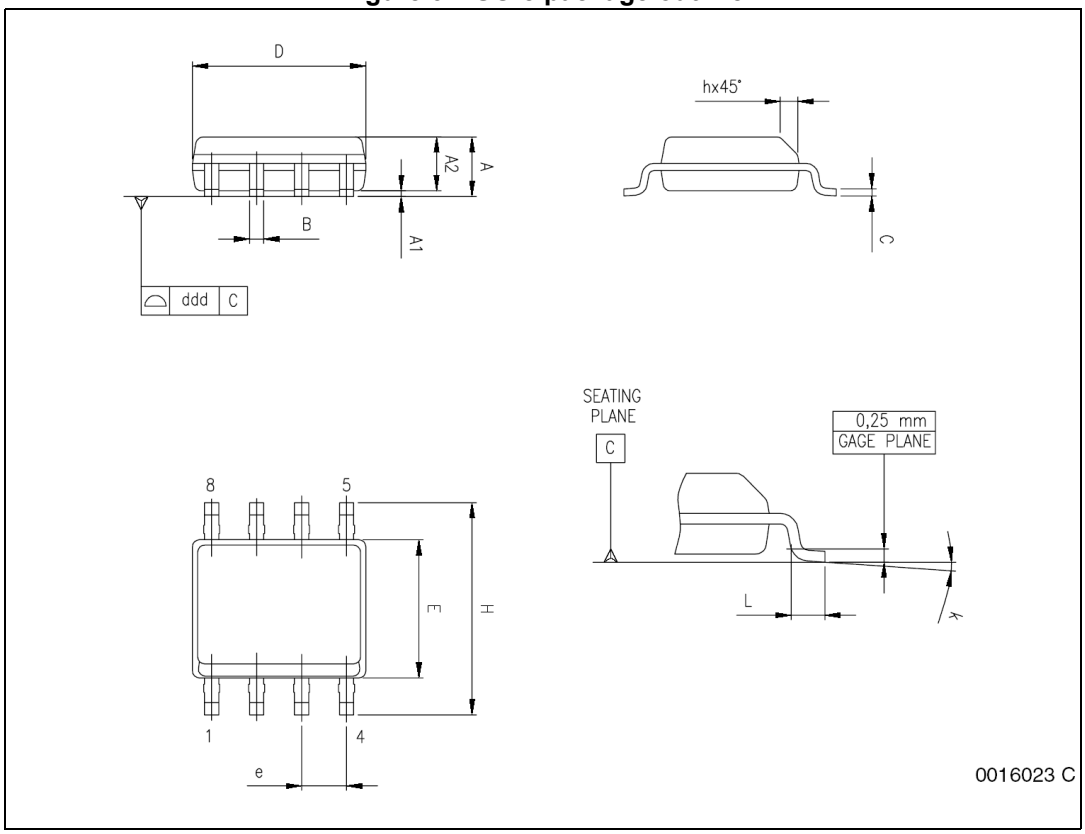


Table 10. SO-8 package mechanical data

Symbol	Dimensions					
	mm			inch		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	1.35		1.75	0.053		0.069
A1	0.10		0.25	0.004		0.010
A2	1.10		1.65	0.043		0.065
B	0.33		0.51	0.013		0.020
C	0.19		0.25	0.007		0.010
D (1)	4.80		5.00	0.189		0.197
E	3.80		4.00	0.15		0.157
e		1.27			0.050	
H	5.80		6.20	0.228		0.244
h	0.25		0.50	0.010		0.020
L	0.40		1.27	0.016		0.050
k	0° (min.), 8° (max.)					
ddd			0.10			0.004

1. Dimensions D does not include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.15 mm (.006 inch) in total (both sides).

11 Order codes

Table 11. Ordering information

Order code	Package	Packaging
A5970D	SO-8	Tube
A5970D013TR		Tape and reel

12 Revision history

Table 12. Document revision history

Date	Revision	Changes
06-Aug-2007	1	Initial release.
24-Oct-2007	2	Updated: Table 4 on page 5
2-May-2008	3	Updated cover page, Table 4 on page 5
27-Aug-2008	4	Updated cover page and Table 4 on page 5
22-Apr-2009	5	Updated first feature in coverpage
03-Nov-2009	6	Updated *Table 4 on page 6* and added *Figure 28 on page 36*.
28-Mar-2014	7	Updated *Table 4: Electrical characteristics on page 6* (added value "∞" to "R_L" in "Error amplifier" part). Updated *Section 8.1: Component selection on page 21* (*Table 6*: updated units in "Capacitor value", added text below *Table 6*). Updated titles from *Figure 33* to *Figure 36* (added values of "V_{IN}"). Updated *Section 10: Package information on page 38* (reversed order of *Figure 37* and *Table 10*, updated titles, minor modifications). Updated cross-references throughout document. Minor modifications throughout document.
12-May-2015	8	Updated *Figure 33 on page 37* to *Figure 36 on page 37* (replaced by new figures). Minor modifications throughout document.
04-Nov-2015	9	Added *Section 11: Order codes on page 40*.

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