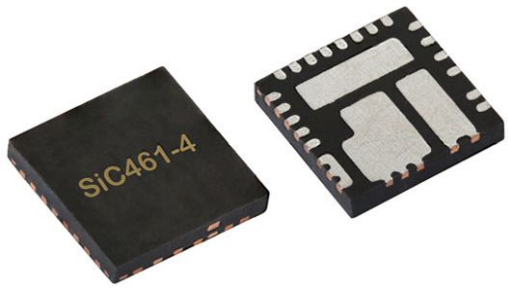
4.5 V to 60 V Input, 2 A, 4 A, 6 A, 10 A Synchronous Buck Regulators



DESCRIPTION

The SiC46x is a family of wide input voltage high efficiency synchronous buck regulators with integrated high side and low side power MOSFETs. Its power stage is capable of supplying high continuous current at up to 2 MHz switching frequency. This regulator produces an adjustable output voltage down to 0.8 V from 4.5 V to 60 V input rail to accommodate a variety of applications, including computing, consumer electronics, telecom, and industrial.

SiC46x's architecture delivers ultrafast transient response with minimum output capacitance and tight ripple regulation at very light load. The device enables loop stability regardless of the type of output capacitor used, including low ESR ceramic output capacitors. The device also incorporates a power saving scheme that significantly increases light load efficiency. The regulator integrates a full protection feature set, including over current protection (OCP), output overvoltage protection (OVP), short circuit protection (SCP), output undervoltage protection (UVP) and thermal shutdown (OTP). It also has UVLO for input rail and a user programmable soft start.

The SiC46x family is available in 2 A, 4 A, 6 A, 10 A pin compatible 5 mm by 5 mm lead (Pb)-free power enhanced MLP55-27L package.

TYPICAL APPLICATION CIRCUIT

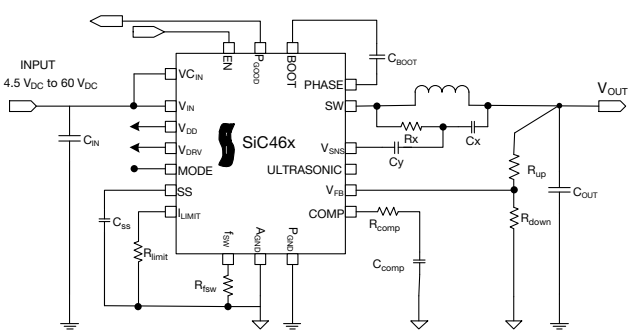


Fig. 1 - Typical Application Circuit for SiC46x

FEATURES

- Versatile
  - Single supply operation from 4.5 V to 60 V input voltage
  - Adjustable output voltage down to 0.8 V
  - Scalable solution 2 A (SiC464), 4 A (SiC463), 6 A (SiC462), 10 A (SiC461)
  - Output voltage tracking and sequencing with pre-bias start up
  - ± 1 % output voltage accuracy at -40 °C to +125 °C
- Highly efficient
  - 98 % peak efficiency
  - 4 µA supply current at shutdown
  - 235 µA operating current not switching
- Highly configurable
  - Adjustable switching frequency from 100 kHz to 2 MHz
  - Adjustable soft start and adjustable current limit
  - 3 modes of operation, forced continuous conduction, power save or ultrasonic
- Robust and reliable
  - Output over voltage protection
  - Output under voltage / short circuit protection with auto retry
  - Power good flag and over temperature protection
  - Supported by Vishay PowerCAD online design simulation
- Design support tools
  - PowerCAD online design simulation (vishay.transim.com)
  - External component calculator (www.vishay.com/doc?75760)
  - Schematic, design, BOM, and gerber files (www.vishay.com/doc?75763)
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

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APPLICATIONS

- Industrial and automation
- Home automation
- Industrial and server computing
- Networking, telecom, and base station power supplies
- Wall transformer regulation
- Robotics
- High end hobby electronics: remote control cars, planes, and drones
- Battery management systems
- Power tools
- Vending, ATM, and slot machines

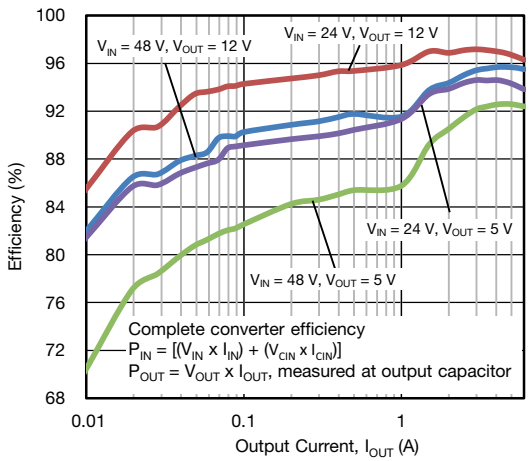

Fig. 2 - SiC462 Efficiency vs. Output Current

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PIN CONFIGURATION

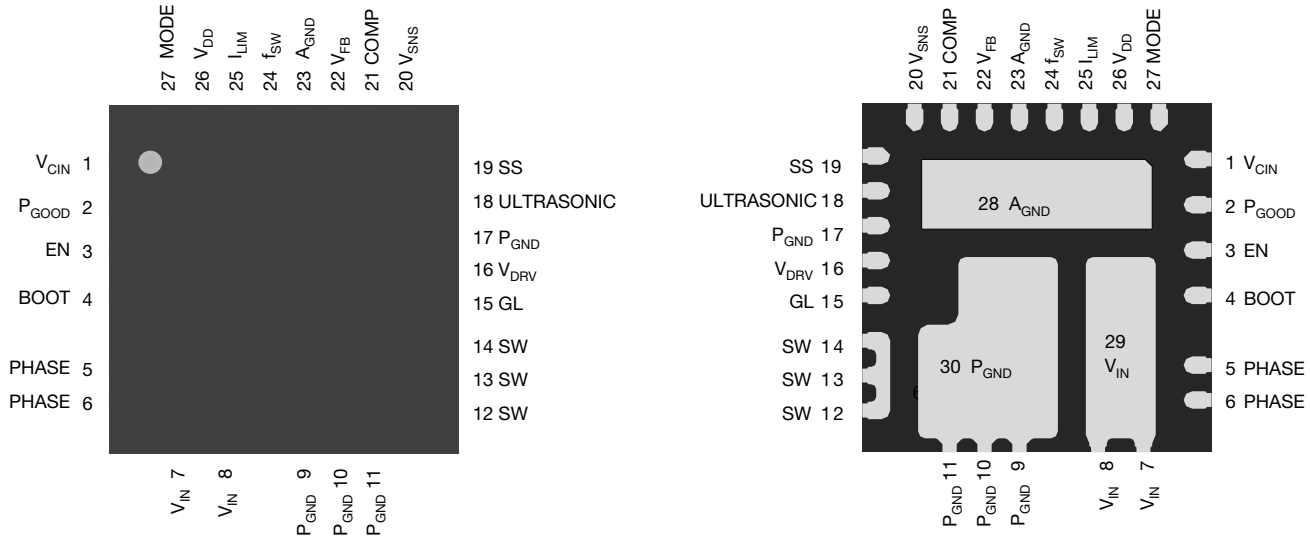

Fig. 3 - SiC46x Pin Configuration

PIN DESCRIPTION		
PIN NUMBER	**SYMBOL**	**DESCRIPTION**
1	V_{CIN}	Supply voltage for internal regulators V_{DD} and V_{DRV}. This pin should be tied to V_{IN}, but can also be connected to a lower supply voltage (> 5 V) to reduce losses in the internal linear regulators
2	P_{GOOD}	Open-drain power good indicator - high impedance indicates power is good. An external pull-up resistor is required
3	EN	Enable pin
4	BOOT	High side driver bootstrap voltage
5, 6	PHASE	Return path of high side gate driver
7, 8, 29	V_{IN}	Power stage input voltage. Drain of high side MOSFET
9, 10, 11, 17, 30	P_{GND}	Power ground
12, 13, 14	SW	Power stage switch node
15	GL	Low side MOSFET gate signal
16	V_{DRV}	Supply voltage for internal gate driver. When using the internal LDO as a bias power supply, V_{DRV} is the LDO output. Connect a 4.7 µF decoupling capacitor to P_{GND}
18	ULTRASONIC	Float to disable ultrasonic mode, connect to V_{DD} to enable. Depending on the operation mode set by the mode pin, power save mode or forced continuous mode will be enabled when the ultrasonic mode is disabled
19	SS	Set the soft start ramp by connecting a capacitor to A_{GND}. An internal current source will charge the capacitor
20	V_{SNS}	Power inductor signal feedback pin for system stability compensation
21	COMP	Output of the internal error amplifier. The feedback loop compensation network is connected from this pin to the V_{FB} pin
22	V_{FB}	Feedback input for switching regulator used to program the output voltage - connect to an external resistor divider from V_{OUT} to A_{GND}
23, 28	A_{GND}	Analog ground
24	f_{SW}	Set the on-time by connecting a resistor to A_{GND}
25	I_{LIMIT}	Set the current limit by connecting a resistor to A_{GND}
26	V_{DD}	Bias supply for the IC. V_{DD} is an LDO output, connect a 1 µF decoupling capacitor to A_{GND}
27	Mode	Set various operation modes by connecting a resistor to A_{GND}. See specification table for details

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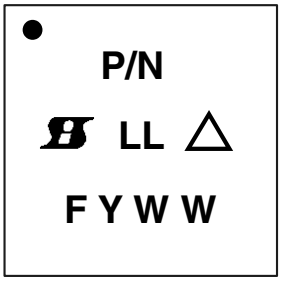
ORDERING INFORMATION		
PART NUMBER	**PACKAGE**	**MARKING CODE**
SiC461ED-T1-GE3	PowerPAK® MLP55-27L	SiC461
SiC461EVB	Reference board	
SiC462ED-T1-GE3	PowerPAK® MLP55-27L	SiC462
SiC462EVB	Reference board	
SiC463ED-T1-GE3	PowerPAK® MLP55-27L	SiC463
SiC463EVB	Reference board	
SiC464ED-T1-GE3	PowerPAK® MLP55-27L	SiC464
SiC464EVB	Reference board	

PART MARKING INFORMATION



● = pin 1 indicator
P/N = part number code
= Siliconix logo
△ = ESD symbol
F = assembly factory code
Y = year code
WW = week code
LL = lot code

ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C, unless otherwise noted)			
ELECTRICAL PARAMETER	**CONDITIONS**	**LIMITS**	**UNIT**
EN, V_{CIN}, V_{IN}	Reference to P_{GND}	-0.3 to +66	V
SW / PHASE	Reference to P_{GND}	-0.3 to +66	
V_{DRV}	Reference to P_{GND}	-0.3 to +6	
V_{DD}	Reference to A_{GND}	-0.3 to +6	
SW / PHASE (AC)	100 ns	-10 to +72	
BOOT		-0.3 to V_{PHASE} + V_{DRV}	
A_{GND} to P_{GND}		-0.3 to +0.3	
All other pins	Reference to A_{GND}	-0.3 to V_{DD} + 0.3	
Temperature			
Junction temperature	T_J	-40 to +150	°C
Storage temperature	T_{STG}	-65 to +150	
Power Dissipation			
Thermal resistance from junction to ambient		12	°C/W
Thermal resistance from junction to case		2	
ESD Protection			
Electrostatic discharge protection	Human body model, JESD22-A114	2000	V
	Charged device model, JESD22-A101	500	

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating/conditions for extended periods may affect device reliability.

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RECOMMENDED OPERATING CONDITIONS (all voltages referenced to GND = 0 V)				
PARAMETER	**MIN.**	**TYP.**	**MAX.**	**UNIT**
Input voltage (V_{IN})	4.5	-	60	V
Control input voltage (V_{CIN}) [1]	4.5	-	60	
Enable (EN)	0	-	60	
Bias supply (V_{DD})	4.75	5	5.25	
Drive supply voltage (V_{DRV})	4.75	5.3	5.55	
Output voltage (V_{OUT})	0.8	-	0.92 x V_{IN}	
Temperature				
Recommended ambient temperature	-40 to +105			°C
Operating junction temperature	-40 to +125			

Note

[1] For input voltages below 5 V, provide a separate supply to V_{CIN} of at least 5 V to prevent the internal V_{DD} rail UVLO from triggering

ELECTRICAL SPECIFICATIONS (V_{IN} = V_{CIN} = 48 V, T_J = -40 °C to +125 °C, unless otherwise stated)						
PARAMETER	**SYMBOL**	**TEST CONDITIONS**	**MIN.**	**TYP.**	**MAX.**	**UNIT**
Power Supplies						
V_{DD} supply	V_{DD}	V_{IN} = V_{CIN} = 6 V to 60 V, V_{EN} = 5 V, not switching	4.75	5	5.25	V
		V_{IN} = V_{CIN} = 5 V, V_{EN} = 5 V, not switching	4.7	5	-	
V_{DD} dropout	$V_{DD_DROPOUT}$	V_{IN} = V_{CIN} = 5 V, I_{VDD} = 1 mA	-	70	-	mV
V_{DD} UVLO threshold, rising	V_{DD_UVLO}		4	4.25	4.5	V
V_{DD} UVLO hysteresis	$V_{DD_UVLO_HYST}$		-	225	-	mV
Maximum V_{DD} current	I_{DD}	V_{IN} = V_{CIN} = 6 V to 60 V	3	-	-	mA
V_{DRV} supply	V_{DRV}	V_{IN} = V_{CIN} = 6 V to 60 V, V_{EN} = 5 V, not switching	5.1	5.3	5.55	V
		V_{IN} = V_{CIN} = 5 V, V_{EN} = 5 V, not switching	4.8	5	5.2	
V_{DRV} dropout	$V_{DRV_DROPOUT}$	V_{IN} = V_{CIN} = 5 V, I_{VDD} = 10 mA	-	160	-	mV
Maximum V_{DRV} current	I_{DRV}	V_{IN} = V_{CIN} = 6 V to 60 V	50	-	-	mA
V_{DRV} UVLO threshold, rising	V_{DRV_UVLO}		4	4.25	4.5	V
V_{DRV} UVLO hysteresis	$V_{DRV_UVLO_HYST}$		-	275	-	mV
Input current	IV_{CIN}	Non-switching, V_{FB} > 0.8 V	-	235	325	µA
Shutdown current	IV_{CIN_SHDN}	V_{EN} = 0 V	-	4	8	
Controller and Timing						
Feedback voltage	V_{FB}	T_J = 25 °C	796	800	804	m/V
		T_J = -40 °C to +125 °C [1]	792	800	808	
V_{FB} input bias current	I_{FB}		-	2	-	nA
Transconductance	g_m		-	0.3	-	mS
COMP source current	I_{COMP_SOURCE}		15	20	-	µA
COMP sink current	I_{COMP_SINK}		15	20	-	
Minimum on-time	$t_{ON_MIN.}$		-	90	110	ns
t_{ON} accuracy	$t_{ON_ACCURACY}$		-10	-	10	%
On-time range	t_{ON_RANGE}		110	-	8000	ns
Frequency range	f_{sw}	Ultrasonic mode enabled	20	-	2000	kHz
		Ultrasonic mode disabled	-	-	2000	
Minimum off-time	$t_{OFF_MIN.}$		190	250	310	ns
Soft start current	I_{SS}		3	5	7	µA
Soft start voltage	V_{SS}	When V_{OUT} reaches regulation	-	1.5	-	V

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ELECTRICAL SPECIFICATIONS (V_{IN} = V_{CIN} = 48 V, T_J = -40 °C to +125 °C, unless otherwise stated)						
PARAMETER	**SYMBOL**	**TEST CONDITIONS**	**MIN.**	**TYP.**	**MAX.**	**UNIT**
Power MOSFETs						
High side on resistance	R_{ON_HS}	SiC461 (10 A), V_{DRV} = 5.3 V, T_A = 25 °C	-	14	-	mΩ
Low side on resistance	R_{ON_LS}		-	6.5	-	
High side on resistance	R_{ON_HS}	SiC462 (6 A), V_{DRV} = 5.3 V, T_A = 25 °C	-	25	-	
Low side on resistance	R_{ON_LS}		-	11	-	
High side on resistance	R_{ON_HS}	SiC463 (4 A), V_{DRV} = 5.3 V, T_A = 25 °C	-	35	-	
Low side on resistance	R_{ON_LS}		-	25	-	
High side on resistance	R_{ON_HS}	SiC464 (2 A), V_{DRV} = 5.3 V, T_A = 25 °C	-	40	-	
Low side on resistance	R_{ON_LS}		-	30	-	
Fault Protections						
Valley current limit	I_{OCP}	SiC461 (10 A), R_{ILIM} = 60 kΩ, T_J = -10 °C to +125 °C	10.4	13	15.6	A
		SiC462 (6 A), R_{ILIM} = 60 kΩ, T_J = -10 °C to +125 °C	6.4	8	9.6	
		SiC463 (4 A), R_{ILIM} = 40 kΩ, T_J = -10 °C to +125 °C	4.8	6	7.2	
		SiC464 (2 A), R_{ILIM} = 60 kΩ, T_J = -10 °C to +125 °C	3.2	4	4.8	
Output OVP threshold	OVP	V_{FB} with respect to 0.8 V reference	-	20	-	%
Output UVP threshold	UVP		-	-80	-	
Over temperature protection	OTP_R	Rising temperature	-	150	-	°C
	OTP_{HYST}	Hysteresis	-	35	-	
Power Good						
Power good output threshold	$V_{FB_RISING_VTH_OV}$	V_{FB} rising above 0.8 V reference	-	20	-	%
	$V_{FB_FALLING_VTH_UV}$	V_{FB} falling below 0.8 V reference	-	-10	-	
Power good hysteresis	P_{GOOD_HYST}		-	50	-	mV
Power good on resistance	R_{ON_PGOOD}		-	7.5	15	Ω
Power good delay time	t_{DLY_PGOOD}		15	25	35	µs
EN / MODE / Ultrasonic Threshold						
EN logic high level	V_{EN_H}		1.4	-	-	V
EN logic low level	V_{EN_L}		-	-	0.4	
EN pull down resistance	R_{EN}		-	5	-	MΩ
Ultrasonic mode high Level	U_{HIGH}		2	-	-	V
Ultrasonic mode low level	U_{LOW}		-	-	0.8	
Mode pull up current	I_{MODE}		3.75	5	6.25	µA
Mode 1		Power save mode enabled, V_{DD}, V_{DRV} Pre-reg on	0	2	100	kΩ
Mode 2		Power save mode disabled, V_{DD}, V_{DRV} Pre-reg on	298	301	304	
Mode 3		Power save mode disabled, V_{DRV} Pre-reg off, V_{DD} Pre-reg on, provide external V_{DRV}	494	499	504	
Mode 4		Power save mode enabled, V_{DRV} Pre-reg off, V_{DD} Pre-reg on, provide external V_{DRV}	900	1000	1100	

Note

(1) Guaranteed by design

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FUNCTIONAL BLOCK DIAGRAM

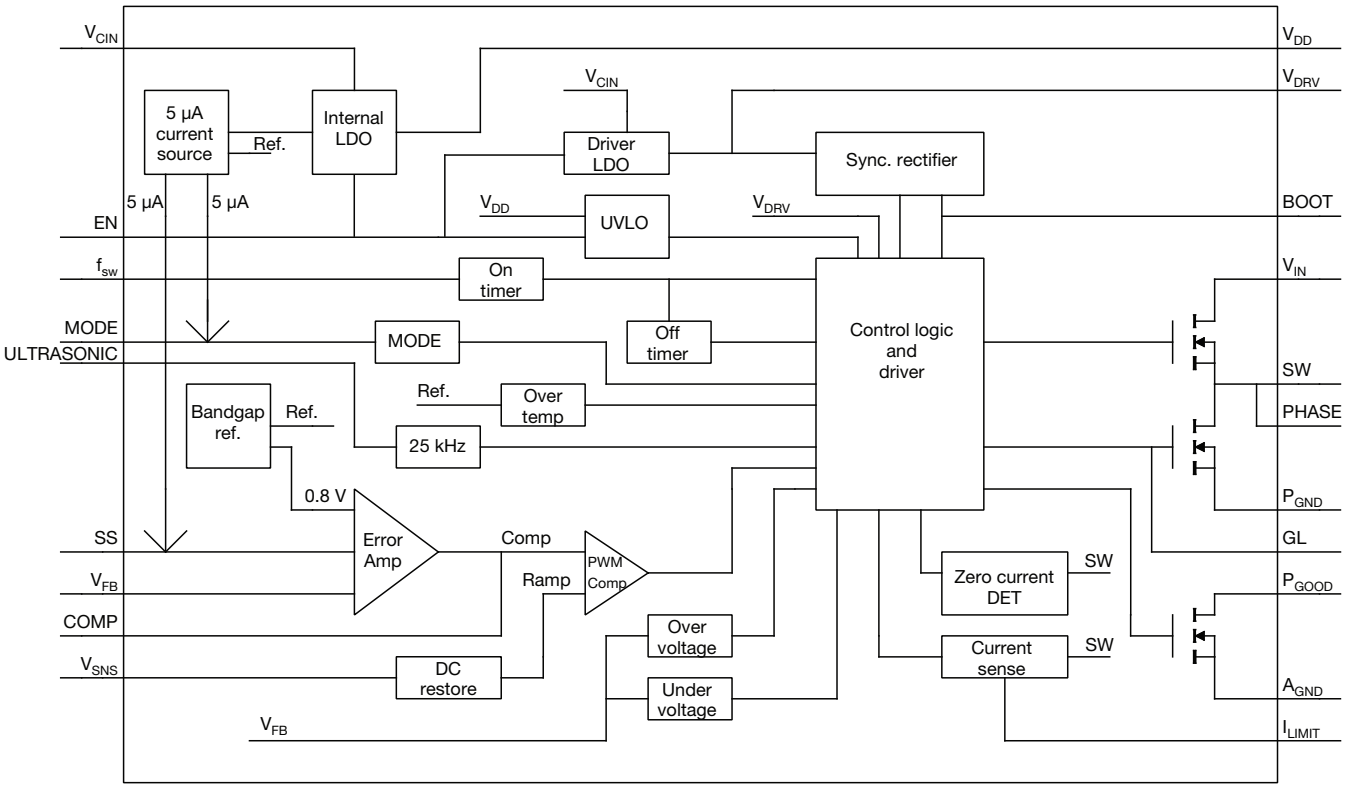

Fig. 4 - SiC46x Functional Block Diagram

OPERATIONAL DESCRIPTION

Device Overview

SiC46x is a high efficiency synchronous buck regulator family capable of delivering up to 10 A continuous current. The device has programmable switching frequency of 100 kHz to 2 MHz. The control scheme is based on voltage mode constant on time. It delivers fast transient response and minimizes external components. It also enables loop stability regardless of the type of output capacitor used, including low ESR ceramic capacitors. This device also incorporates a power saving feature by enabling diode emulation mode and frequency fold back as the load decreases.

SiC46x has a full set of protection and monitoring features:

- Over current protection in pulse-by-pulse mode
- Output overvoltage protection
- Output undervoltage protection with device latch
- Over temperature protection with hysteresis
- Dedicated enable pin for easy power sequencing
- Power good open drain output
- This device is available in MLP55-27L package to deliver high power density and minimize PCB area

Power Stage

SiC46x integrates a high performance power stage with a n-channel high side MOSFET and a n-channel low side MOSFET optimized to achieve up to 98 % efficiency.
The power input voltage (V_{IN}) can go up to 60 V and down as low as 4.5 V for power conversion.

Control Scheme

SiC46x employs a voltage - mode COT control mechanism in conjunction with adaptive zero current detection which allows for power saving in discontinuous conduction mode (DCM). The switching frequency, f_{SW}, is set by an external resistor to A_{GND}, R_{fsw}. The SiC46x operates between 200 kHz to 2 MHz depending on V_{IN} and V_{OUT} conditions.

$$R_{fsw} = \frac{V_{OUT}}{f_{sw} \times 190 \times 10^{-12}}$$

Note, that there is no V_{IN} dependency on f_{SW} as the ON-time adjusts as V_{IN} is varied as long as V_{IN} and V_{CIN} are connected to the same supply. If V_{CIN} uses a different supply from V_{IN}, then the formula is: (see separate formula) In this case, the on time (and hence, switching frequency) will vary with V_{IN}. During steady-state operation, V_{COMP} is generated from the feedback voltage and internal 0.8 V reference inputs to the error amplifier. An externally generated ramp signal and V_{COMP} are fed into a comparator. Once V_{RAMP} crosses V_{COMP}, a single shot ON-time pulse is generated for a fixed time, programmed by the external R_{fsw}.

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During the ON-time pulse, the high side MOSFET will be turned ON. Once the ON-time pulse expires, the high side MOSFET is turned off and the low side MOSFET will be turned ON after a break-before-make period. The low side MOSFET will be on for duration of OFF-time pulse until V_{RAMP} crosses V_{COMP}. The cycle is then repeated.

Fig. 6 illustrates the basic block diagram for voltage mode constant on time architecture with external ripple injection while Fig. 5 illustrates the basic operational principle.

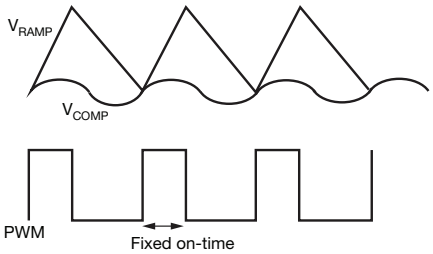

Fig. 5 - SiC46x Operational Principle

The need for ripple injection in this architecture is explained further below. First, let us understand the basic principles of this control architecture:

- The reference of a basic voltage mode COT regulator is replaced with a high gain error amplifier loop. This loop ensures the DC component of the output voltage follows the internal accurate reference voltage provides excellent regulation
- A second voltage feedback path via the V_{SNS} with a ripple injection scheme ensures rapid correction of the transient perturbation
- This establishes two voltage loops, one is the steady state voltage feedback path (via the FB pin) and the other is the feed forward path (via the V_{SNS} pin). This gives the user the best of both worlds; the fast transient response of a COT regulator, and the stable (jitter free), excellent line and load regulation performance of a PWM controller

Choosing the Ripple Injection Component Values

For stability purposes the SiC46x requires adequate ripple injection amplitude. Adequate ripple amplitude is required for two main reasons:

1. To reduce jitter due to noise coupled into the system
2. To provide stable operation Sub harmonic oscillation can occur with constant on time ripple control if below condition is not met

$$R_{ESR} \times C_{OUT} > \frac{t_{ON}}{2}$$

Therefore, when the converter design uses an all ceramic output capacitor or other low ESR output capacitors, instability can occur. In order to avoid this, a ripple injection network is used to increase the equivalent R_{ESR} in order to satisfy the above condition. The ripple injection amplitude must be large enough to avoid instability or noise sensitivity but not too large that it degrades transient performance. To ensure stable operation under CCM, DCM and ultrasonic mode, minimum ripple amplitude of 100 mV is recommended for the SiC46x family of regulators. A maximum ripple of 900 mV is recommended so as not to degrade transient response.

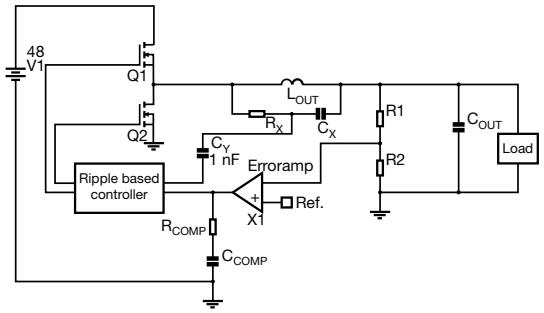

Fig. 6 - SiC46x Control Block Diagram

Ripple amplitude is a function of frequency, V_{IN}, and V_{OUT}. The formula for V_{RIPPLE} amplitude is:

Equation 1

$$V_{RIPPLE} = \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{(V_{IN} \times f_{sw} \times C_x \times R_x)}$$

where f_{sw} is the switching frequency.

From the above equation for V_{RIPPLE} it is clear that the ripple amplitude is a function of V_{IN}, V_{OUT}, and switching frequency and should be adjusted whenever V_{IN}, V_{OUT}, or switching frequency is changed.

For a given buck regulator design, V_{OUT}, and switching frequency is typically fixed, while the converter may be expected to work for a wide V_{IN} range. The ripple injection amplitude will increase as V_{IN} is increased and increase the power dissipated by R_x. In order to limit the power dissipated in R_x the value of R_x should be chosen such that maximum power dissipated is under < 25 mW to safely allow the use of a 0603 resistor even at high ambient temperatures and maximum input voltage condition.

In order to optimize the ripple voltage over a desired V_{IN} range use the following procedure to calculate R_x, C_x, and C_y.

1. First calculate R_x using equation 2 below. This equation calculates a value of R_x that limits power dissipation in R_x
   Equation 2
   $$V_{RIPPLE} = \frac{V_{INMAX.} \times V_{OUT} \times (1 - D)}{R_{x_PD_MAX.}}$$
   where $R_{x_PD_MAX.}$ = 0.025 W is the maximum allowed dissipation in R_x at maximum V_{IN}
2. Determine the $C_{x_min.}$ value based on equation (3) while using the maximum V_{IN} and maximum allowed ripple of 900 mV.
   Equation 3
   $$C_{x_MAX.} = \frac{R_{x_PD_MAX.}}{V_{IN} \times f_{sw} \times V_{RIPPLE}}$$
   where $R_{x_PD_MAX.}$ = 0.025 W, V_{RIPPLE} = 900 mV
3. Use the V_{RIPPLE} equation 1, and calculate the $V_{RIPPLE_MIN.}$ at minimum V_{IN} based on the R_x and the minimum C_x value calculated above

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4. If the $V_{RIPPLE_MIN.}$ is less than 200 mV, set C_x to C_x_MIN., otherwise set C_x to ($C_{x_MIN.}$ x $V_{RIPPLE_MIN.}$/200 mV)

This procedure allows for a maximum range of operation for the converter. In order to simplify the procedure for calculating ripple injection components along with compensation components, a calculator is provided (visit www.vishay.com/doc?75760).

Error Amplifier Compensation Value Selection

R_{COMP} and C_{COMP} in the Fig. 6 are the components used to compensate the control loop.

For optimal transient response, the crossover frequency should be:

- Set typically at 1/10th to 1/5th of the converter switching frequency (Vishay's component calculator tool uses 1/10th the converter switching frequency)
- Be above the LC filter resonance frequency which is 1/2 $\pi\sqrt{LC}$

The procedure to select the R_{COMP} and C_{COMP} such that the above conditions are met is as follows:

1. Plot the magnitude and phase of the control to output transfer function using equation 4 below.
   Control to output transfer function (equation 4).

$$H(s) = A \times \frac{1 + sR_C C_o \times (1 + sR_x C_x) \times (1 + sR_y C_y)}{\left(1 + \frac{sL}{R_o} + s^2 LC_o\right) \times (1 + sR_x C_x) \times (1 + sR_y C_y) + AR_y C_y s \times \left[1 + s \times \left(R_x C_x + \frac{L}{R_o}\right) + s^2 \times (R_x R_c C_x C_o + LC_o)\right]}$$

   Where A = ($2V_{IN}$ x R_x x C_x x f)/V_{OUT}, R_x, C_x, C_y are components for ripple injection as shown in Fig. 6 and R_y is the internal impedance of the V_{SNS} pin and is = 65 kΩ.
   C_o - output capacitance
   R_c - output capacitor ESR
2. From the plot of the control to output transfer function, determine the gain and phase at the crossover frequency
3. Calculate the R_{COMP} using the equation

$$R_{COMP} = \frac{1}{G_H \times gm \times r_{FB}}$$

   where G_H is the gain of the transfer function at cross over frequency, "gm" is the transconductance of the error amplifier (300 μs) and r_{FB} is the ratio of the feedback divider
4. Select C_{COMP}based on the placement of the zero such that phase margin is sufficient at the cross over frequency. A phase margin of over 60° is sufficient for converter stability. A good starting point is to place the compensation zero at 1/5th of the LC pole

$$C_{COMP} = \frac{5\sqrt{LC}}{R_{COMP}}$$

Once the component values are calculated, it is now possible to calculate the total loop gain. The total loop gain is the product of the control to output transfer function and the error amplifier transfer function.

The transfer function of the error amplifier is given by equation 5 below.

$$G(s) = gmR_o \times \frac{(1 + sR_{COMP}C_{COMP})}{(1 + s \times (R_{COMP}C_{COMP} + R_o C_{COMP}))}$$

Where R_o = 40 MΩ is the output resistance of the transconductance amplifier.
Total loop gain = H(s)G(s)

As this procedure could be complicated an automated calculator (visit www.vishay.com/doc?75760) is provided to assist the user to determine ripple injection components as well as error amplifier compensation components using user selected operating conditions.

Power-Save Mode, Mode Pin, and Ultrasonic Pin Operation

To improve efficiency at light-loads, SiC46x provides a set of innovative implementations to eliminate LS re-circulating current and switching losses. The internal zero crossing detector (ZCD) monitors SW node voltage to determine when inductor current starts to flow negatively. In power saving mode, as soon as inductor valley current crosses zero, the device first deploys diode emulation mode by turning off the LS FET. If load further decreases, switching frequency is reduced proportional to the load condition to save switching losses while keeping output ripple within tolerance. If the ultrasonic pin is tied to V_{DD}, the minimum switching frequency in the discontinuous mode is 25 kHz to avoid switching frequencies in the audible range. If this feature is not required this ultrasonic mode can be disabled by floating the ultrasonic pin. When the ultrasonic mode is disabled, the regulator will either operate in forced continuous mode or in a power save mode where there is no limit to the lower frequency limit. In this state, at zero load switching frequency can go as low as hundreds of Hz.

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To improve the converter efficiency, the user can choose to disable the internal V_{DRV} regulator by picking either mode 3 or mode 4 and connecting a 5 V supply to the V_{DRV} pin. This reduces power dissipation in the SiC46x by eliminating the V_{DRV} linear regulator losses.

The mode pin supports several modes of operation as shown in table 1. An internal current source is used to set the voltage on this pin using an external resistor:

TABLE 1 - OPERATION MODES

MODE	RANGE (kΩ)	POWER SAVE MODE	INTERNAL V_{DRV} REGULATOR
1	0 to 100	Enabled	ON
2	298 to 304	Disabled	ON
3	494 to 504	Disabled	OFF [1]
4	900 to 1100	Enabled	OFF [1]

Note

[1] Connect a 5 V (± 5 %) supply to the V_{DRV} pin

The mode pin is not latched to any state and can be changed on the fly.

OUTPUT MONITORING AND PROTECTION FEATURES

Output Over-Current Protection (OCP)

SiC46x has cycle by cycle current limiting. The inductor valley current is monitored during LS FET turn-on period through $R_{DS(on)}$ sensing. After a pre-defined blanking time, the valley current is compared with an internal threshold. If monitored current is higher than threshold, HS turn-on pulse is skipped and LS FET is kept on until the valley current returns below OCP limit.

In a short circuit or a severe over-current condition, output undervoltage protection (UVP) will result in both the HS and LS FET turning off. See output undervoltage protection (UVP) section for more details.

OCP is enabled immediately after V_{DD} passes UVLO level.

OCP is set by an external resistor R_{LIM} to A_{GND}. (See table 2)

$$R_{LIM} = 480K/I_{OUT\ max.}$$

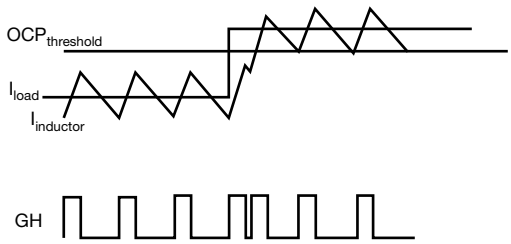

Fig. 7 - Over-Current Protection Illustration

Output Undervoltage Protection (UVP)

UVP is implemented by monitoring output through V_{FB} pin. If the voltage level at V_{FB} goes below 0.16 V (V_{OUT} is 20 % of V_{OUT} set point) for more than 25 µs a UVP event is recognized and both HS and LS MOSFETs are turned off. After a time-out period equal to 20 soft start cycles, the IC attempts to re-start by going through a soft start cycle. If the fault condition still exists, the above cycle will be repeated.

UVP is only active after the completion of soft-start sequence.

Output Over Voltage Protection (OVP)

For OVP implementation, output is monitored through FB pin. After soft start, if the voltage level at FB is above 0.96 V (typ.) (V_{OUT} is 120 % of V_{OUT} set point), OVP is triggered with both the HS and LS MOSFETs turned off. Normal operation is resumed once FB voltage drops back to 0.96 V.
OVP is active immediately after V_{DD} passes UVLO level.

Over Temperature Protection (OTP)

SiC46x has internal thermal monitor block that turns off both HS and LS FETs when junction temperature is above 150 °C (typ). A hysteresis of 35 °C is implemented, so when junction temperature drops below 115 °C, the device restarts by initiating soft-start sequence again.

Sequencing of Input / Output Supplies

SiC46x has no sequencing requirements on any of its input / output (V_{IN}, V_{DRV}, V_{DD}, V_{CIN}, EN) supplies or enables.

Enable

The SiC46x has an enable pin to turn the part on and off. Driving this pin high enables the device, while grounding it turns it off.

The SiC46x enable has a weak pull down to prevent unwanted turn on due to a floating GPIO.

There are no sequencing requirements with respect to other input / output supplies.

Soft-Start

During soft start time period, inrush current is limited and the output voltage is ramped gradually. The following control scheme is implemented:
Once the V_{DD} voltage reaches the UVLO trip point, an internal “Soft start Reference” (SR) begins to ramp up. The SR ramp rate is determined by the external soft start capacitor. There is an internal 5 µA current source tied to the soft start pin which charges the external soft start cap.
The internal SR signal is being used as a reference voltage to the loop error amplifier (see functional block diagram). The control scheme guarantees that the output voltage during the soft start interval will ramp up coincidently with the SR signal. voltage. The speed of the internal soft start ramp can SiC46x soft-start time is adjustable by selecting a capacitor value from the following equation.

$$\text{SS time} = \frac{C_{ext} \times 0.8\ V}{5\ \mu A}$$

During soft-start period, OCP is activated. Short circuit protection is not active until soft-start is complete.

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Pre-Bias Start-Up

In case of pre-bias startup, if the sensed voltage on FB is higher than the internal soft-start ramp value, control logic prevents HS and LS FET from switching to avoid negative output voltage spike and excessive current sinking through LS FET.

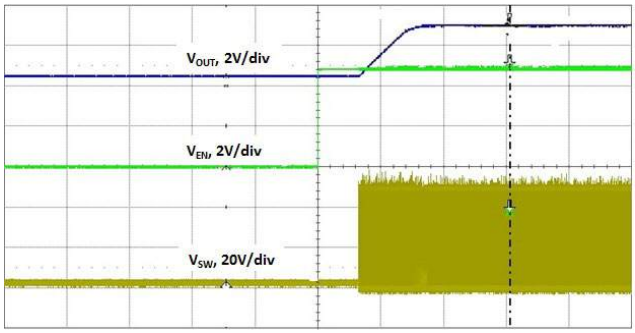

Fig. 8 - Pre-Bias Start-Up

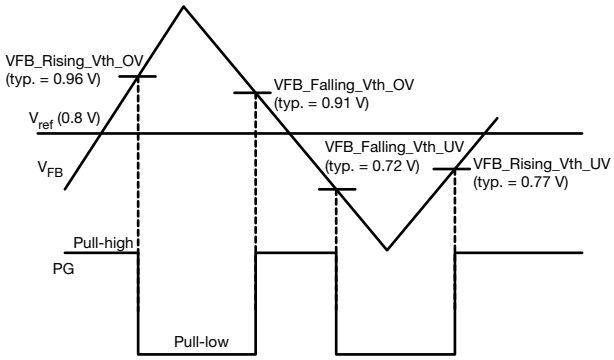

Fig. 9 - P_{GOOD} Window and Timing Diagram

Power Good

SiC46x's power good is an open-drain output. Pull P_{GOOD} pin high up to 5 V through a 10K resistor to use this signal. Power good window is shown in the diagram above. If voltage level on FB pin is out of this window, PG signal is de-asserted by pulling down to GND. To prevent false triggering during transient events, P_{GOOD} has a 25 µs

EXAMPLE SCHEMATIC OF SiC462

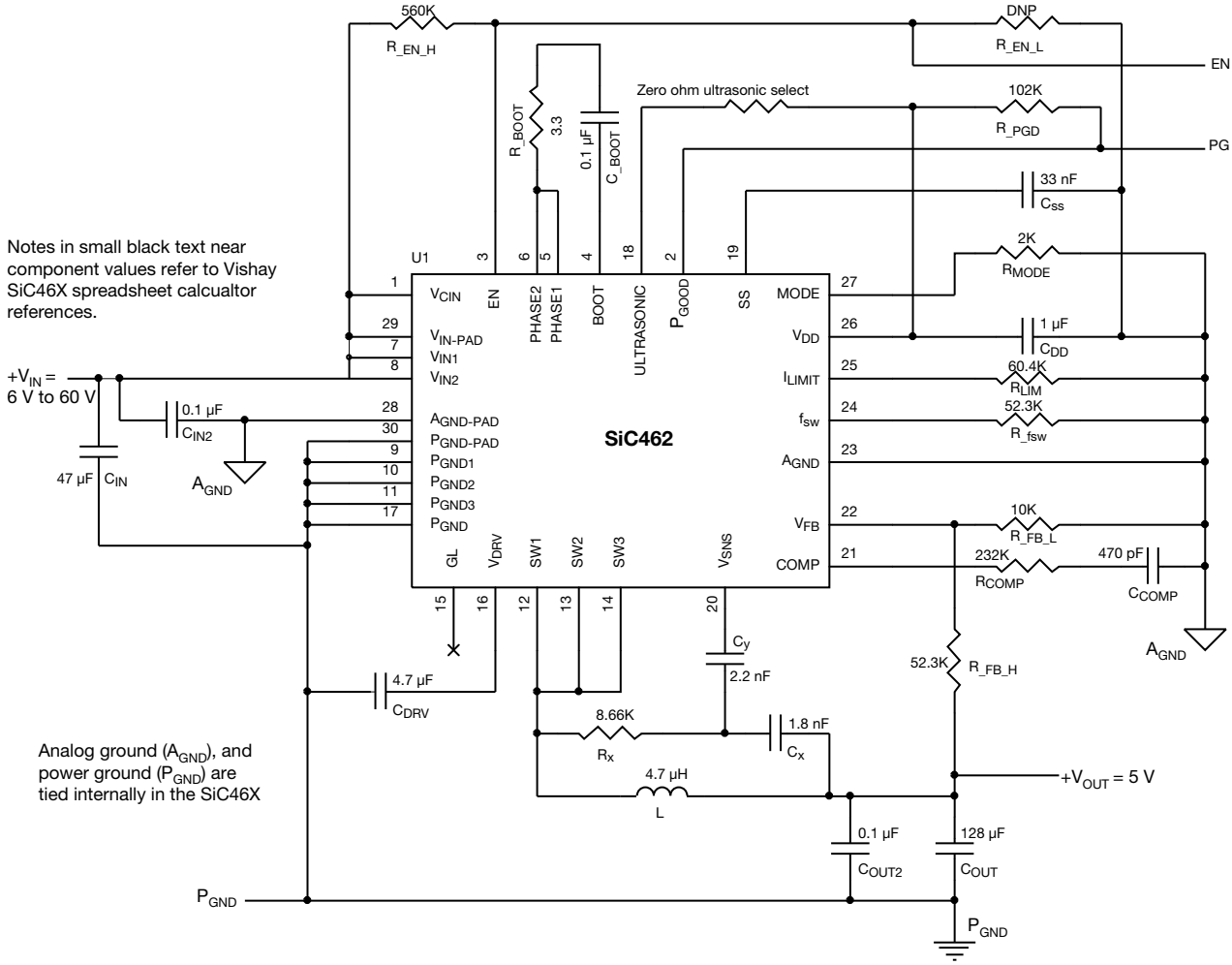

Fig. 10 - SiC462 Configured for 6 V to 60 V Input, 5 V Output at 6 A, 500 kHz Operation with Ultrasonic Power Save Mode Enabled all Ceramic Output Capacitance Design

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EXTERNAL COMPONENT SELECTION FOR THE SiC46x

This section explains external component selection for the SiC46x family of regulators. Component reference designators in any equation refer to the schematic shown in Fig. 10.

An excel based calculator is available on the website to make external component calculation simple. The user simply needs to enter required operating conditions.

Output Voltage Adjustment

If a different output voltage is needed, simply change the value of V_{OUT} and solve for $R_{_FB_H}$ based on the following formula:

$$R_{_FB_H} = \frac{R_{_FB_L}(V_{OUT} - V_{FB})}{V_{FB}}$$

Where V_{FB} is 0.8 V for the SiC46x. $R_{_FB_L}$ (R_{13}) should be a maximum of 10 kΩ to prevent V_{OUT} from drifting at no load.

Switching Frequency Selection

The following equation illustrates the relationship between on-time, V_{IN}, V_{OUT}, and R_{fsw} value:

$$R_{_fsw} = \frac{V_{OUT}}{f_{sw} \times 190 \times 10^{-12}}$$

Inductor Selection

The choice of inductor is specific to each application and quickly determined with the following equations:

$$t_{ON} = \frac{V_{OUT}}{V_{IN_max.} \text{ x } f_{sw}}$$

and

$$L = \frac{(V_{IN} - V_{OUT}) \text{ x } t_{ON}}{I_{OUT_MAX.} \text{ x } K}$$

Where K is a percentage of maximum output current ripple required. The designer can quickly make a choice of inductor if the ripple percentage is decided, usually no more than 30 % however higher or lower percentages of I_{OUT} can be acceptable depending on application. This device allows choices larger than 30 %.

Other than the inductance the DCR and saturation current parameters are key values. The DCR causes an I^2R loss which will decrease the system efficiency and generate heat. The saturation current has to be higher than the maximum output current plus ½ of the ripple current. In an over current condition the inductor current may be very high. All this needs to be considered when selecting the inductor.

Output Capacitor Selection

The SiC46x is stable with any type of output capacitors by choosing the appropriate ripple injection components. This allows the user to choose the output capacitance based on the best trade off of board space, cost and application requirements.

The output capacitance will be determined by the ripple voltage requirement. Voltage mode COT topology can work with very small values of capacitor ESR.

The following equations are used to calculate the size needed to meet a transient load response:

$$I_{LPK} = I_{max.} + 0.5 \text{ x } I_{RIPPLE_max.}$$

and

$$C_{OUT_min.} = I_{LPK} \text{ x } \frac{L \text{ x } \frac{I_{LPK}^2}{V_{OUT}} - \frac{I_{max}^2 \text{ x dt}}{dI_{LOAD}}}{2 \text{ x } (V_{PK} - V_{OUT})}$$

Where I_{LPK} is the peak inductor current, $I_{MAX.}$ is the maximum output current, dI_{LOAD} is the current step in µs and V_{PK} is the peak voltage, the output voltage summed with the specified over and under shoot.

In case high ESR electrolytic capacitors are used, it is good practice to also include low ESR ceramic capacitors in parallel with the high ESR bulk capacitance to improve output ripple and transient response. A good starting point is to use a 10 µF output capacitor.

Care must be taken to account for voltage derating of the capacitance when choosing an all ceramic output capacitance.

Enable Pin Voltage

The EN pin has an internal pull down resistor and only requires an enable voltage. This needs to be greater than 1.4 V. An input voltage or a resistor connected across V_{IN} and EN can be used. The internal pull down resistance is 5 MΩ.

Current Limit Resistor

The current limit is set by placing a resistor between I_{LIM} and A_{GND}. The values can be found using the following equation:

TABLE 2 - I_{LIMIT} RESISTOR CALCULATION

PART NUMBER	EQUATION
SiC461	R_{LIM} = 780K/I_{OUT} max.
SiC462	R_{LIM} = 480K/I_{OUT} max.
SiC463, SiC464	R_{LIM} = 240K/I_{OUT} max.

Input Capacitance

In order to determine the minimum capacitance the input voltage ripple needs to be specified; $V_{CINPP} \leq 500$ mV is a suitable starting point. This magnitude is determined by the final application specification. The input current needs to be determined for the lowest operating input voltage,

$$I_{CIN(RMS)} = I_O \text{ x } \sqrt{D \text{ x } (1-D) + \frac{1}{12} \times \left(\frac{V_{OUT}}{L \times f_{sw} \times I_{OUT}}\right)^2 \times (1-D)^2 \times D}$$

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The minimum input capacitance can then be found,

$$C_{IN_min.} = I_{OUT} \times \frac{D - (1 - D)}{V_{CINPKPK} \times f_{sw}}$$

If high ESR capacitors are used, it is good practice to also add low ESR ceramic capacitance. A 4.7 µF ceramic input capacitance is a suitable starting point.
Care must be taken to account for voltage derating of the capacitance when choosing an all ceramic input capacitance.

Error Amplifier Compensation and Ripple Injection Values

The compensation of the error amplifier in the SiC46x as well as the ripple injection components need to change based on the required operating conditions. The component selection is discussed in detail in the earlier sections of the datasheet on pages 6 and 7. To simplify the task of calculating these components, an excel based calculator is provided. Visit www.vishay.com/doc?75760)to download the file.

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ELECTRICAL CHARACTERISTICS (V_{IN} = 48 V, V_{OUT} = 5 V, f_{sw} = 300 kHz, SiC461 (10 A), unless otherwise noted)

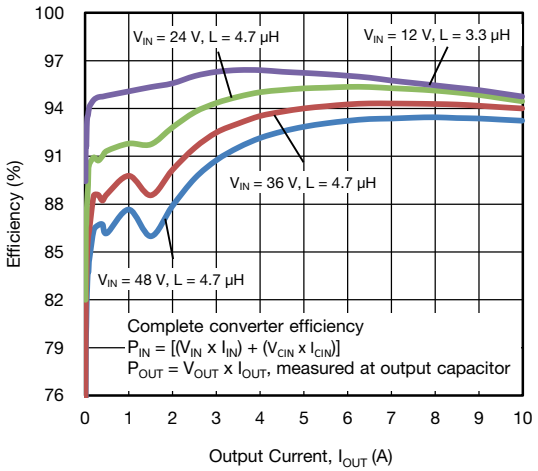

Fig. 11 - SiC461 Efficiency vs. Output Current, V_{OUT} = 5 V

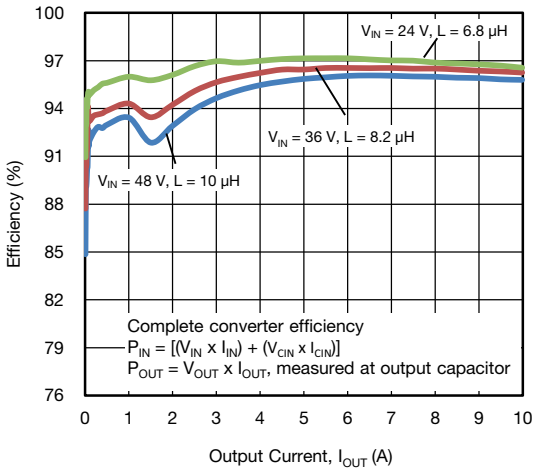

Fig. 12 - SiC461 Efficiency vs. Output Current, V_{OUT} = 12 V

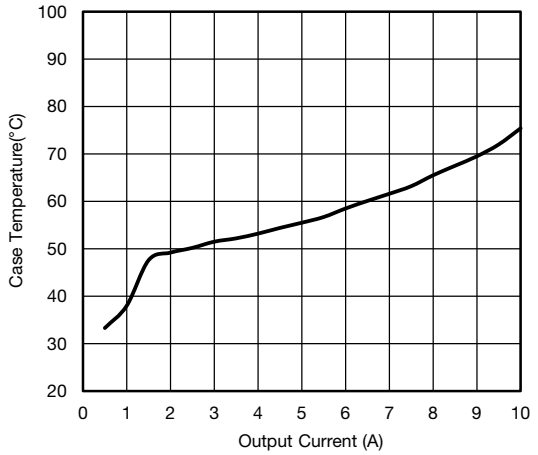

Fig. 13 - SiC461 Load Current vs. Case Temperature, V_{IN} = 48 V, V_{OUT} = 5 V

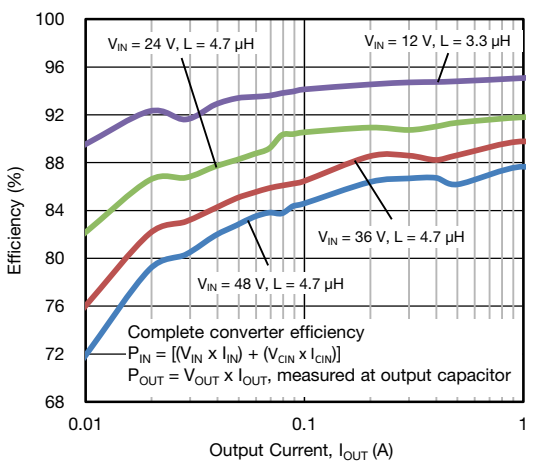

Fig. 14 - SiC461 Efficiency vs. Output Current - Light Load, V_{OUT} = 5 V

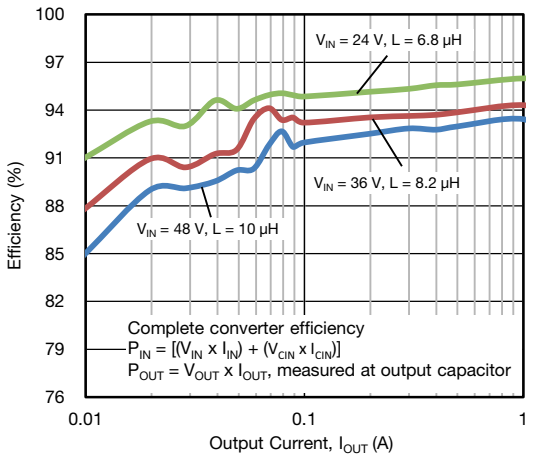

Fig. 15 - SiC461 Efficiency vs. Output Current - Light Load, V_{OUT} = 12 V

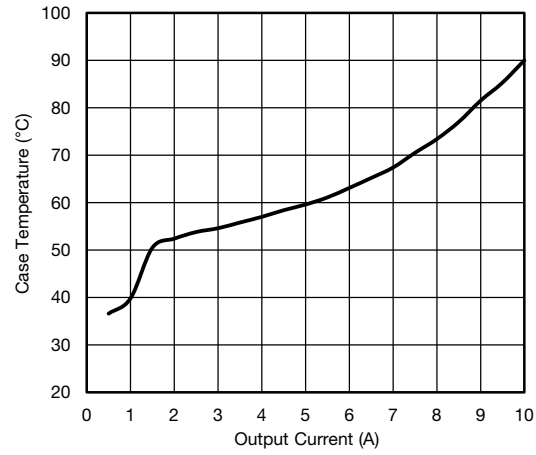

Fig. 16 - SiC461 Load Current vs. Case Temperature, V_{IN} = 48 V, V_{OUT} = 12 V

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ELECTRICAL CHARACTERISTICS (V_{IN} = 48 V, V_{OUT} = 5 V, f_{sw} = 300 kHz, SiC462 (6 A), unless otherwise noted)

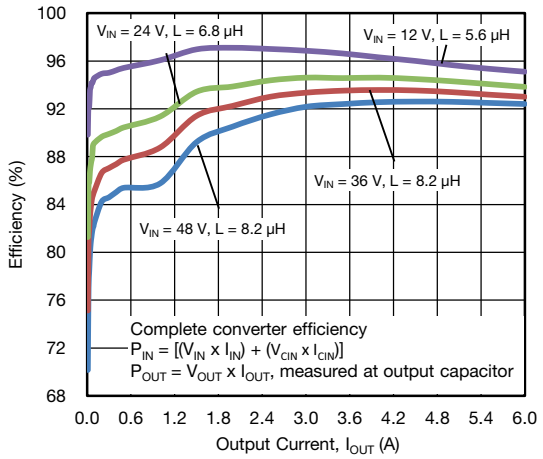

Fig. 17 - SiC462 Efficiency vs. Output Current, V_{OUT} = 5 V

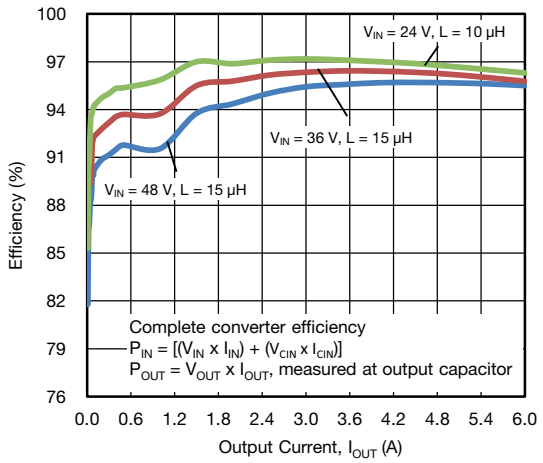

Fig. 18 - SiC462 Efficiency vs. Output Current, V_{OUT} = 12 V

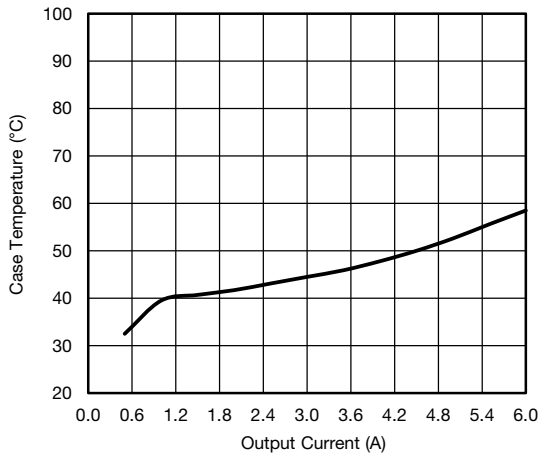

Fig. 19 - SiC462 Load Current vs. Case Temperature, V_{IN} = 48 V, V_{OUT} = 5 V

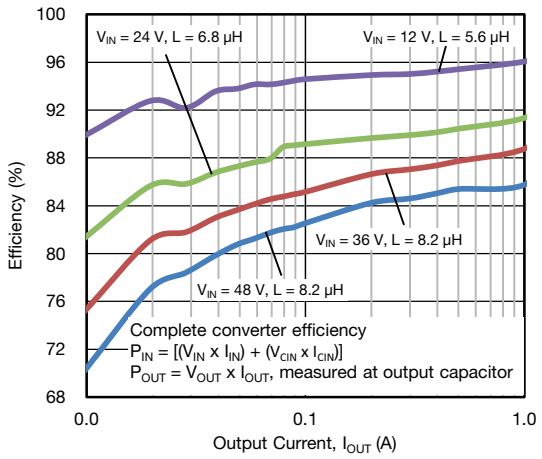

Fig. 20 - SiC462 Efficiency vs. Output Current - Light Load, V_{OUT} = 5 V

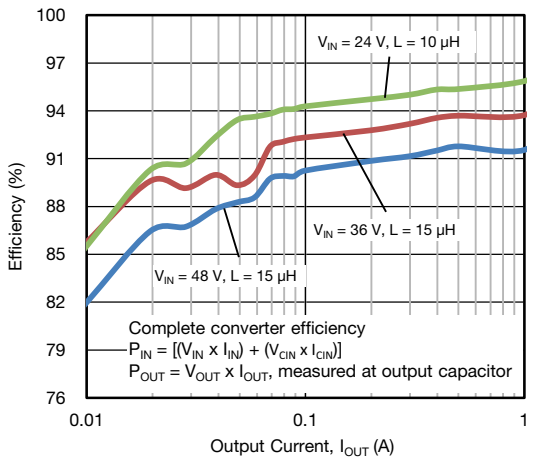

Fig. 21 - SiC462 Efficiency vs. Output Current - Light Load, V_{OUT} = 12 V

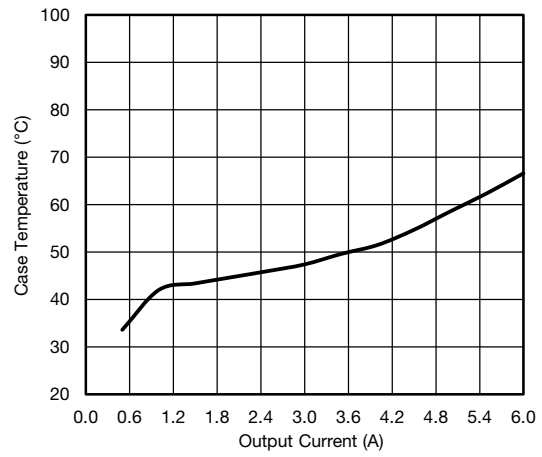

Fig. 22 - SiC462 Load Current vs. Case Temperature, V_{IN} = 48 V, V_{OUT} = 12 V

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ELECTRICAL CHARACTERISTICS (V_{IN} = 48 V, V_{OUT} = 5 V, f_{sw} = 300 kHz, SiC463 (4 A), unless otherwise noted)

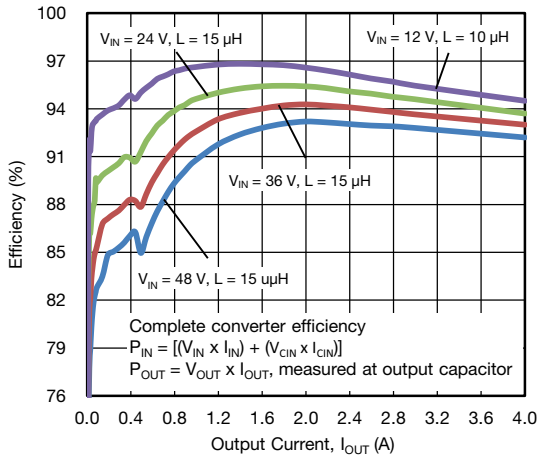

Fig. 23 - SiC463 Efficiency vs. Output Current, V_{OUT} = 5 V

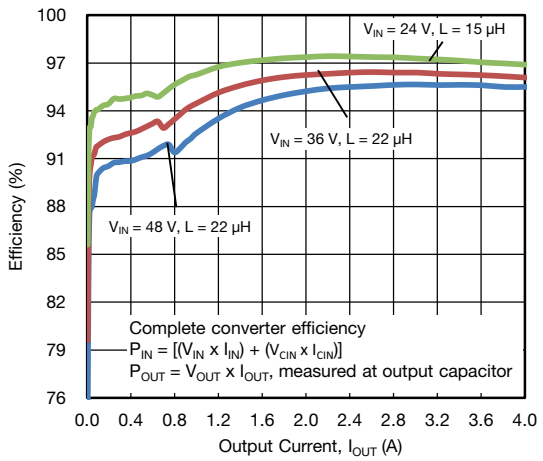

Fig. 24 - SiC463 Efficiency vs. Output Current, V_{OUT} = 12 V

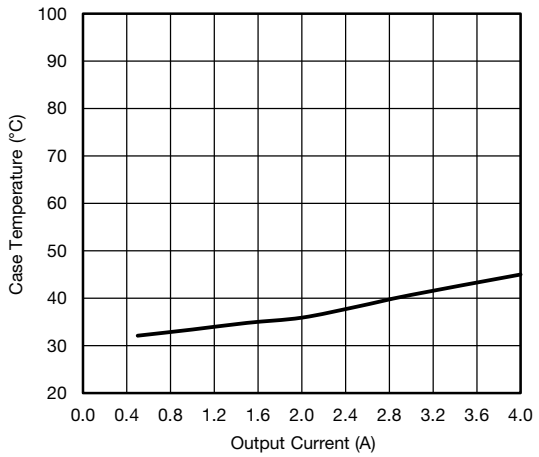

Fig. 25 - SiC463 Load Current vs. Case Temperature, V_{IN} = 48 V, V_{OUT} = 5 V

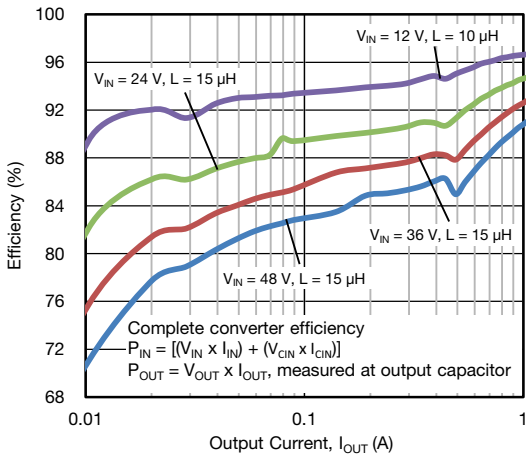

Fig. 26 - SiC463 Efficiency vs. Output Current - Light Load, V_{OUT} = 5 V

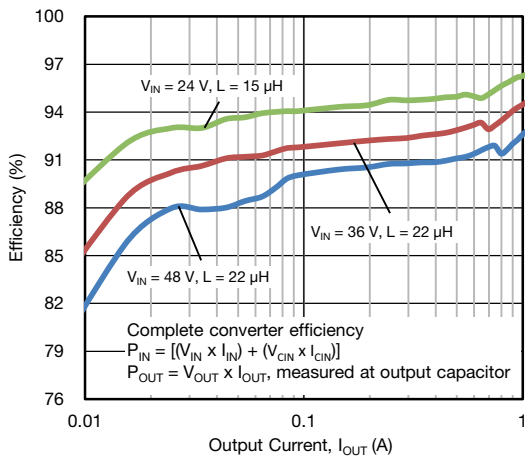

Fig. 27 - SiC463 Efficiency vs. Output Current - Light Load, V_{OUT} = 12 V

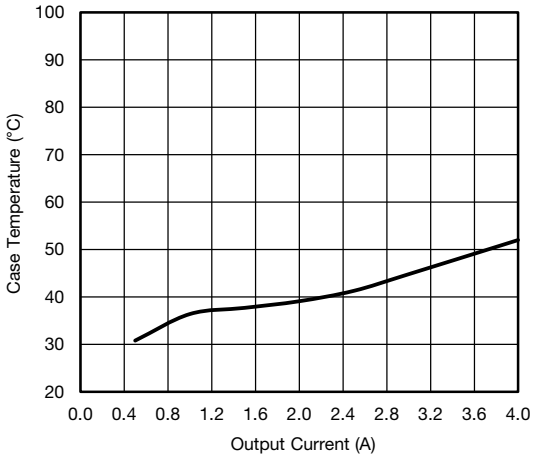

Fig. 28 - SiC463 Load Current vs. Case Temperature, V_{IN} = 48 V, V_{OUT} = 12 V

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ELECTRICAL CHARACTERISTICS (V_{IN} = 48 V, V_{OUT} = 5 V, f_{sw} = 300 kHz, SiC464 (2 A), unless otherwise noted)

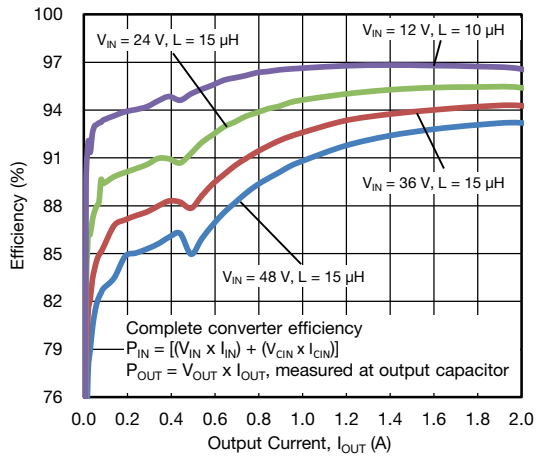

Fig. 29 - SiC464 Efficiency vs. Output Current, V_{OUT} = 5 V

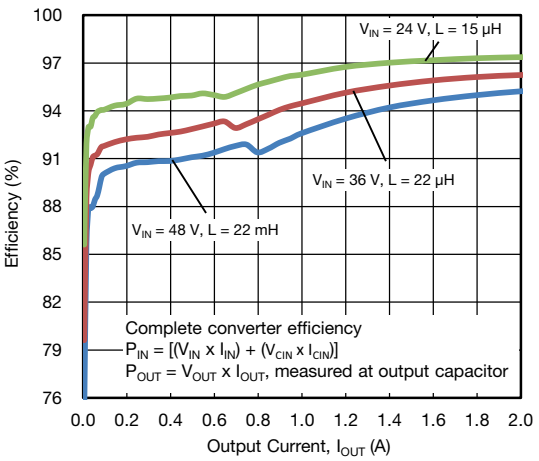

Fig. 30 - SiC464 Efficiency vs. Output Current, V_{OUT} = 12 V

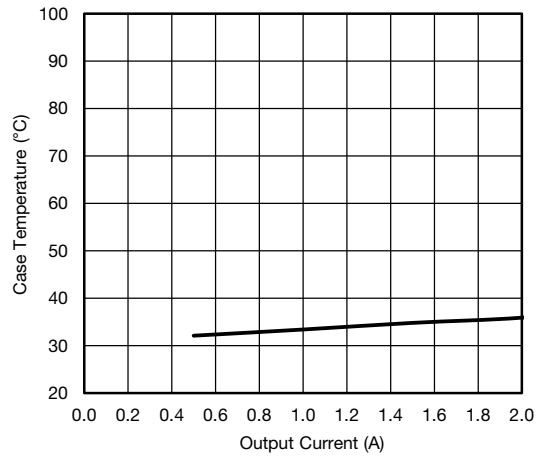

Fig. 31 - SiC464 Load Current vs. Case Temperature, V_{IN} = 48 V, V_{OUT} = 5 V

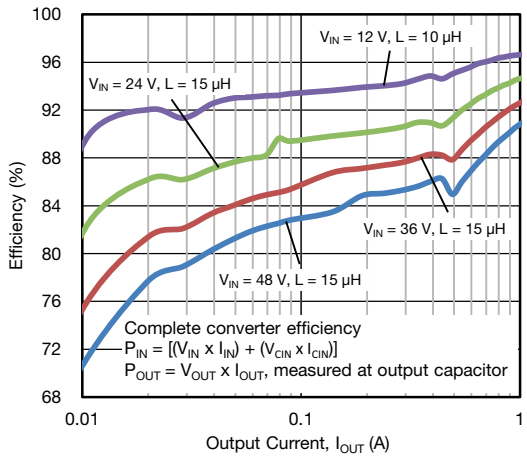

Fig. 32 - SiC464 Efficiency vs. Output Current - Light Load, V_{OUT} = 5 V

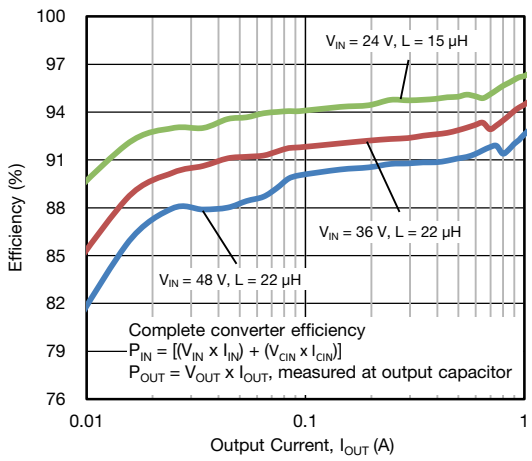

Fig. 33 - SiC464 Efficiency vs. Output Current - Light Load, V_{OUT} = 12 V

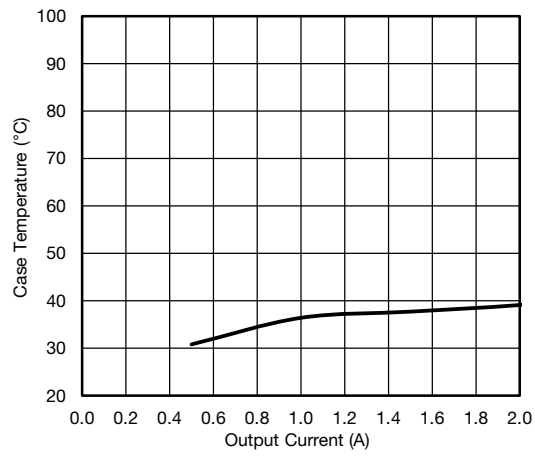

Fig. 34 - SiC464 Load Current vs. Case Temperature, V_{IN} = 48 V, V_{OUT} = 12 V

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ELECTRICAL CHARACTERISTICS (V_{IN} = 48 V, V_{OUT} = 5 V, f_{sw} = 300 kHz, SiC462 (6 A), unless otherwise noted)

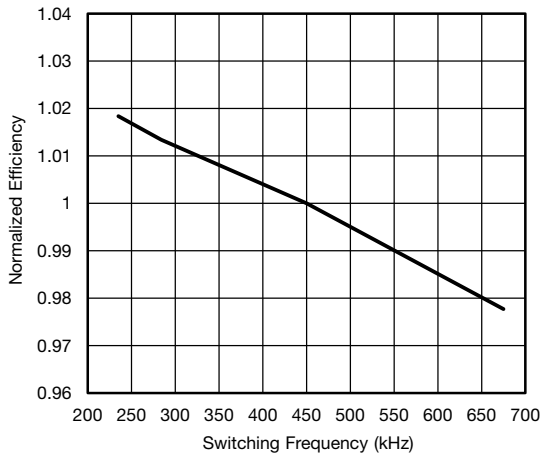

Fig. 35 - SiC461 Efficiency vs. Switching Frequency

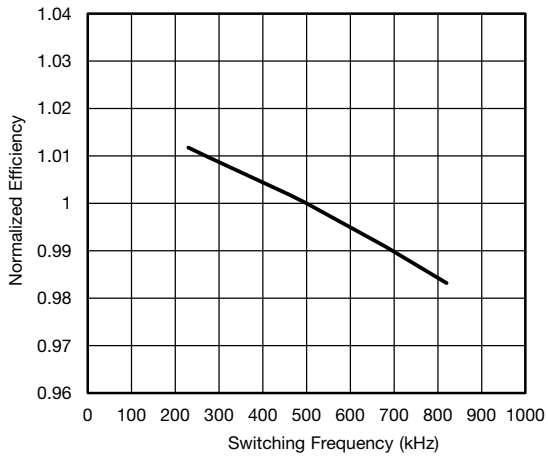

Fig. 36 - SiC463 Efficiency vs. Switching Frequency

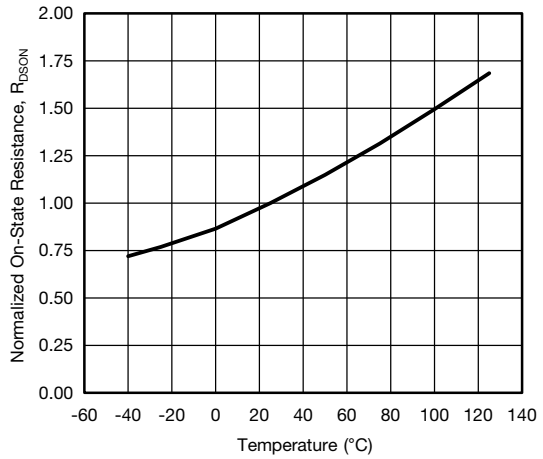

Fig. 37 - $R_{DS(ON)}$ vs. Temperature

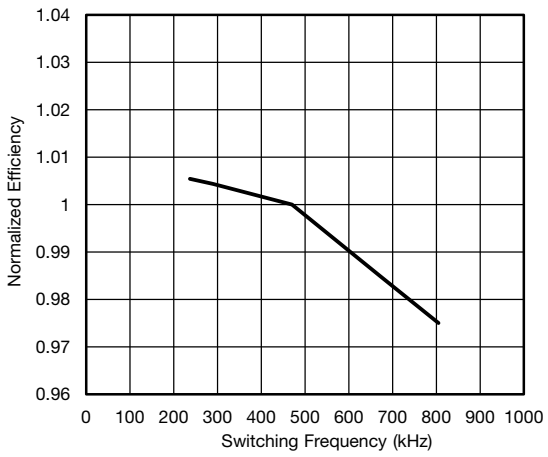

Fig. 38 - SiC462 Efficiency vs. Switching Frequency

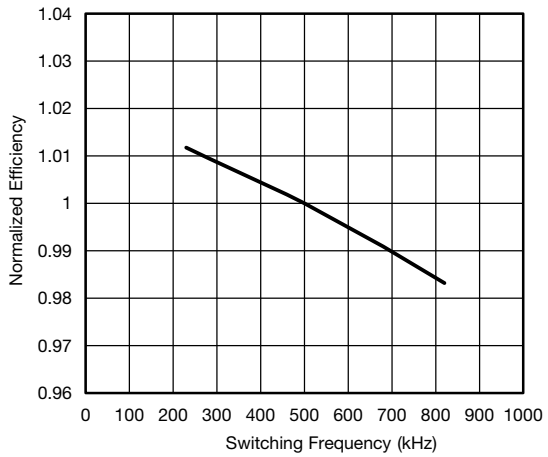

Fig. 39 - SiC464 Efficiency vs. Switching Frequency

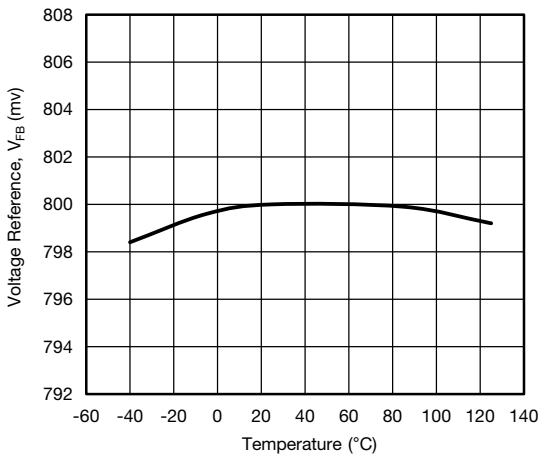

Fig. 40 - Voltage Reference vs. Temperature

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ELECTRICAL CHARACTERISTICS (V_{IN} = 48 V, V_{OUT} = 5 V, f_{sw} = 300 kHz, SiC462 (6 A), unless otherwise noted)

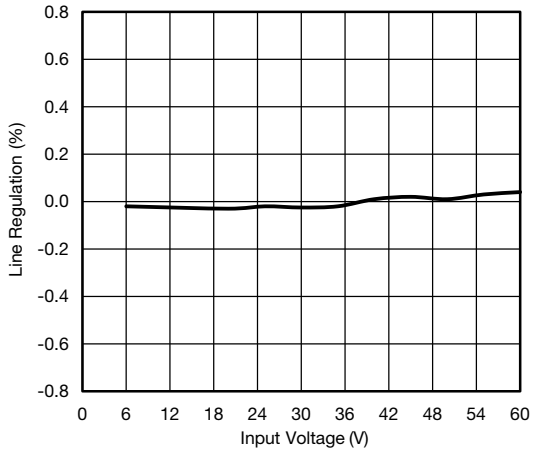

Fig. 41 - Line Regulation

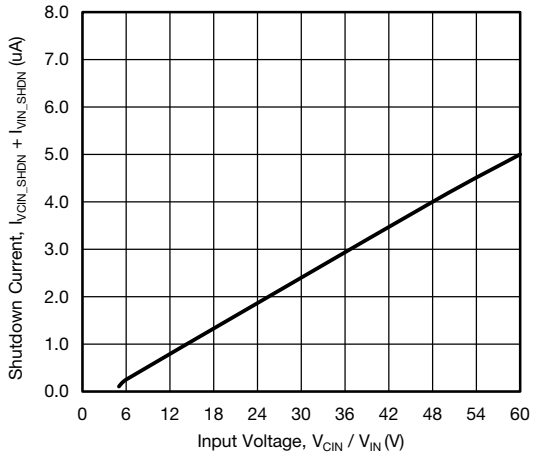

Fig. 42 - Shutdown Current vs. Input Voltage

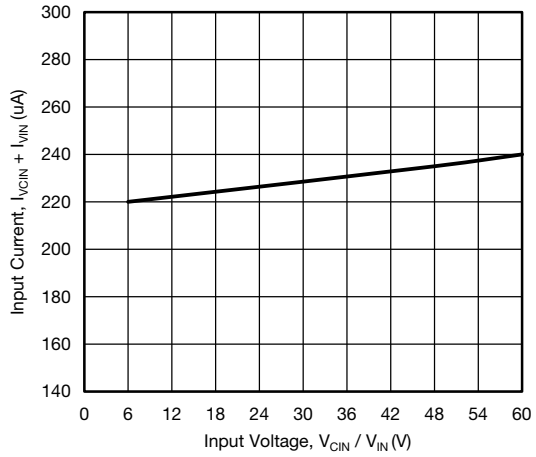

Fig. 43 - Input Current vs. Input Voltage

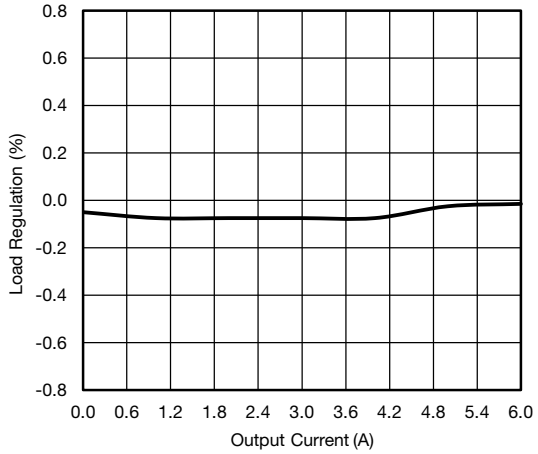

Fig. 44 - Load Regulation

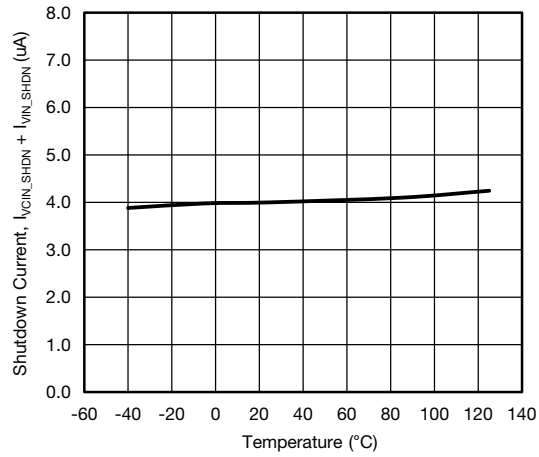

Fig. 45 - Shutdown Current vs. Junction Temperature

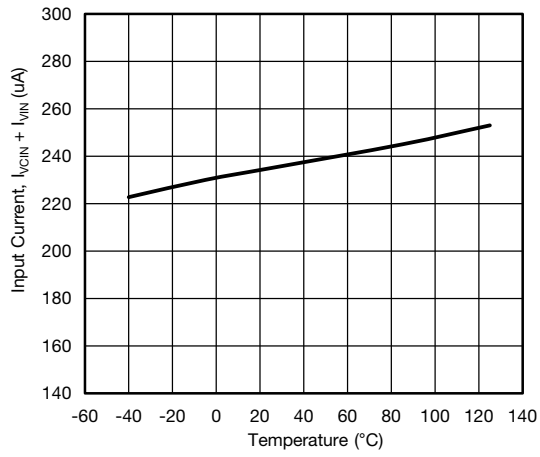

Fig. 46 - Input Current vs. Junction Temperature

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ELECTRICAL CHARACTERISTICS (V_{IN} = 48 V, V_{OUT} = 5 V, f_{sw} = 300 kHz, SiC462 (6 A), unless otherwise noted)

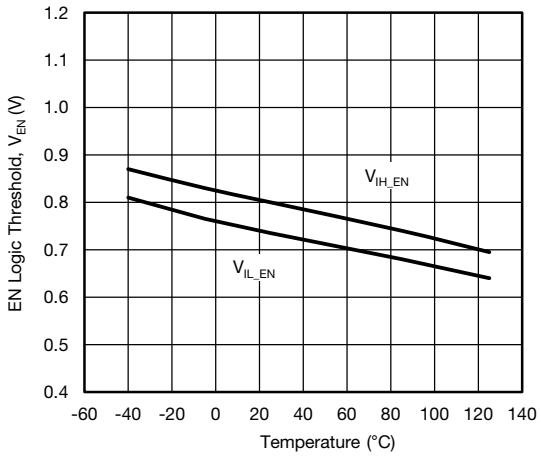

Fig. 47 - EN Logic Threshold vs. Junction Temperature

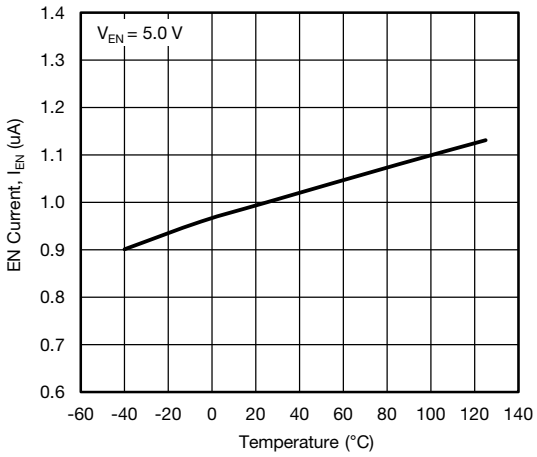

Fig. 50 - EN Current vs. Junction Temperature

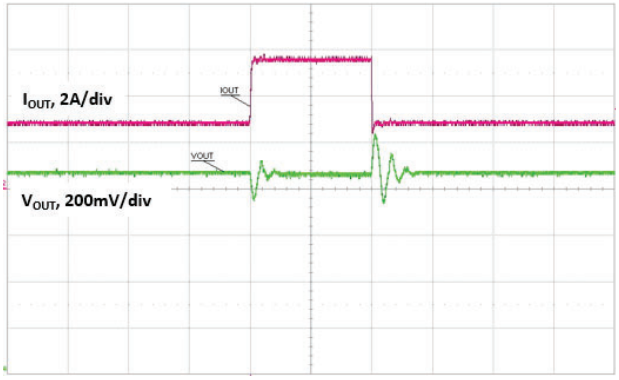

Fig. 48 - Load Transient (3 A to 6 A), Time = 100 µs/div

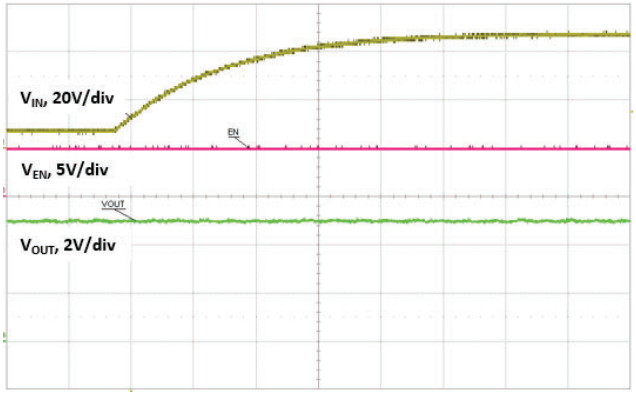

Fig. 51 - Line Transient (8 V to 48 V), Time = 10 ms/div

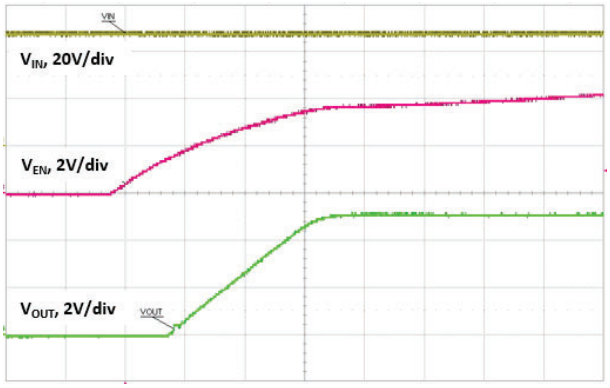

Fig. 49 - Start-Up with EN, Time = 1 ms/div

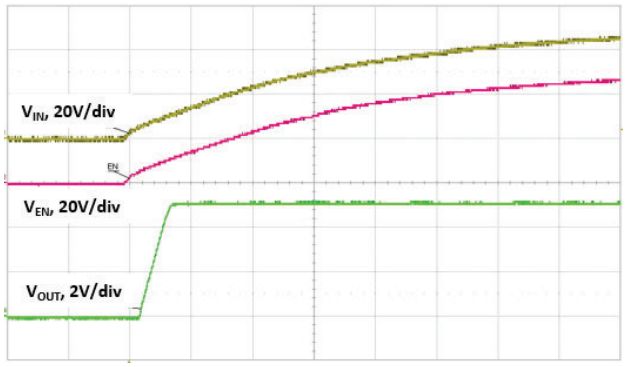

Fig. 52 - Start-up with V_{IN}, Time = 5 ms/div

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ELECTRICAL CHARACTERISTICS (V_{IN} = 48 V, V_{OUT} = 5 V, f_{sw} = 300 kHz, SiC462 (6 A), unless otherwise noted)

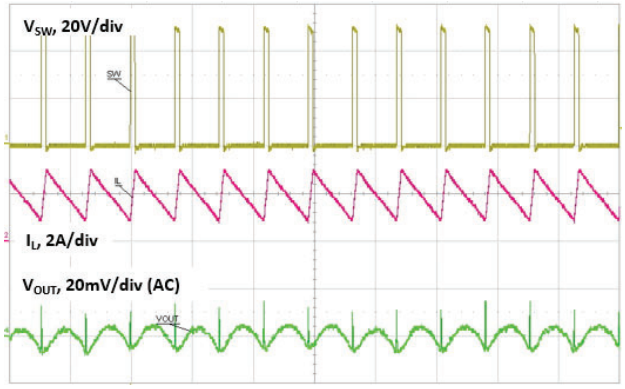

Fig. 53 - Output Ripple 2 A, Time = 5 µs/div

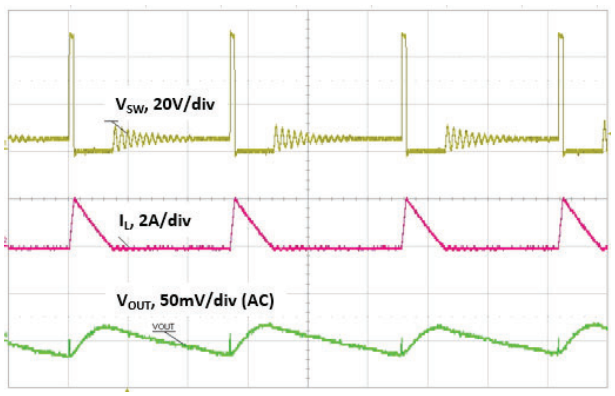

Fig. 55 - Output Ripple 300 mA, Time = 5 µs/div

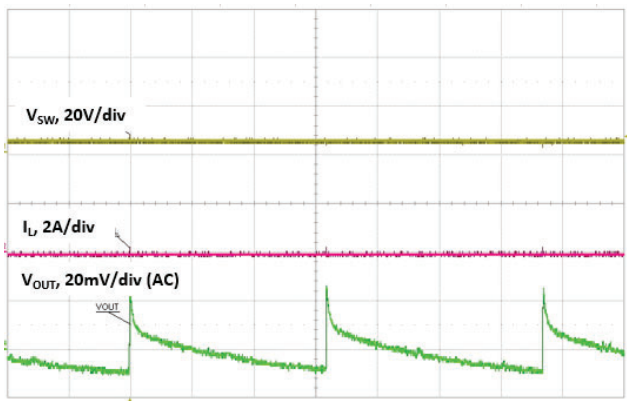

Fig. 54 - Output Ripple PSM, Time = 10 ms/div

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PCB LAYOUT RECOMMENDATIONS

Step 1: V_{IN}/GND Planes and Decoupling

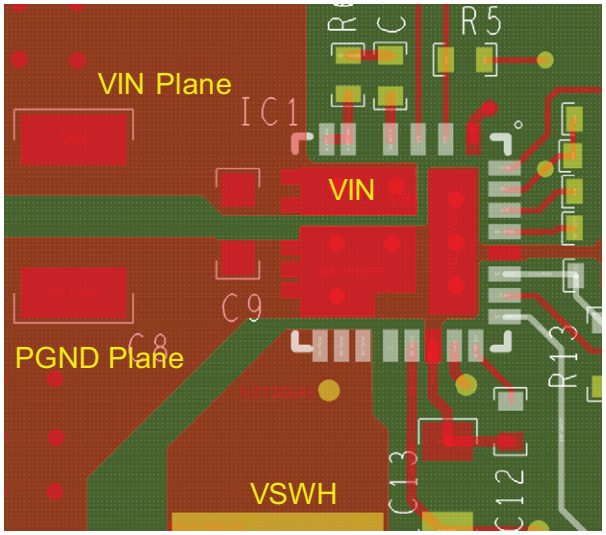

Fig. 56

1. Layout V_{IN} and P_{GND} planes as shown above
2. Ceramic capacitors should be placed between V_{IN} and P_{GND}, and very close to the device for best decoupling effect
3. Different values / packages of ceramic capacitors should be used to cover entire decoupling spectrum e.g. 1210 and 0603
4. Smaller capacitance values, placed closer to device's V_{IN} pin(s), is better for high frequency noise absorbing

Step 2: V_{CIN} Pin

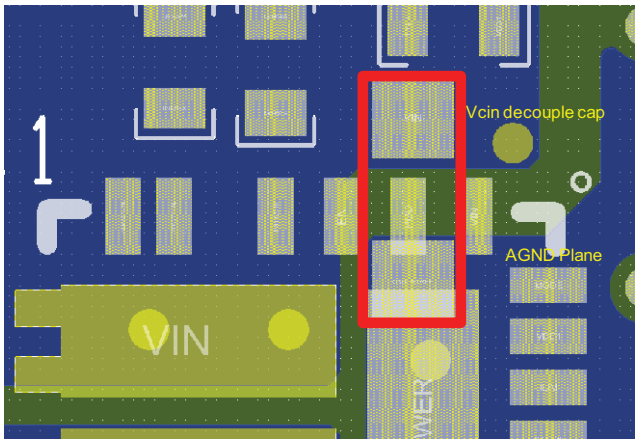

Fig. 57

1. V_{CIN} (pin 1) is the input pin for both internal LDO and t_{ON} block. T_{ON} time varies based on input voltage. It is necessary to put a decoupling capacitor close to this pin
2. The connection can be made through a via and the cap can be placed at bottom layer

Step 3: V_{SWH} Plane

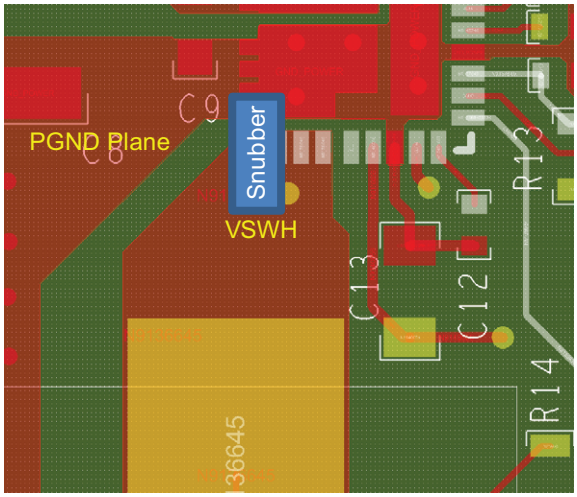

Fig. 58

1. Connect output inductor to SiC462 with large plane to lower the resistance
2. If any snubber network is required, place the components on the bottom side as shown above

Step 4: V_{DD}/V_{DRV} Input Filter

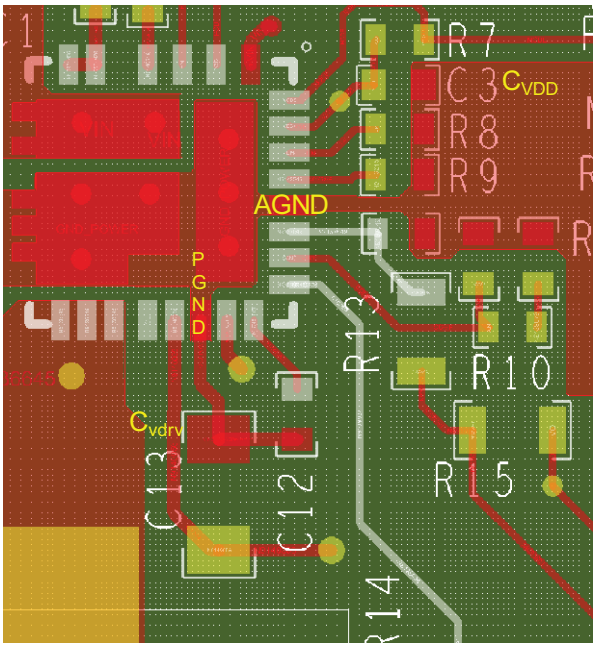

Fig. 59

1. C_{VDD} cap should be placed between pin 26 and pin 23 (the A_{GND} of driver IC) to achieve best noise filtering
2. C_{VDRV} cap should be placed close to V_{DRV} (pin 16) and P_{GND} (pin 17) to reduce effects of trace impedance and provide maximum instantaneous driver current for low side MOSFET during switching cycle

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Step 5: BOOT Resistor and Capacitor Placement

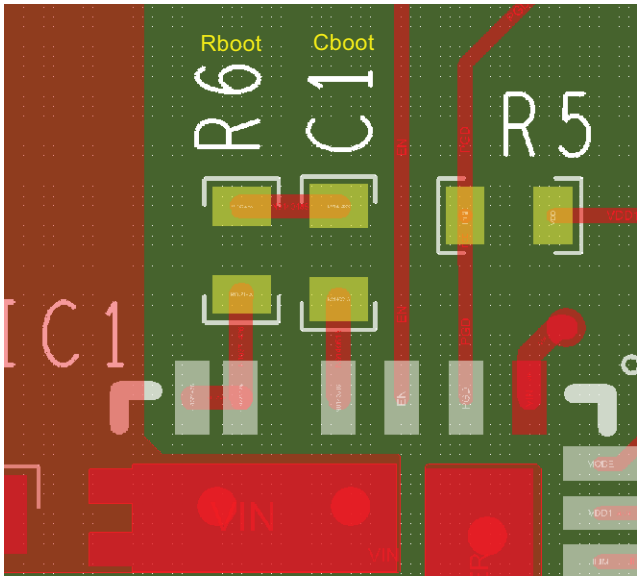

Fig. 60

1. These components need to be placed very close to SiC462, right between PHASE (pin 5, 6) and BOOT (pin 4)
2. In order to reduce parasitic inductance, it is recommended to use 0402 chip size for the resistor and the capacitor

Step 6: Signal Routing

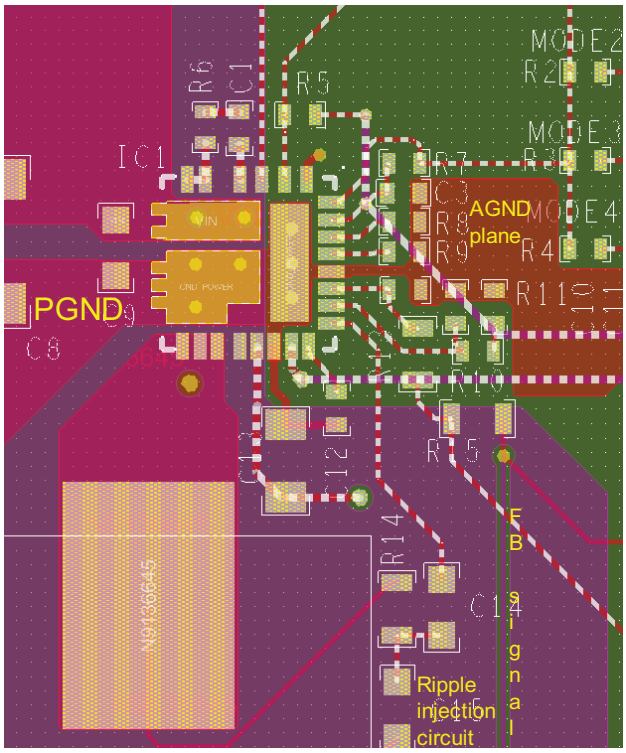

Fig. 61

1. Separate the small analog signal from high current path. As shown above, the high current paths with high dv/dt, di/dt are placed on the left side of the IC, while the small control signals are placed on the right side of the IC. All the components for small analog signal should be placed closer to IC with minimum trace length
2. Pin 23 is the IC analog ground, which should have a single connection to power ground. The A_{GND} ground plane connected with pin 23 helps keep A_{GND} quiet and improve noise immunity
3. Feedback signal can be routed through inner layer. Make sure this signal is far away from V_{SWH} node and shielded by inner ground layer
4. Ripple injection circuit can be placed next to inductor. Kelvin connection as shown above is recommended

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Step 7: Adding Thermal Relief Vias and Duplicate Power Path Plane

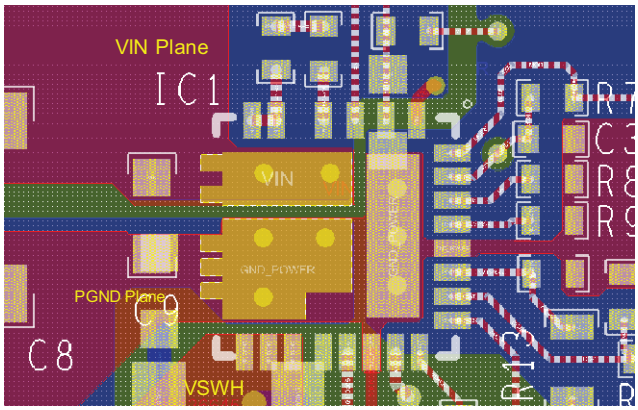

Fig. 62

1. Thermal relief vias can be added on the V_{IN} and P_{GND} pads to utilize inner layers for high current and thermal dissipation
2. To achieve better thermal performance, additional vias can be put on V_{IN} and P_{GND} plane. Also, it is necessary to duplicate the V_{IN} and ground planes at bottom layer to maximize the power dissipation capability from PCB.
3. V_{SWH} pad is a noise surce and not recommended to put vias on this pad.
4. 8 mil drill for pads and 10 mils drill for plane are optional via sizes. The vias on pads may drain solder during assembly and cause assembly issues. Please consult with the assembly house for guidelines

Step 8: Ground Layer

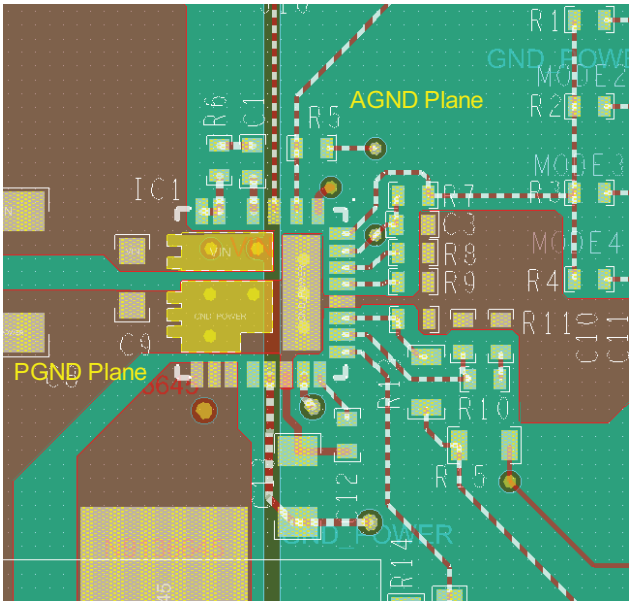

Fig. 63

1. It is recommended to make the entire inner layer (next to top layer) ground plane
2. This ground plane provides shielding between noise source on top layer and signal trace within inner layer.
3. The ground plane can be broken into two sections as P_{GND} and A_{GND}

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PRODUCT SUMMARY				
Part number	SiC461	SiC462	SiC463	SiC464
Description	to 60 V input, 100 kHz to 2 MHz, synchronous buck regulator	6 A, 4.5 V to 60 V input, 100 kHz to 2 MHz, synchronous buck regulator	4 A, 4.5 V to 60 V input, 100 kHz to 2 MHz, synchronous buck regulator	2 A, 4.5 V to 60 V input, 100 kHz to 2 MHz, synchronous buck regulator
Input voltage min. (V)	4.5	4.5	4.5	4.5
Input voltage max. (V)	60	60	60	60
Output voltage min. (V)	0.8	0.8	0.8	0.8
Output voltage max. (V)	0.92 x V_{IN}	0.92 x V_{IN}	0.92 x V_{IN}	0.92 x V_{IN}
Continuous current (A)	10	6	4	2
Switch frequency min. (kHz)	100	100	100	100
Switch frequency max. (kHz)	2000	2000	2000	2000
Pre-bias operation (yes / no)	Yes	Yes	Yes	Yes
Internal bias reg. (yes / no)	Yes	Yes	Yes	Yes
Compensation	External	External	External	External
Enable (yes / no)	Yes	Yes	Yes	Yes
P_{GOOD} (yes / no)	Yes	Yes	Yes	Yes
Over current protection	Yes	Yes	Yes	Yes
Protection	OVP, OCP, UVP/SCP, OTP, UVLO	OVP, OCP, UVP/SCP, OTP, UVLO	OVP, OCP, UVP/SCP, OTP, UVLO	OVP, OCP, UVP/SCP, OTP, UVLO
Light load mode	Selectable powersave / ultrasonic	Selectable powersave / ultrasonic	Selectable powersave / ultrasonic	Selectable powersave / ultrasonic
Peak efficiency (%)	98	98	98	98
Package type	PowerPAK MLP55-27L	PowerPAK MLP55-27L	PowerPAK MLP55-27L	PowerPAK MLP55-27L
Package size (W, L, H) (mm)	5 x 5 x 0.75	5 x 5 x 0.75	5 x 5 x 0.75	5 x 5 x 0.75
Status code	1	1	1	1
Product type	microBUCK (step down regulator)	microBUCK (step down regulator)	microBUCK (step down regulator)	microBUCK (step down regulator)
Applications	Computing, consumer, industrial, healthcare, networking	Computing, consumer, industrial, healthcare, networking	Computing, consumer, industrial, healthcare, networking	Computing, consumer, industrial, healthcare, networking

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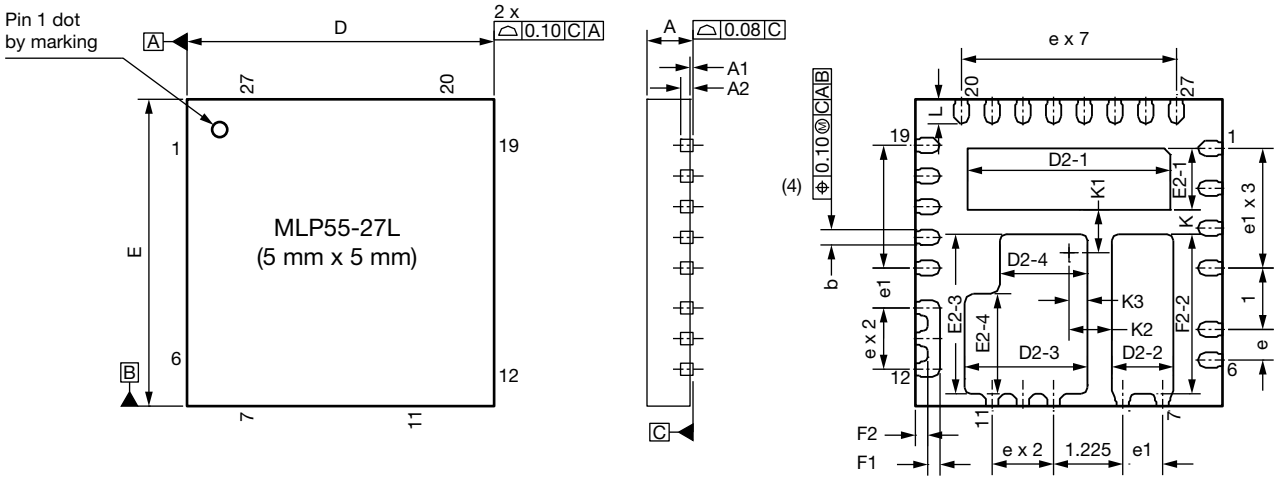
PowerPAK® MLP55-27 Case Outline



Top view Side view Bottom view

DIM.	MILLIMETERS			INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A (8)	0.70	0.75	0.80	0.027	0.029	0.031
A1	0.00	-	0.05	0.000	-	0.002
A2	0.20 ref.			0.008 ref.		
b (4)	0.20	0.25	0.30	0.078	0.098	0.110
D	5.00 BSC			0.196 BSC		
e	0.50 BSC			0.019 BSC		
e1	0.65 BSC			0.0256 BSC		
E	5.00 BSC			0.196 BSC		
L	0.35	0.40	0.45	0.014	0.016	0.018
N (3)	28			28		
D2-1	3.25	3.30	3.35	0.128	0.130	0.132
D2-2	0.95	1.00	1.05	0.037	0.039	0.041
D2-3	1.95	2.00	2.05	0.077	0.079	0.081
D2-4	1.37	1.42	1.47	0.054	0.056	0.058
E2-1	0.95	1.00	1.05	0.037	0.039	0.041
E2-2	2.55	2.60	2.65	0.100	0.102	0.104
E2-3	2.55	2.60	2.65	0.100	0.102	0.104
E2-4	1.58	1.63	1.68	0.062	0.064	0.066
F1	0.20	-	0.25	0.008	-	0.010
F2	min. 0.20			min. 0.008		
K	0.40 BSC			0.016 BSC		
K1	0.70 BSC			0.028 BSC		
K2	0.70 BSC			0.028 BSC		
K3	0.30 BSC			0.012 BSC		
ECN: T16-0944-Rev. A, 02-Jan-17 DWG: 6056						

Notes

(1) Use millimeters as the primary measurement
(2) Dimensioning and tolerances conform to ASME Y14.5M. - 1994
(3) N is the number of terminals.
(4) Dimension b applies to plated terminal and is measured between 0.20 mm and 0.25 mm from terminal tip
(5) The pin #1 identifier must be existed on the top surface of the package by using indentation mark or other feature of package body
(6) Exact shape and size of this feature is optional
(7) Package warpage max. 0.08 mm
(8) Applied only for terminals

For technical questions, contact: powerictechsupport@vishay.com

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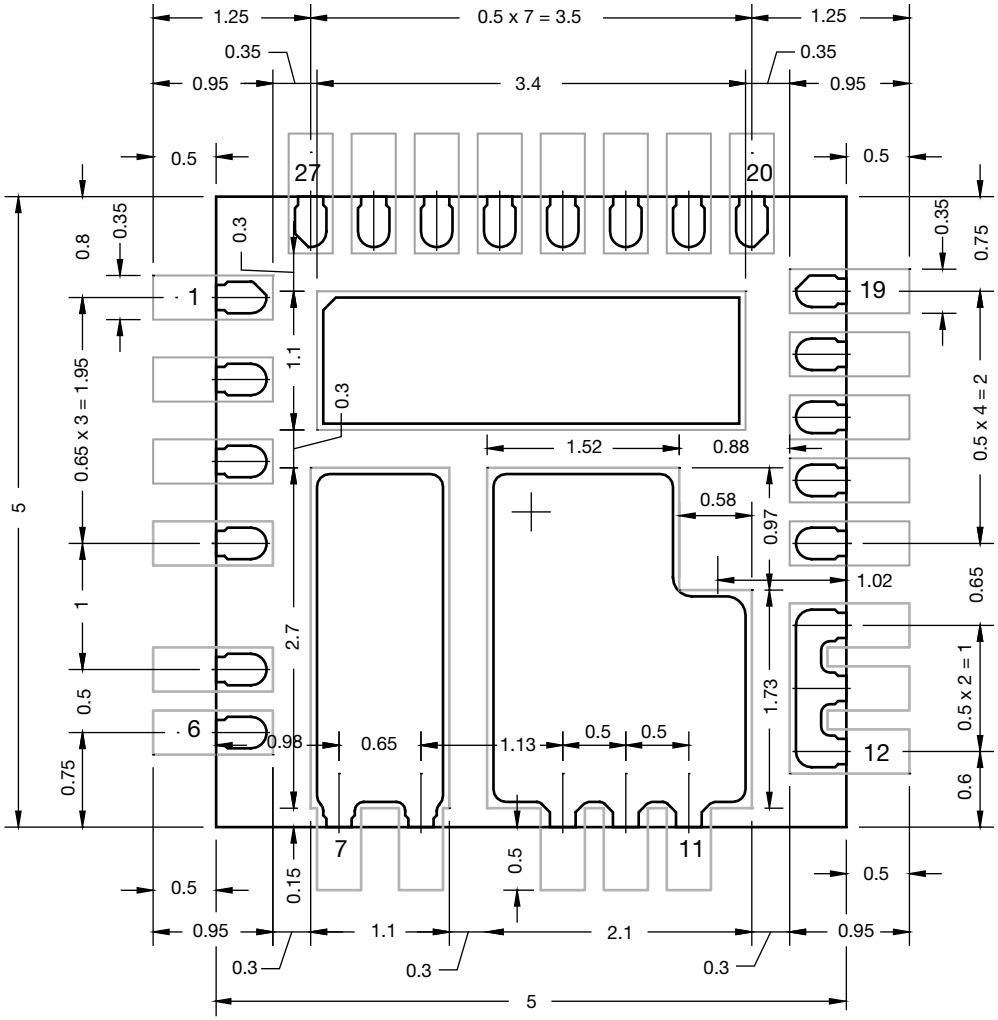
Recommended Land Pattern
PowerPAK® MLP55-27L



All dimensions in millimeters

Component for MLP55-27L

Land pattern for MLP55-27L

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