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LF2184N

Half-Bridge Gate Driver

Features

- **Floating high-side driver in bootstrap operation to 600V**
- **Drives two N-channel MOSFETs or IGBTs in a half bridge configuration**
- **1.4A source / 1.8A sink output current capability**
- **Outputs tolerant to negative transients**
- **Internal dead time of 400ns to protect MOSFETs**
- **Wide low side gate driver supply voltage: 10V to 20V**
- **Logic input (IN and SD*) 3.3V capability**
- **Schmitt triggered logic inputs with internal pull down**
- **Under Voltage Lockout (UVLO) for high and low side drivers**
- **Extended temperature range: -40°C to +125°C**

Description

The LF2184N is a high voltage, high speed gate driver capable of driving N-channel MOSFETs and IGBTs in a half bridge configuration. The high voltage technology enables the LF2184N's high side to switch to 600V in a bootstrap operation.

LF2184N logic inputs are compatible with standard TTL and CMOS levels (down to 3.3V) to interface easily with controlling devices. The driver outputs feature high pulse current buffers designed for minimum driver cross conduction. LF2184N has a fixed internal deadtime of 400ns (typical).

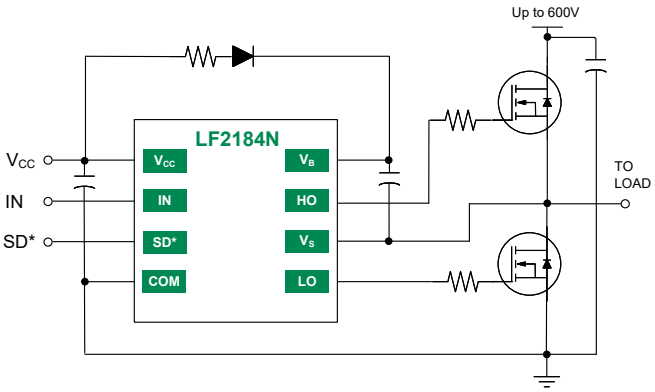
LF2184N is offered in SOIC(N)-8 packages and operates over the extended temperature range of -40 °C to +125 °C .

Applications

- DC-DC Converters
- AC-DC Inverters
- Motor Controls
- Class D Power Amplifiers

SOIC(N)-8

Typical Application



Ordering Information

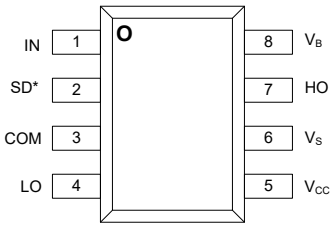
Year Year Week Week

Part#	Package	Pack / Qty	Mark
LF2184NTR	SOIC(N)-8	T&R / 2500	YYWW LF2184N LOT ID

sales@prom-elec.com / ООО ПРОМЭЛЕКТРОНИКА

1 Specifications

1.1 Pin Diagrams



Top View: SOIC(N)-8

LF2184N

1.2 Pin Descriptions

Pin #	Pin Name	Pin Type	Pack / Qty
1	IN	Input	Logic input for high-side and low-side gate driver outputs (HO and LO), in phase with HO.
2	SD*	Input	Logic input for shutdown, active low
3	COM	Power	Low-side and logic return
4	LO	Output	Low-side gate drive output
5	V_{CC}	Power	Low-side and logic fixed supply
6	V_S	Power	High-side floating supply return
7	HO	Output	High-side gate drive output
8	V_B	Power	High-side floating supply

1.3 Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit
High side floating supply voltage	V_B	-0.3	+624	V
High side floating supply offset voltage	V_S	V_B-24	V_B+0.3	V
High side floating output voltage	V_{HO}	V_S-0.3	V_B+0.3	V
Offset supply voltage transient	dV_S/dt	--	50	V/ns
Low side fixed supply voltage	V_{CC}	-0.3	+24	V
Low side output voltage	V_{LO}	-0.3	V_{CC}+0.3	V
Logic input voltage (HIN and LIN)	V_{IN}	-0.3	V_{CC}+0.3	V
Package power dissipation	P_D	--	0.625	W
Junction Operating Temperature	T_J	--	+150	°C
Storage Temperature	T_{STG}	-55	+150	°C

Unless otherwise specified all voltages are referenced to COM . All electrical ratings are at T_A= 25 °C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

1.4 Thermal Characteristics

Parameter	Symbol	Rating	Unit
Junction to ambient	$Ø_{JA}$	200	° C/W

When mounted on a standard JEDEC 2-layer FR-4 board - JESD51-3

1.5 Recommended Operating Conditions

Parameter	Symbol	Min	Max	Unit
High side floating supply absolute voltage	V_B	$V_S + 10$	$V_S + 20$	V
High side floating supply offset voltage	V_S	***NOTE1***	600	V
High side floating output voltage	V_{HO}	V_S	V_B	V
Low side fixed supply voltage	V_{CC}	10	20	V
Low side output voltage	V_{LO}	0	V_{CC}	V
Logic input voltage (HIN and LIN)	V_{IN}	0	5	V
Ambient temperature	T_A	-40	125	°C

Unless otherwise specified all voltages are referenced to COM

NOTE1 *High-side driver remains operational for V_S transients down to -5V*

1.6 DC Electrical Characteristics

$V_{CC} = V_{BS}$=15V, T_A = 25 °C and V_{COM} = 0V , unless otherwise specified.

The V_{IN} and I_{IN} parameters are applicable to both logic input pins: IN and SD. The V_O and I_O parameters are applicable to the respective output pins: HO and LO and are referenced to COM*

Parameter	Symbol	Conditions	MIn	Typ	Max	Unit
Logic "1" input voltage	V_{IH}	V_{CC} = 10V to 20V **Note 2**	2.5	--	--	V
Logic "0" input voltage	V_{IL}		--	--	0.8	
Logic input voltage hysteresis	$V_{IN(HYS)}$		--	0.30	--	
High level output voltage, V_{BIAS} - V_O	V_{OH}	I_O = 0A	--	--	1.2	
Low level output voltage, V_O	V_{OL}	I_O = 20mA	--	--	0.1	
Offset supply leakage current	I_{LK}	$V_B = V_S$ = 600V	--	--	50	µA
Quiescent V_{BS} supply current	I_{BSQ}	V_{IN} = 0V or 5V	20	60	150	
Quiescent V_{CC} supply current	I_{CCQ}	V_{IN} = 0V or 5V	0.4	1.6	2.0	mA
Logic "1" input bias current	I_{IN+}	IN = 5V SD* = 0V	--	25	60	µA
Logic "0" input bias current	I_{IN-}	IN = 0V SD* = 5V	--	--	1.0	
V_{BS} UVLO off positive going threshold	V_{BSUV+}	--	8.0	8.9	9.8	V
V_{BS} UVLO enable negative going threshold	V_{BSUV-}	--	7.4	8.2	9.0	
V_{BS} UVLO hysteresis	$V_{BSUV(HYS)}$	--	--	0.7	--	
V_{CC} UVLO off positive going threshold	V_{CCUV+}	--	8.0	8.9	9.8	
V_{CC} UVLO enable negative going threshold	V_{CCUV-}	--	7.4	8.2	9.0	
V_{CC}UVLO hysteresis	$V_{CCUV(HYS)}$	--	--	0.7	--	
Output high short circuit pulsed current	I_{O+}	V_O = 0V, t ≤ 10 µs	1.4	1.9	--	A
Output low short circuit pulsed current	I_{O-}	V_O = 15V, t ≤ 10 µs	1.7	2.3	--	

NOTE2 *For optimal operation, it is highly recommended the input pulse to IN should have a minimum amplitude of 2.5V with a minimum pulse width of 360ns.*

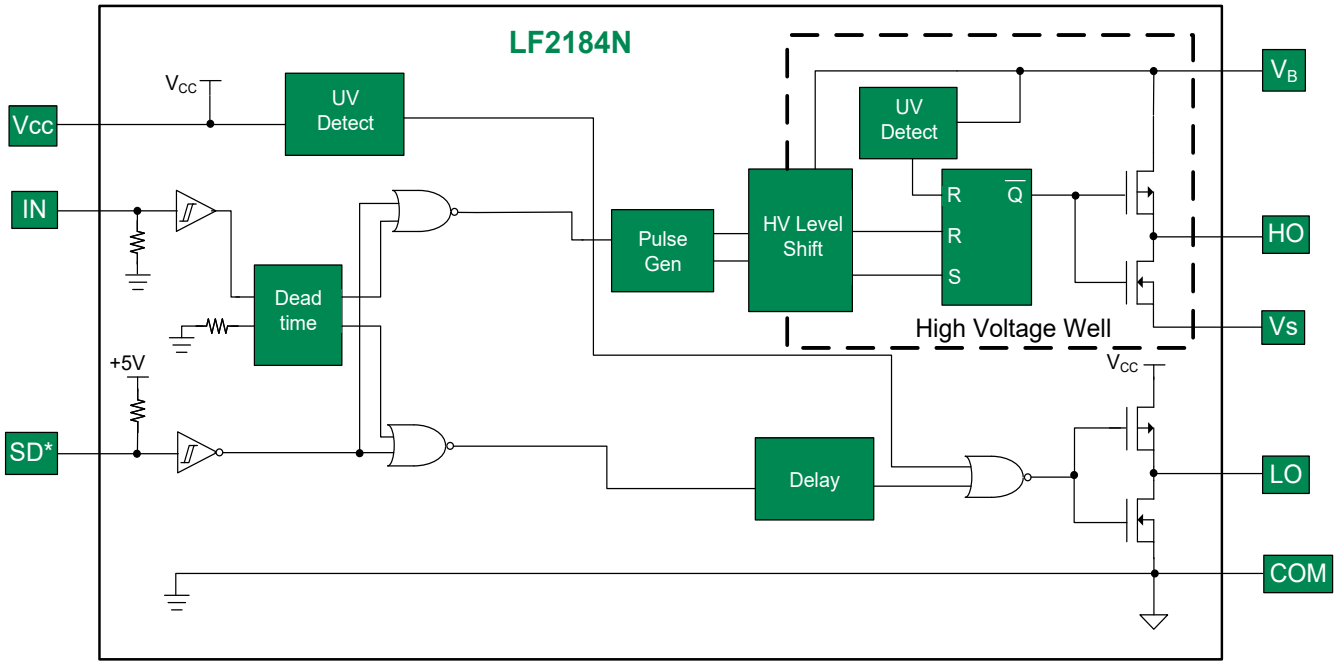
1.7 AC Electrical Characteristics

V_{CC}= V_{BS} =15V, C_L = 1000pF, and T_A = 25 °C , unless otherwise specified.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Turn-on propogation delay	t_{on}	V_S = 0V	--	680	900	ns
Turn-off propogation delay	t_{off}	V_S = 0V or 600V	--	270	400	
Shut-down propagation delay	t_{SD*}	--	--	180	270	
Propagation delay matching, HO & LO turn-on	$t_{DM\ ON}$	--	--	--	90	
Propagation delay matching, HO & LO turn-off	$t_{DM\ OFF}$	I_O = 0A	--	--	40	
Turn-on rise time	t_r	V_S = 0V	--	40	60	
Turn-off fall time	t_f		--	20	35	
Deadtime : $t_{DT\ LO-HO}$ & $t_{DT\ HO-LO}$	t_{DT}	--	280	400	520	
Deadtime Matching	$t_{DT\ MT}$	--	--	--	60	

2 Functional Description

2.1 Functional Block Diagram



2.2 Timing Waveforms

Figure 1. Input / Output Logic Diagram

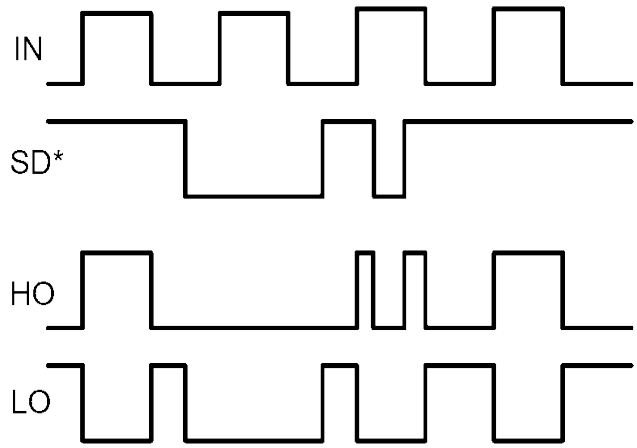


Figure 2. Shutdown Timing Diagram

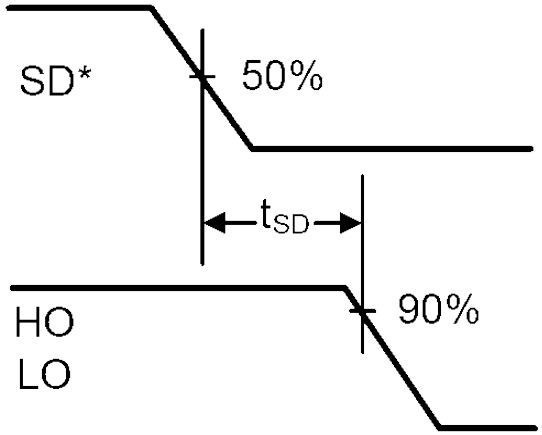
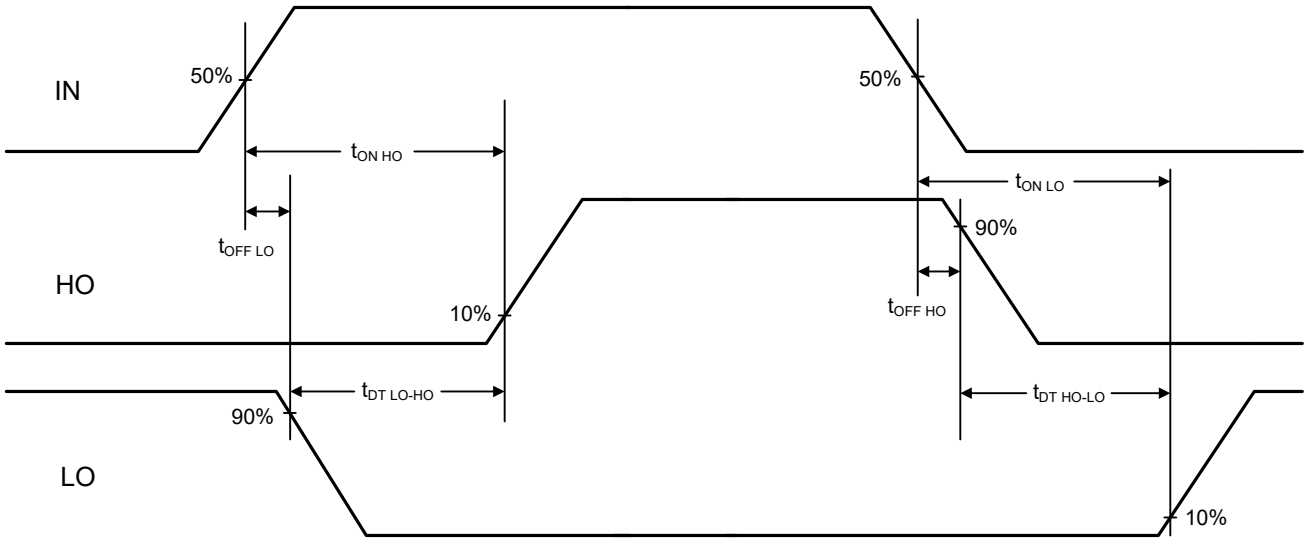


Figure 3. Input-to-Output Delay Timing Diagram



Deadtime: $t_{DT\ LO\text{-}HO} = t_{ON\ HO} - t_{OFF\ LO}$

$t_{DT\ HO\text{-}LO} = t_{ON\ LO} - t_{OFF\ HO}$

Delay matching

$t_{DM\ OFF} = |t_{OFF\ LO} - t_{OFF\ HO}|$

$t_{DM\ ON} = |t_{ON\ LO} - t_{ON\ HO}|$

Deadtime Matching: $t_{DT\ MT} = |t_{DT\ LO\text{-}HO} - t_{DT\ HO\text{-}LO}|$

2.3 Application Information

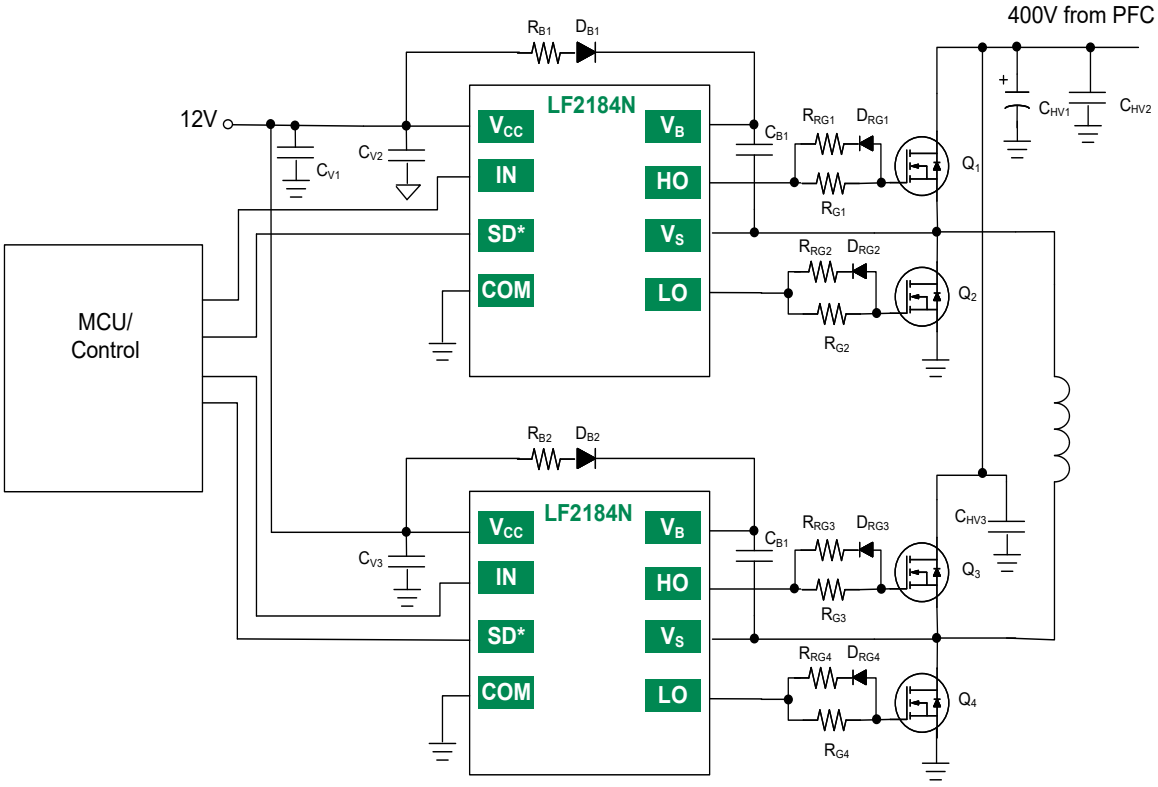


Figure 4. Primary side of Full Bridge converter using LF2184N

- RRG1, RRG2, RRG3, and RRG4 values are typically between 0Ω and 10Ω, exact value decided by MOSFET junction capacitance and drive current of gate driver; 10Ω is used in this example.

- It is **highly recommended** that the input pulse to IN should have a minimum amplitude of 2.5V (for VDD=15V) with a minimum pulse width of 800ns.

- RG1, RG2, RG3, and RG4 values are typically between 20Ω and 100Ω, exact value decided by MOSFET junction capacitance and drive current of gate driver; 50Ω is used in this example.

- RB1 and RB2 value is typically between 3Ω and 20Ω, exact value depending on bootstrap capacitor value and amount of current limiting required for bootstrap capacitor charging; 10Ω is used in this example. Also DB1 and DB2 should be an ultra fast diode of 1A rating minimum and voltage rating greater than system operating voltage.

3 Performance Data

Unless otherwise noted $V_{CC} = V_{BS} = 15V$, $T_A = 25\ °C$, $V_{COM} = 0V$ and values are typical.

Figure 5. Turn-on Propagation Delay vs. Supply Voltage

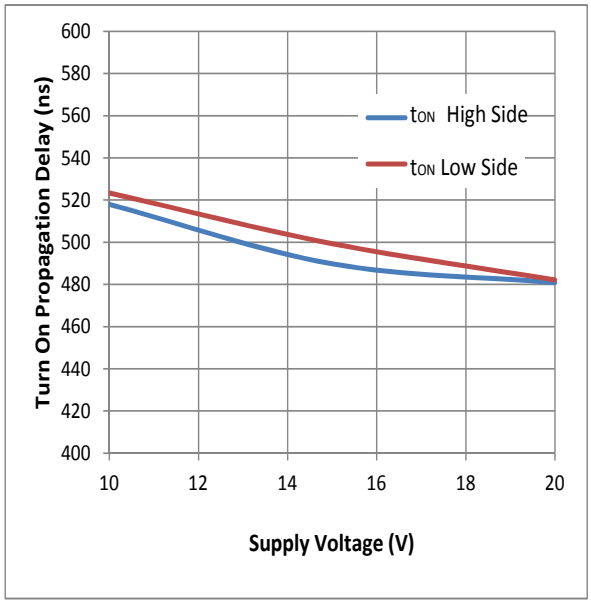


Figure 6. Turn-on Propagation Delay vs. Temperature

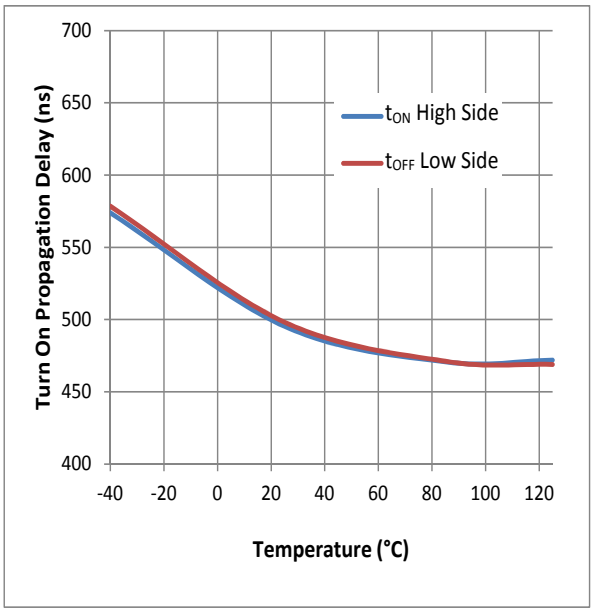


Figure 7. Turn-off Propagation Delay vs. Supply Voltage

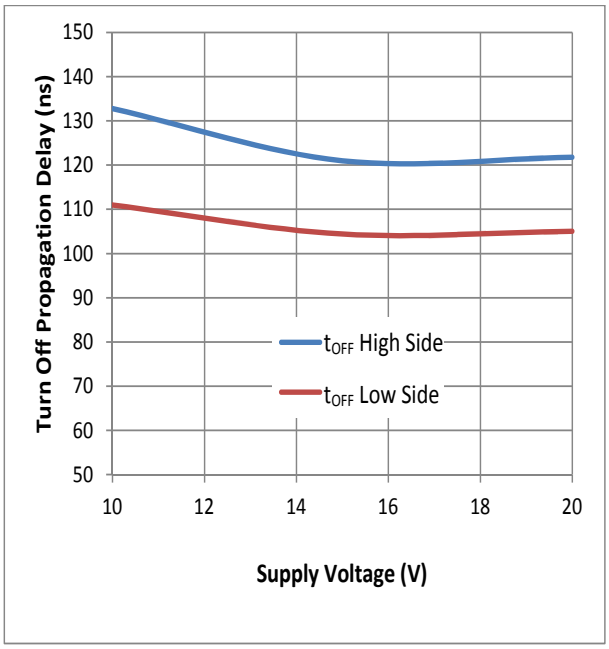


Figure 8. Turn-off Propagation Delay vs. Temperature

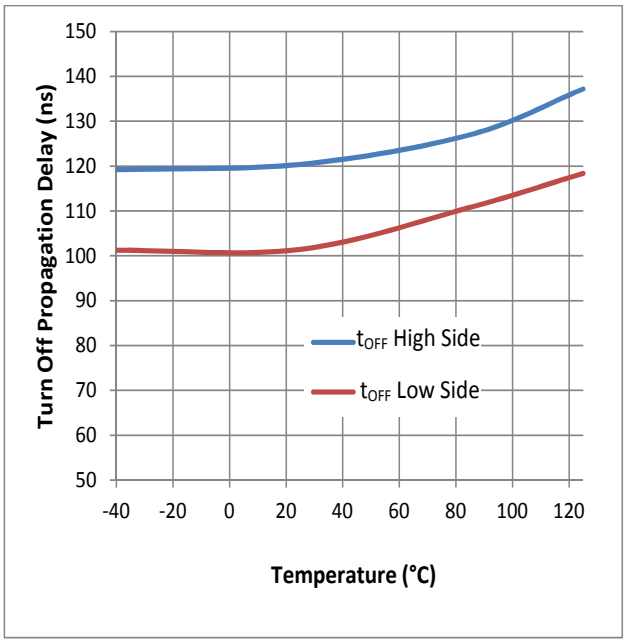


Figure 9. Rise Time vs. Supply Voltage

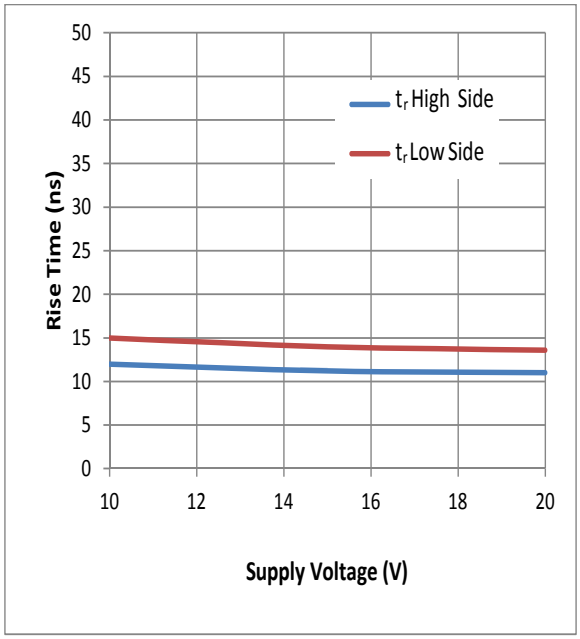


Figure 10. Rise Time vs. Temperature

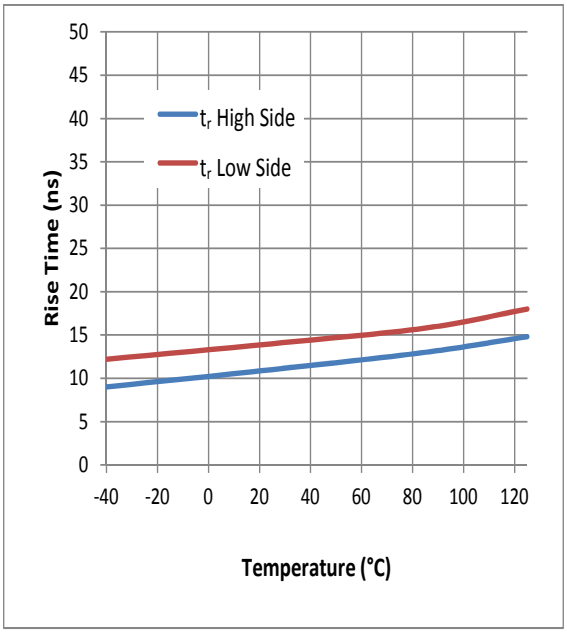


Figure 11. Fall Time vs. Supply Voltage

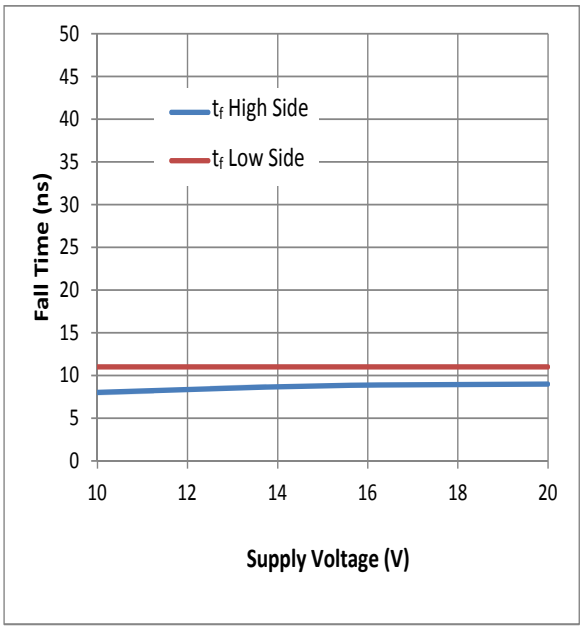


Figure 12. Fall Time vs. Temperature

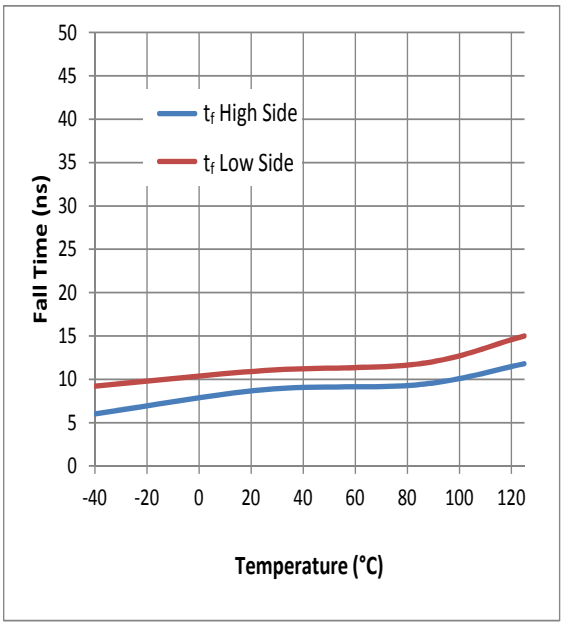


Figure 13. Deadtime vs. Supply Voltage

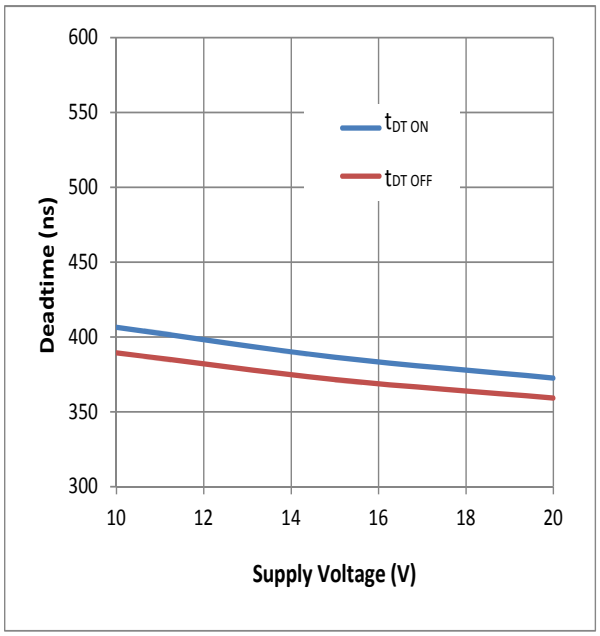


Figure 14. Deadtime vs. Temperature

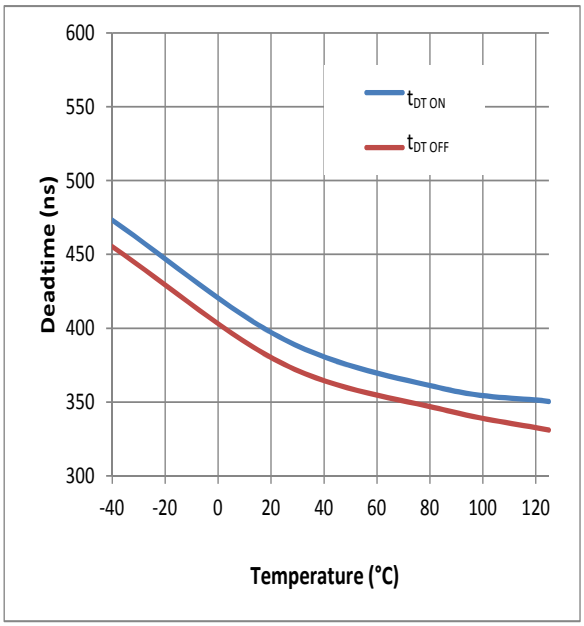


Figure 15. Delay Matching vs. Supply Voltage

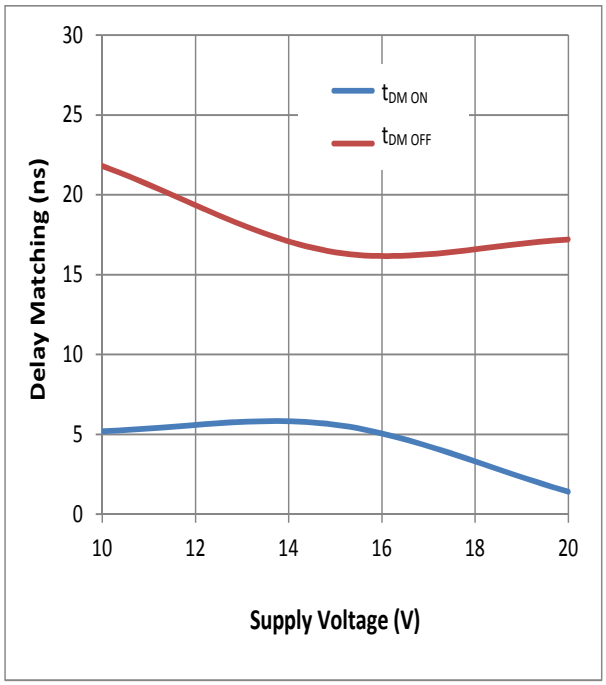


Figure 16. Delay Matching vs. Temperature

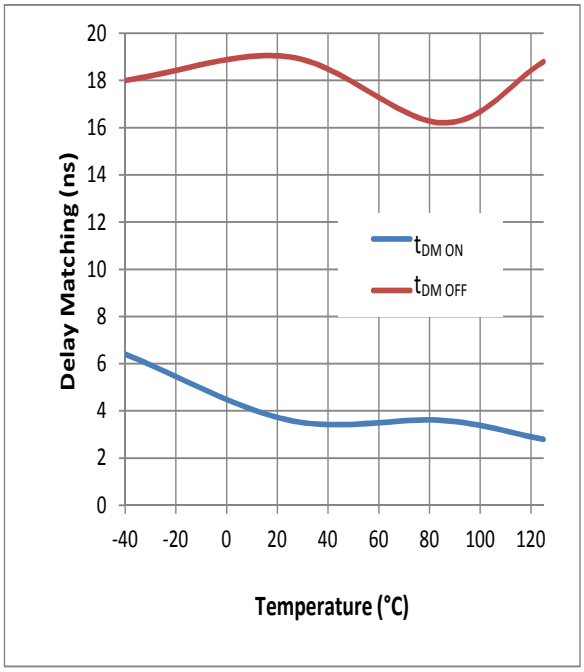


Figure 17. Output Source Current vs. Supply Voltage

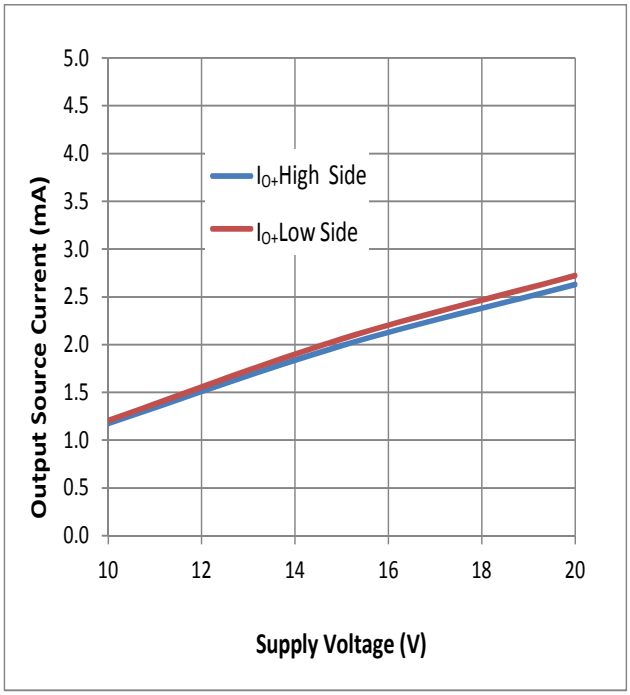


Figure 18. Output Source Current vs. Temperature

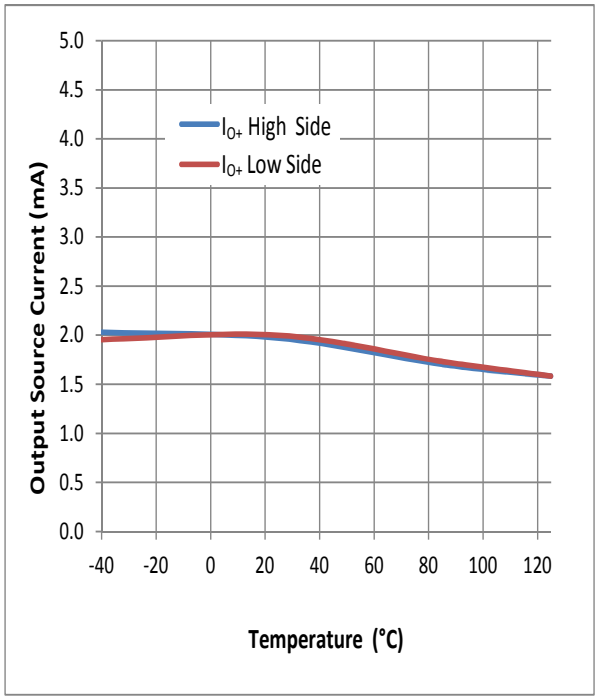


Figure 19. Output Sink Current vs. Supply Voltage

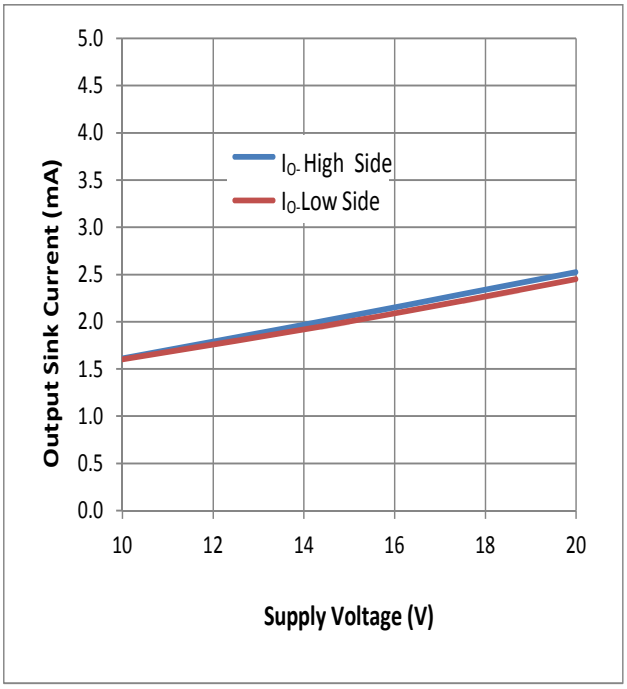


Figure 20. Output Sink Current vs. Temperature

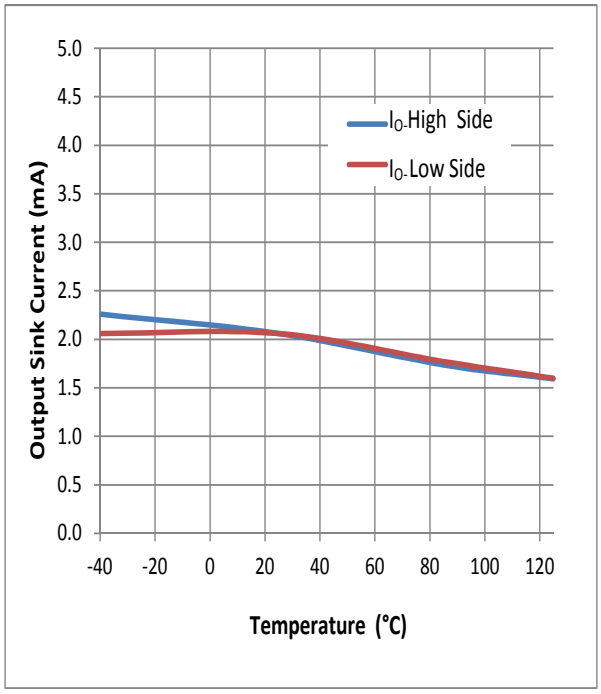


Figure 21. Quiescent Current vs. Supply Voltage

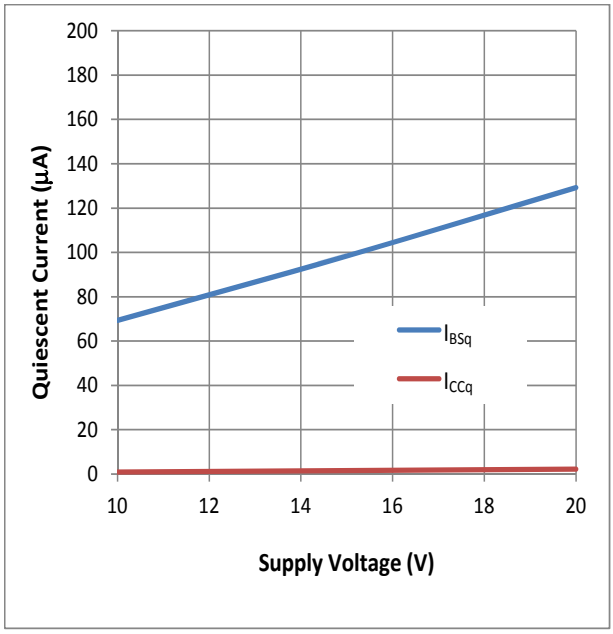


Figure 22. Quiescent Current vs. Temperature

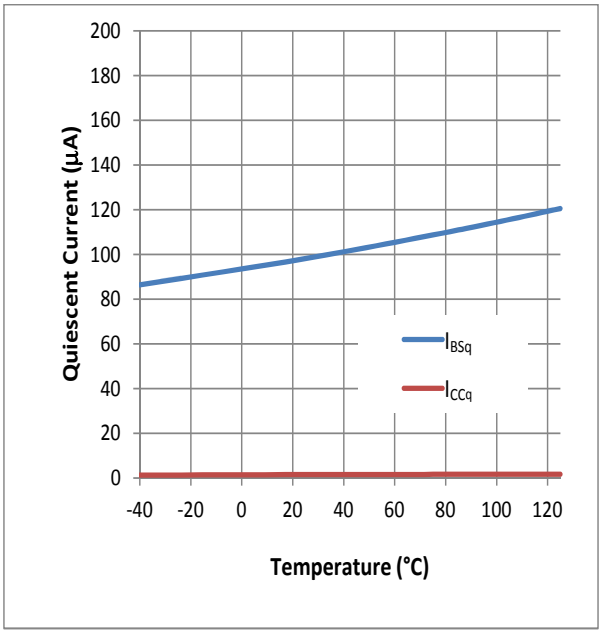


Figure 23. Logic 1 Input Voltage vs. Supply Voltage

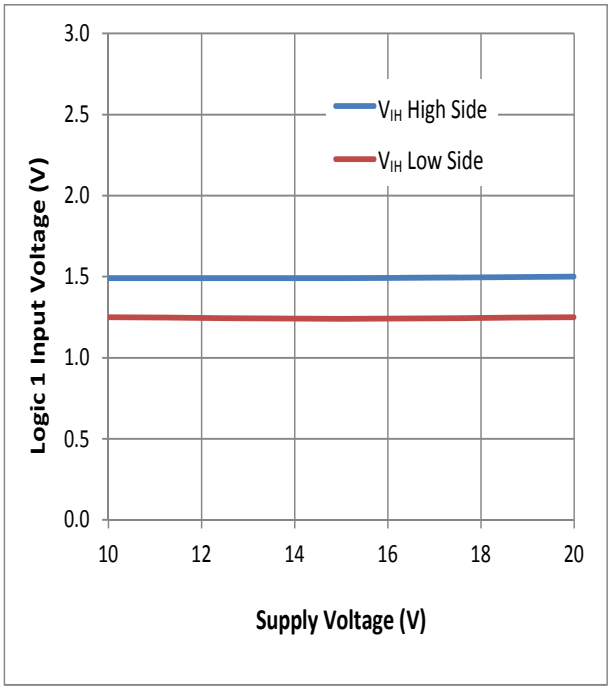


Figure 24. Logic 1 Input Voltage vs. Temperature

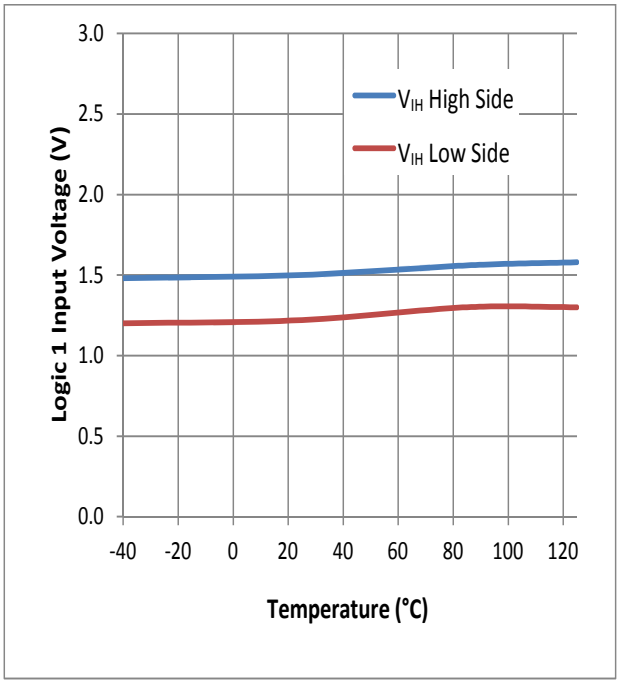


Figure 25. Logic 0 Input Voltage vs. Supply Voltage

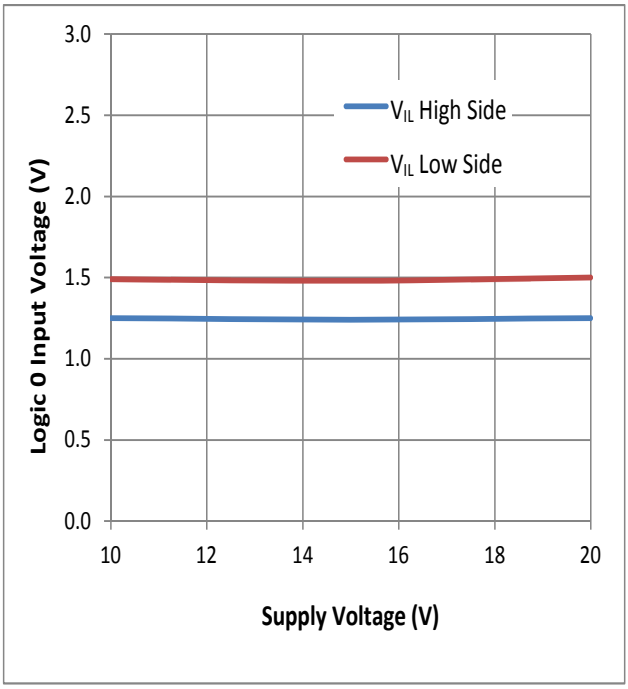


Figure 26. Logic 0 Input Voltage vs. Temperature

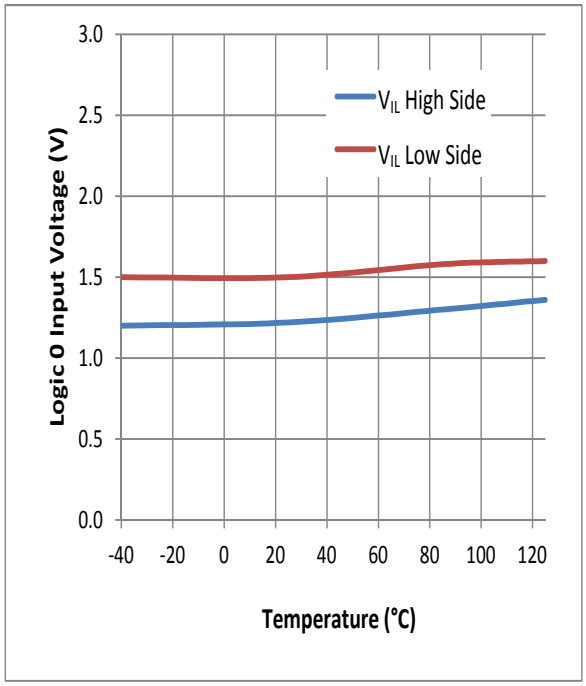


Figure 27. V_{CC} UVLO vs. Temperature

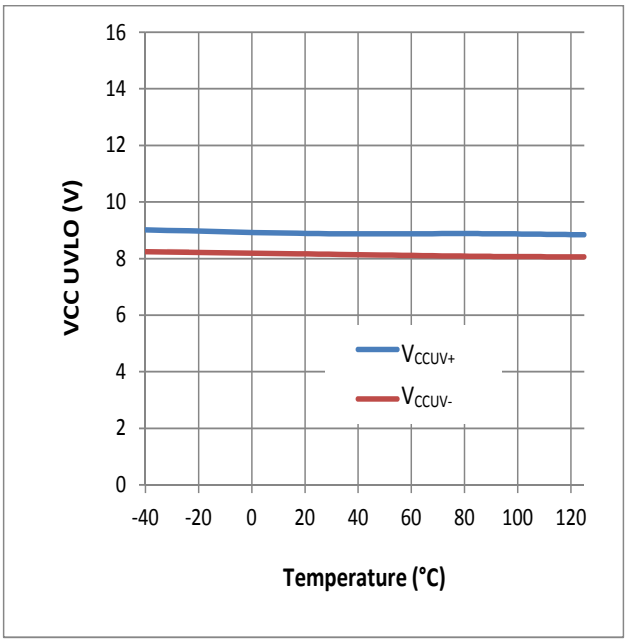
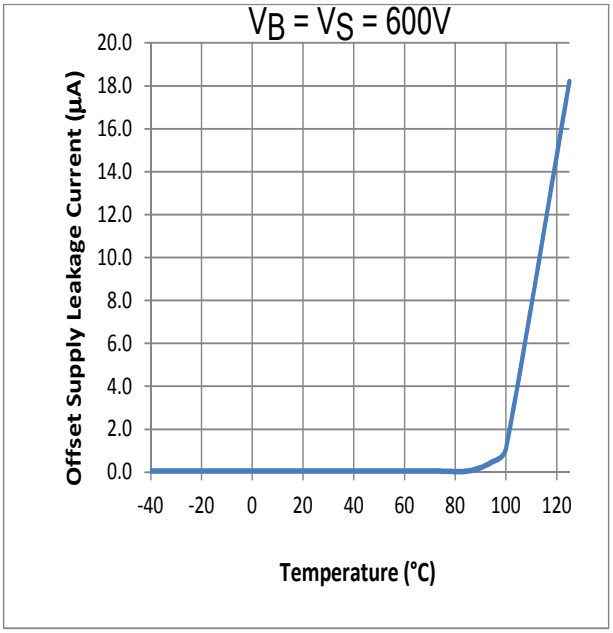


Figure 28. Offset Supply Leakage Current Temperature



4 Application Information

4.1 Half-bridge Configuration

A common configuration used for the LF2184N is a half-bridge (see fig. 29). In a half-bridge configuration the source of the high-side MOSFET (Q_H) and the drain of the low-side MOSFET (Q_L) are connected. That line (V_S) is both the return for the high side in the gate driver IC as well as the output of the half-bridge. When Q_H is on and Q_L is off, V_S swings to high voltage, and when Q_H is off and Q_L is on, V_S swings to GND. Hence the output switches from GND to high voltage at the frequency of HIN and LIN, this line drives a transformer for a power supply, or a coil on a motor

In this half-bridge configuration, high voltage DC is input to the MOSFETs, and converted to a high voltage switching signal to output to load (fig 29).

The MOSFETs operate in saturation mode and an important function of the gate driver is to turn on the MOSFET quickly to minimize switching losses from the linear region of the MOSFET (turn on and turn off); the LF2184N has a typical rise/fall time of 40ns/20ns into a 1nF load.

Another important function of the gate driver IC in the half-bridge configuration is to convert the logic signals of control (LF2184N operates at logic 3V), to a voltage level and current capacity to drive the gate of the MOSFET and IGBT; this requires driving large currents initially to turn on/turn off the MOSFET quickly. Also the floating well of the high-side allows high voltage operation in the bootstrap operation.

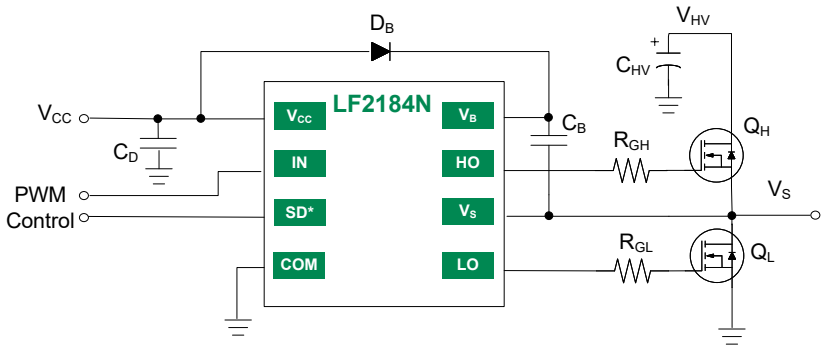


Figure 29. LF2184N in a half-bridge configuration

4.2 Bootstrap Operation

The supply for the LF2184N High Side is provided by the bootstrap capacitor C_B (see fig 30). In the half-bridge configuration, V_S swings from 0V to V_{HV} depending on the PWM input ot the IC. When V_S is 0V, V_{BS} will go below V_{CC} and V_{CC} will charge C_B. When HO goes high, V_S swings to V_{HV}, and V_{BS} remains at V_{CC} minus a diode drop (D_B) due to the voltage on C_B. This is the supply for the high side gate driver and allows the gate driver to function with the floating well (V_S) at the high voltage.

When considering the **value of the bootstrap capacitor C_B**, it is important that it is sized to provide enough energy to quickly drive the gate of Q_H. Values of 1µF to 10µF are recommended, exact value depending on gate capacitance, and the noise in application. It is key to use a low ESR capacitor that is close to the device. This will best quickly supply charge to the gate of the MOSFET.

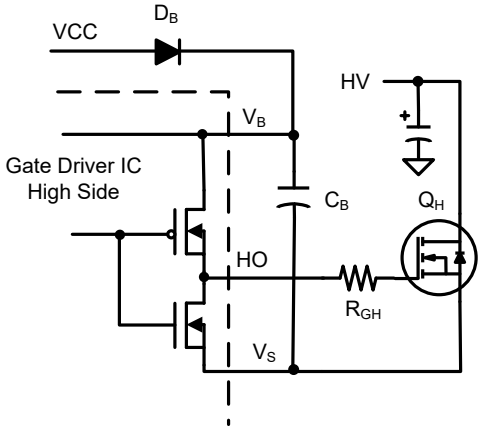


Figure 30. LF2184N high-side in bootstrap operation

4.3 Gate Drive Control

The most crucial time in the gate drive is the turn on and turn off of the MOSFET, and performing this function quickly, but with minimal noise and ringing is key. Too fast a rise/fall time can cause unnecessary ringing, and too slow a rise/fall time will increase switching losses in the MOSFET.

An example of just the high side gate driver is shown in figure 31 (any selection of gate driver components should be the same for high side and low side drive); two extra components are seen, R_{DH} and D_H. With the careful selection of R_{GH} and R_{DH}, it is possible to selectively control the rise time and fall time of the gate drive. For turn on, all current will go from the IC through R_{GH} and charge the MOSFET gate capacitor, hence increasing or decreasing R_{GH} will increase or decrease rise time in the application. With the addition of D_H, the fall time can be separately controlled as the turn offf current flows from the MOSFET gate capacitor, through D_H and R_{DH} to the driver in the IC to VS. So increasing or decreasing R_{DH} will increase or decrease the fall time.

Increasing turn on and turn off has the effect of limiting ringing and noise due to parasitic inductances, hence with a noisy environment, it may be necessary to increase the gate resistors. For **gate resistor value selection** the exact value depends on the type of application and desired level of noise and ringing expected. Generally, power supplies switch at a fast speed, and want to squeeze out efficiency of the MOSFETs, so lower values are recommended, for example RGH = 5Ω - 20Ω. For motors, the switching speed is generally slower, and the application has more inherent noise, so higher values are recommended, for example RGH = 20Ω - 100Ω.

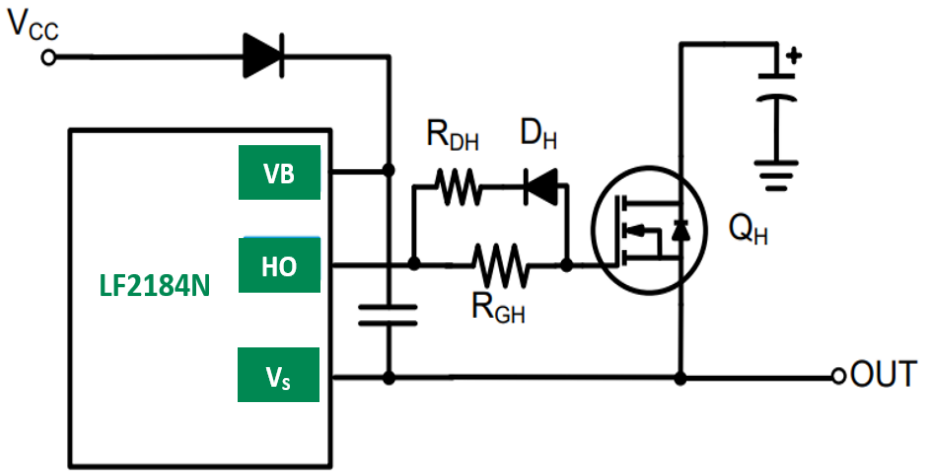


Figure 31. Gate Drive Control

4.4 Layout Considerations

Layout plays a considerable role in noise and ringing in a circuit; unwanted noise coupling, unpredicted glitches and abnormal operation could arise due to poor layout of the associated components. Figure 32 shows a halfbridge schematic with parasitic inductances in the high current path (L_{P1}, L_{P2}, L_{P3}, L_{P4}) which would be caused by inductance in the metal of the trace. Considering fig. 32, the length of the tracks in red should be minimized, and the bootstrap capacitor (C_B) and the decoupling capacitor (C_D) should be placed as close to the IC as possible. Low ESR ceramic capacitors should be used to minimize inductance.

And finally the gate resistors (R_{GH} and R_{GL}) and the sense resistor (R_S) should be surface mount devices. These suggestions will reduce the parasitics due to the PCB traces.

Generally, for the **decoupling capacitor** on VCC, at least one low ESR capacitor is recommended with it close to the device as possible. Recommended values are 1µF to 10µF. A second smaller decoupling capacitor is sometimes added to provide better high frequency response (for example 0.1µF).

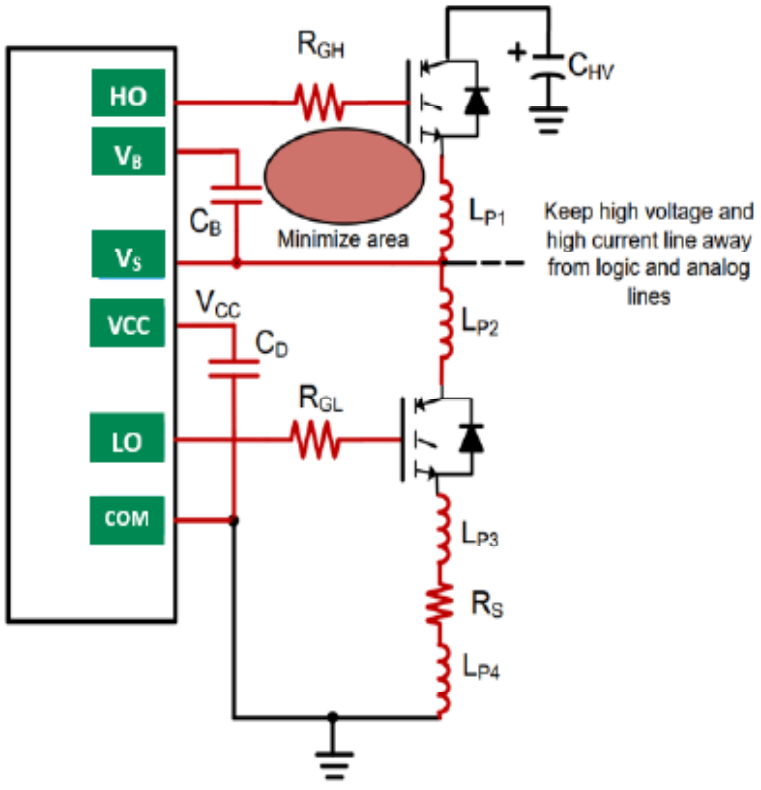


Figure 32. Layout Suggestions for LF2184N in a halfbridge

4.5 Application Example

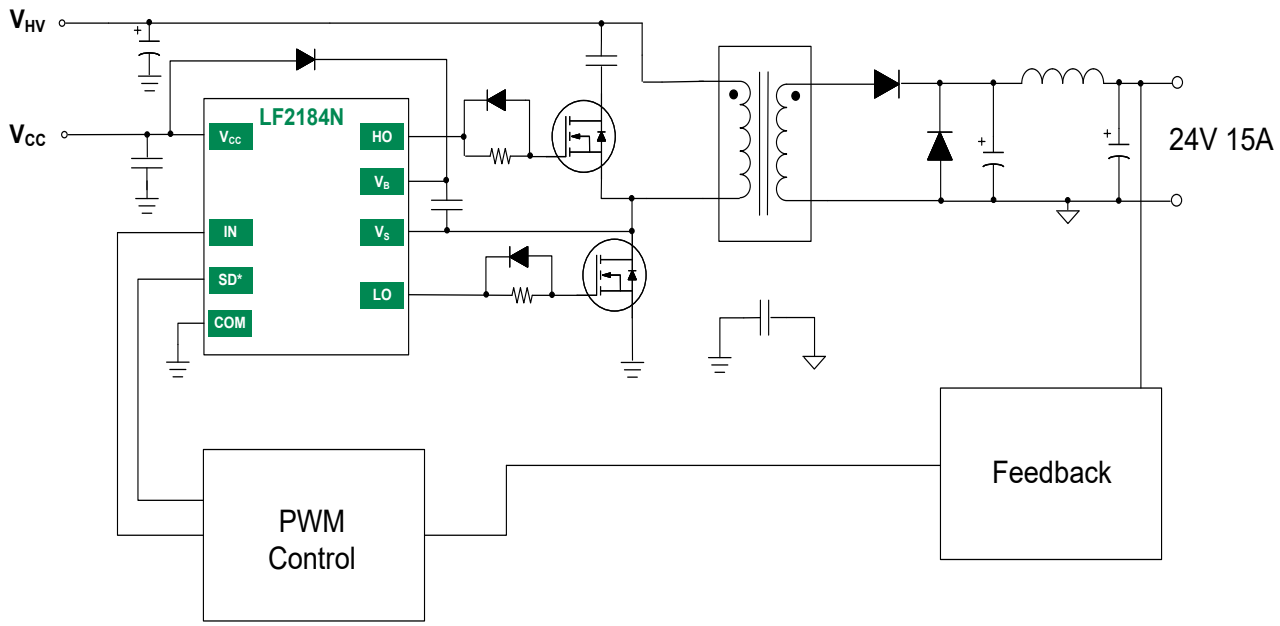


Figure 33. 360W Active Clamp Forward Converter using LF2184N

5 Manufacturing Information

5.1 Moisture Sensitivity

All plastic encapsulated semiconductor packages are susceptible to moisture ingression. Littelfuse Integrated Circuits Division classified all of its plastic encapsulated devices for moisture sensitivity according to the latest version of the joint industry standard, **IPC/JEDEC J-STD-020**, in force at the time of product evaluation. We test all of our products to the maximum conditions set forth in the standard, and guarantee proper operation of our devices when handled according to the limitations and information in that standard as well as to any limitations set forth in the information or standards referenced below.

Failure to adhere to the warnings or limitations as established by the listed specifications could result in reduced product performance, reduction of operable life, and/or reduction of overall reliability.

This product carries a **Moisture Sensitivity Level (MSL)** rating as shown below, and should be handled according to the requirements of the latest version of the joint industry standard **IPC/JEDEC J-STD-033.**

Device	Moisture Sensitivity Level (MSL) Classification
LF2184N	MSL3

5.2 ESD Sensitivity

This product is **ESD Sensitive**, and should be handled according to the industry standard **JESD-625**.

5.3 Reflow Profile

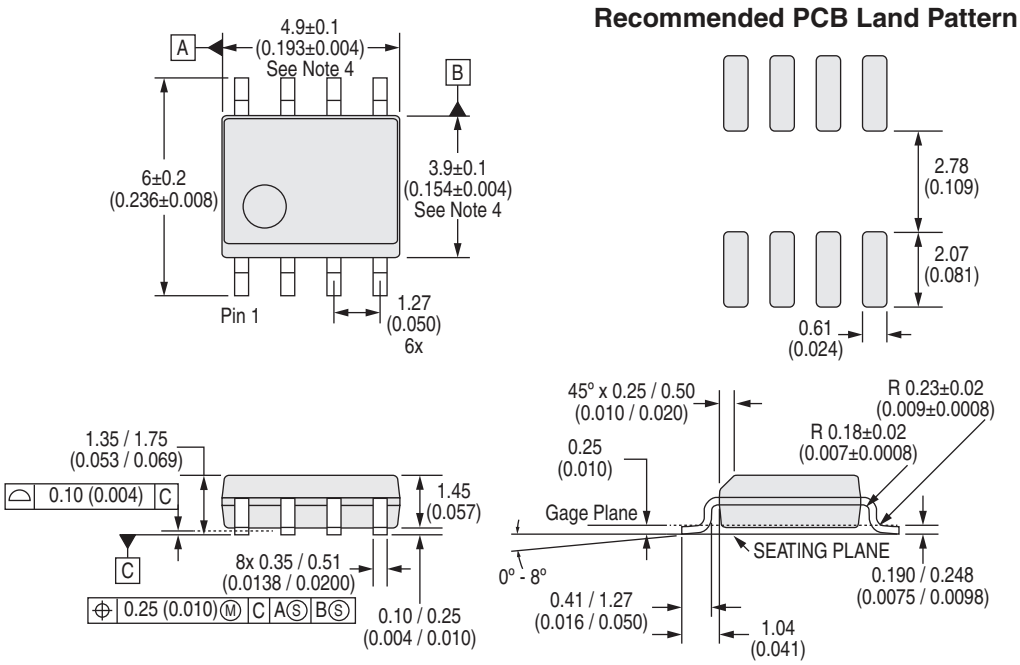
Provided in the table below is the IPC/JEDEC J-STD-020 Classification Temperature (T_C) and the maximum dwell time the body temperature of these surface mount devices may be (T_C - 5)°C or greater. The Classification Temperature sets the Maximum Body Temperature allowed for these devices during reflow soldering processes.

Device	Classification Temperature(Tc)	Dwell Time (tp)	Max Reflow Cycles
LF2184N	260°C	30 seconds	3

5.4 Board Wash

Littelfuse recommends the use of no-clean flux formulations. Board washing to reduce or remove flux residue following the solder reflow process is acceptable provided proper precautions are taken to prevent damage to the device. These precautions include but are not limited to: using a low pressure wash and providing a follow up bake cycle sufficient to remove any moisture trapped within the device due to the washing process. Due to the variability of the wash parameters used to clean the board, determination of the bake temperature and duration necessary to remove the moisture trapped within the package is the responsibility of the user (assembler). Cleaning or drying methods that employ ultrasonic energy may damage the device and should not be used. Additionally, the device must not be exposed to halide flux or solvents.

6 Package Dimensions SOIC(N)-8



Notes: (Unless otherwise specified)
1. Controlling dimension: millimeters.
2. All dimensions are in mm (inches).
3. Reference JEDEC registration MS-012, variation AA.
4. Not including mold flash, protrusion, or gate burrs
   0.15 (0.006) maximum per end.

Dimensions:
Minimum / Maximum

Important Notice

Disclaimer Notice - Information furnished is believed to be accurate and reliable. However, users should independently evaluate the suitability of and test each product selected for their own applications. Littelfuse products are not designed for, and may not be used in, all applications. Read complete Disclaimer Notice at **https://www.littelfuse.com/disclaimer-electronics**.

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