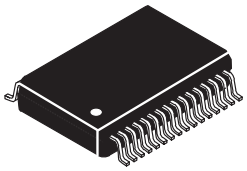
16 Output Switch with SPI Control

33996

LOW SIDE SWITCH

The 33996 is a 16-output low side switch with a 24-bit serial input control. It is designed for a variety of applications including inductive, incandescent, and LED loads. The Serial Peripheral Interface (SPI) provides both input control and diagnostic readout. A Pulse Width Modulation (PWM) control input is provided for pulse width modulation of multiple outputs at the same duty cycle. A dedicated reset input provides the ability to clear all internal registers and turn all outputs off.

The 33996 directly interfaces with micro controllers and is compatible with both 3.3 and 5.0V CMOS logic levels. The 33996, in effect, serves as a bus expander and buffer with fault management features that reduce the MCU's fault management burden.



EK SUFFIX (PB-FREE)
98ARL10543D
32-PIN SOICW EXPOSED PAD

Features

- Designed to operate 5.0V ≤ V_{PWR} ≤ 27V
- 24 Bit SPI for control and fault reporting, 3.3/5.0V compatible
- Outputs are current limited (0.9 to 2.5A) to drive incandescent lamps
- Output voltage clamp of +50V during inductive switching
- On/Off control of open load detect current (LED application)
- V_{PWR} standby current < 10µA
- $R_{DS(ON)}$ of 0.55Ω at 25°C typical
- Independent over-temperature protection
- Output selectable for PWM control
- Output ON short-to-V_{BAT} and off short-to-ground/open detection
- Pb-free packaging designated by suffix code EK

ORDERING INFORMATION

Device	Temperature Range (T_A)	Package
MC33996EK/R2	-40°C to 125°C	32 SOICW-EP
MCZ33996EK/R2		

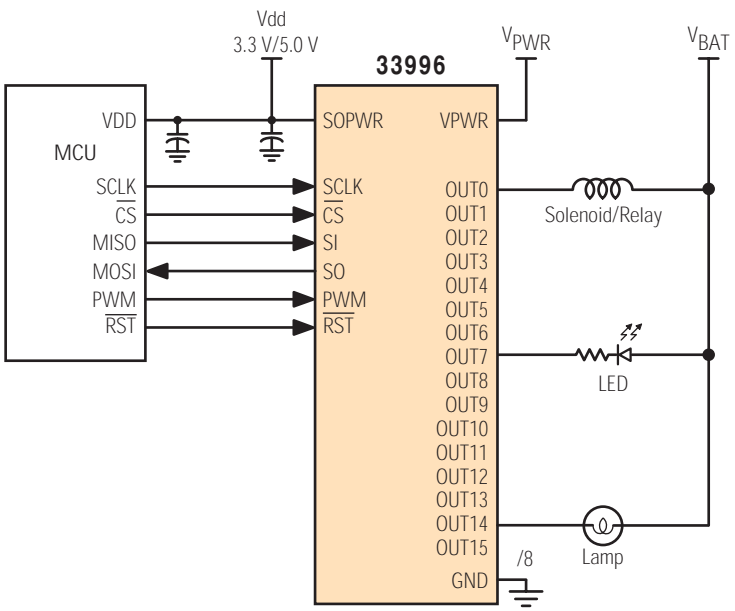


Figure 1. 33996 Simplified Application Diagram

* This document contains certain information on a new product.
Specifications and information herein are subject to change without notice.

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sales@prom-elec.com / ООО ПРОМЭЛЕКТРОНИКА

IINTERNAL BLOCK DIAGRAM

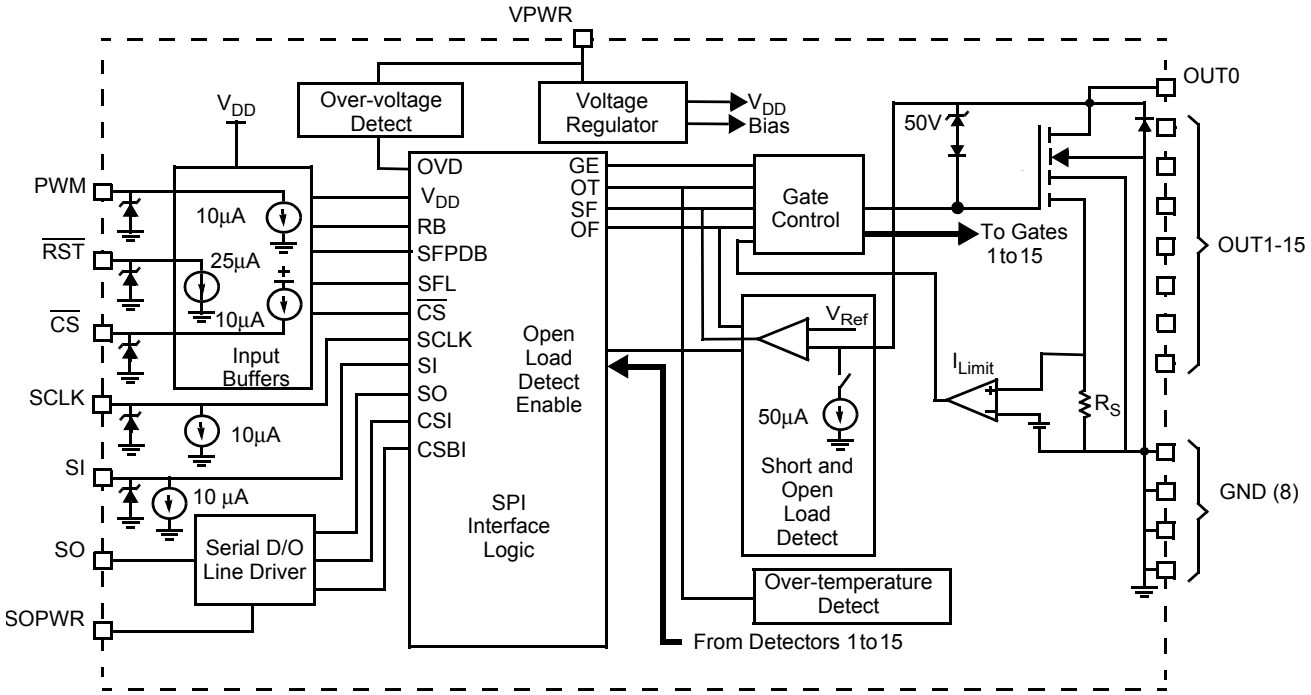


Figure 2. 33996 Simplified Internal Block Diagram

PIN CONNECTIONS

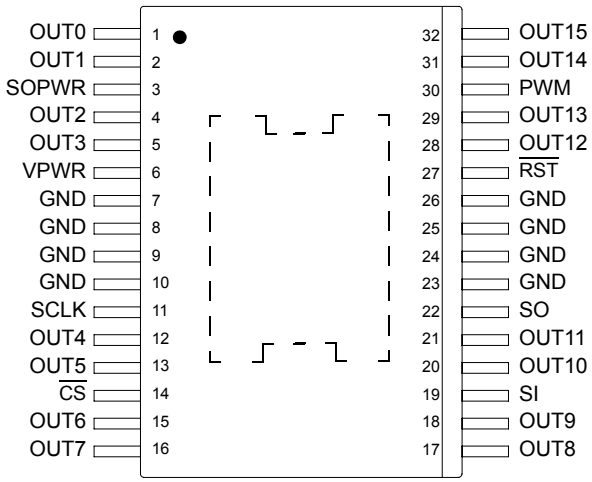


Figure 3. 33996 Pin Locations

Table 1. Pin Definitions

A functional description of each pin can be found in the Functional Pin Description section beginning on page 10.

Pin	Pin Name	Formal Name	Definition
1, 2, 4, 5, 12, 13, 15–18, 20, 21, 28, 29, 31, 32	OUT0–OUT15	Output 0–Output 15	Open drain output pin.
3	SOPWR	SO_{PWR} Supply	Power supply pin to the SO output driver.
6	VPWR	Battery Input	Battery supply input pin.
7–10, 23–26	GND	Ground	Ground for logic, analog, and power output devices.
11	SCLK	System Clock	System Clock for internal shift registers of the 33996.
14	$\overline{CS}$	Chip Select	SPI control chip select input pin from the MCU to the 33996.
19	SI	Serial Input	Serial data input pin to the 33996.
22	SO	Serial Output	Serial data output pin.
27	$\overline{RST}$	Reset	Active low reset input pin.
30	PWM	PWM Control	PWM control input pin. Supports PWM on any combination of outputs.
33	EP	Exposed Pad	Device will perform as specified with the Exposed Pad un-terminated (floating) however, it is recommended that the Exposed Pad be terminated to system ground.

ELECTRICAL CHARACTERISTICS

MAXIMUM RATINGS

Table 2. Maximum Ratings

All voltages are with respect to ground unless otherwise noted.

Rating	Symbol	Value	Unit
ELECTRICAL RATINGS			
VPWR Supply Voltage [1]	V_{PWR}	-1.5 to 50	V
SO Output Driver Power Supply Voltage [1]	SO_{PWR}	-0.3 to 7.0	V
SPI Interface Logic Input Voltage ($\overline{CS}$, PWM, SI, SO, SCLK, $\overline{RST}$) [1]	V_{IN}	-0.3 to 7.0	V
Output Drain Voltage	V_D	-0.3 to 45	V
Frequency of SPI Operation [2]	f_{SPI}	6.0	MHz
Output Clamp Energy [3]	E_{CLAMP}	50	mJ
ESD Voltage [4]			V
Human Body Model	V_{ESD1}	±2000	
Machine Model	V_{ESD2}	±200	
THERMAL RATINGS			
Operating Temperature			°C
Ambient	T_A	-40 to 125	
Junction	T_J	-40 to 150	
Case	T_C	-40 to 125	
Storage Temperature	T_{STG}	-55 to 150	°C
Power Dissipation (T_A = 25°C) [5]	P_D	1.7	W
Peak Package Reflow Temperature During Reflow [6], [7]	T_{PPRT}	Note 7	°C
Thermal Resistance			°C/W
Junction-to-Ambient [8]	$R_{\theta JA}$	75	
Junction- to-Lead [9]	$R_{\theta JL}$	8.0	
Junction-to-Flag	$R_{\theta JC}$	1.2	

Notes

1. Exceeding these limits may cause malfunction or permanent damage to the device.
2. This parameter is guaranteed by design but not production tested.
3. Maximum output clamp energy capability at 150°C junction temperature using single nonrepetitive pulse method.
4. ESD data available upon request. ESD testing is performed in accordance with the Human Body Model (C_{ZAP} = 100pF, R_{ZAP} = 1500Ω) and the Machine Model (C_{ZAP} = 200pF, R_{ZAP} = 0Ω).
5. Maximum power dissipation with no heat sink used.
6. Pin soldering temperature limit is for 10 seconds maximum duration. Not designed for immersion soldering. Exceeding these limits may cause malfunction or permanent damage to the device.
7. Freescale's Package Reflow capability meets Pb-free requirements for JEDEC standard J-STD-020C. For Peak Package Reflow Temperature and Moisture Sensitivity Levels (MSL), Go to www.freescale.com, search by part number [e.g. remove prefixes/suffixes and enter the core ID to view all orderable parts. (i.e. MC33xxxD enter 33xxx), and review parametrics.
8. Tested per JEDEC test JESD52-2 (single-layer PWB).
9. Tested per JEDEC test JESD51-8 (two-layer PWB).

STATIC ELECTRICAL CHARACTERISTICS

Table 3. STATIC ELECTRICAL CHARACTERISTICS

Characteristics noted under conditions 3.1V ≤ SO_{PWR} ≤ 5.5V, 5.0V ≤ V_{PWR} ≤ 18V, -40°C ≤ T_A ≤ 125°C unless otherwise noted. Where applicable, typical values noted reflect the parameter 's approximate value with V_{PWR} = 13V, T_A = 25°C.

Characteristic	Symbol	Min	Typ	Max	Unit
POWER SUPPLY (VPWR)					
Supply Voltage Range Fully Operational	$V_{PWR(FO)}$	5.0	–	27	V
Supply Current All Outputs ON, I_{OUT} = 0.3A	$I_{PWR(ON)}$	–	4.0	8.0	mA
Sleep State Supply Current at $\overline{RST}$ ≤ 0.8 and/or SO_{PWR} ≤ 1.5V	$I_{PWR(SS)}$	–	1.0	10	µA
Over-voltage Shutdown	V_{OV}	27.5	31.5	35	V
Over-voltage Shutdown Hysteresis	$V_{OV(HYS)}$	0.6	1.4	2.3	V
VPWR Under-voltage Shutdown	$V_{PWR(UV)}$	–	3.2	4.0	V
SPI Interface Logic Supply Voltage	SO_{PWR}	3.1	–	5.5	V
SPI Interface Logic Supply Current ($\overline{RST}$ Pin High)	$I_{SOPWR(\overline{RST}H)}$	100	–	500	µA
SPI Interface Logic Supply Current ($\overline{RST}$ Pin Low)	$I_{SOPWR(\overline{RST}L)}$	-10	–	10	µA
SPI Interface Logic Supply Under-voltage Lockout Threshold	$SO_{PWR(UNVOL)}$	1.5	2.5	3.0	V
POWER OUTPUT (VPWR)					
Drain-to-Source ON Resistance (I_{OUT} = 0.35A, V_{PWR} = 13V) T_J = 125°C T_J = 25°C T_J = -40°C	$R_{DS(ON)}$	 – – –	 0.75 0.55 0.45	 1.1 – –	Ω
Output Self-Limiting Current Outputs Programmed ON	$I_{OUT(lim)}$	0.9	1.2	2.5	A
Output Fault Detect Threshold [10] Outputs Programmed OFF	$V_{OUTth(F)}$	2.5	3.0	3.5	V
Output Off Open Load Detect Current [11] Outputs Programmed OFF (V_{PWR} = 5.0V, 13V, 18V)	I_{OCO}	25	50	100	µA
Output Clamp Voltage I_{OUT} = 20mA	V_{CL}	45	50	55	V
Output Leakage Current SO_{PWR} ≤ 1.5V, V_{OUT} 1-16 = 18V	$I_{OUT(lkg)}$	-10	2.0	10	µA
Over-temperature Shutdown (Outputs OFF) [12]	T_{LIM}	155	165	180	°C
Over-temperature Shutdown Hysteresis [12]	$T_{LIM(hys)}$	5.0	10	20	°C

Notes

10. Output Fault Detect Thresholds with outputs programmed OFF. Output Fault Detect Thresholds are the same for output open and shorts.
11. Output OFF Open Load Detect Current is the current required to flow through the load for the purpose of detecting the existence of an open load condition when the specific output is commanded to be OFF.
12. This parameter is guaranteed by design; however, it is not production tested.

Table 3. STATIC ELECTRICAL CHARACTERISTICS

Characteristics noted under conditions 3.1V ≤ SO_{PWR} ≤ 5.5V, 5.0V ≤ V_{PWR} ≤ 18V, -40°C ≤ T_A ≤ 125°C unless otherwise noted. Where applicable, typical values noted reflect the parameter 's approximate value with V_{PWR} = 13V, T_A = 25°C.

Characteristic	Symbol	Min	Typ	Max	Unit
DIGITAL INTERFACE ($\overline{RST}$, SI, $\overline{CS}$, SCLK, SO, PWM)					
Input Logic Voltage Thresholds [13]	$V_{INLOGIC}$	0.8	–	2.2	V
Input Logic Voltage Thresholds for $\overline{RST}$	$V_{IN\overline{RST}}$	0.8	–	2.2	V
SI Pull-down Current SI = 5.0 V	I_{SI}	2.0	10	30	µA
$\overline{CS}$ Pull-up Current $\overline{CS}$ = 0 V	$I_{\overline{CS}}$	-30	-10	-2.0	µA
SCLK Pull-down Current SCLK = 5.0 V	I_{SCLK}	2.0	10	30	µA
$\overline{RST}$ Pull-down Current $\overline{RST}$ = 5.0 V	$I_{\overline{RST}}$	5.0	25	50	µA
PWM Pull-down Current	I_{PWM}	2.0	10	30	µA
SO High State Output Voltage $I_{SO\text{-}high}$ = -1.6 mA	V_{SOH}	SO_{PWR} - 0.4	SO_{PWR} - 0.2	–	V
SO Low State Output Voltage $I_{SO\text{-}low}$ = 1.6 mA	V_{SOL}	–	–	0.4	V
Input Capacitance on SCLK, SI, Tri-State SO, $\overline{RST}$ [14]	C_{IN}	–	–	20	pF

Notes
13. Upper and lower logic threshold voltage levels apply to SI, $\overline{CS}$, SCLK, and PWM.
14. This parameter is guaranteed by design; however, it is not production tested.

DYNAMIC ELECTRICAL CHARACTERISTICS

Table 4. DYNAMIC ELECTRICAL CHARACTERISTICS

Characteristics noted under conditions of 3.1 V ≤ SO_{PWR} ≤ 5.5 V, 5.0 V ≤ V_{PWR} ≤ 18 V, -40°C ≤ T_A ≤ 125°C unless otherwise noted. Where applicable, typical values reflect the parameter's approximate average value with V_{PWR} = 13 V, T_A = 25°C.

Characteristic	Symbol	Min	Typ	Max	Unit
POWER OUTPUT TIMING (VPWR)					
Output Slew Rate R_L = 60Ω [15]	SR	1.0	2.0	10	V/µs
Output Turn ON Delay Time [16]	$t_{DLY(ON)}$	1.0	2.0	10	µs
Output Turn OFF Delay Time [16]	$t_{DLY(OFF)}$	1.0	4.0	10	µs
Output ON Short Fault Disable Report Delay [17]	$t_{DLY(SHORT)}$	100	–	450	µs
Output OFF Open Fault Delay Time [17]	$t_{DLY(OPEN)}$	100	–	450	µs
Output PWM Frequency	t_{FREQ}	–	–	2.0	kHz
DIGITAL INTERFACE TIMING ($\overline{CS}$, SO, SI, SCLK) [23]					
Required Low State Duration on V_{PWR} for Reset V_{PWR} ≤ 0.2V [18]	$t_{\overline{RST}}$	–	–	10	µs
Falling Edge of $\overline{CS}$ to Rising Edge of SCLK Required Setup Time	t_{LEAD}	100	–	–	ns
Falling Edge of SCLK to Rising Edge of $\overline{CS}$ Required Setup Time	t_{LAG}	50	–	–	ns
SI to Falling Edge of SCLK Required Setup Time	$t_{SI(su)}$	16	–	–	ns
Falling Edge of SCLK to SI Required Hold Time	$t_{SI(hold)}$	20	–	–	ns
SI, $\overline{CS}$, SCLK Signal Rise Time [19]	$t_{R(SI)}$	–	5.0	–	ns
SI, $\overline{CS}$, SCLK Signal Fall Time [19]	$t_{F(SI)}$	–	5.0	–	ns
Time from Falling Edge of $\overline{CS}$ to SO Low-impedance [20]	$t_{SO(EN)}$	–	–	50	ns
Time from Rising Edge of $\overline{CS}$ to SO High-impedance [21]	$t_{SO(DIS)}$	–	–	50	ns
Time from Rising Edge of SCLK to SO Data Valid [22]	t_{VALID}	–	25	80	ns

Notes
15. Output slew rate measured across a 60Ω resistive load.
16. Output turn ON and OFF delay time measured from 50% rising edge of $\overline{CS}$ to 80% and 20% of initial voltage.
17. Duration of fault before fault bit is set. Duration between access times must be greater than 450µs to read faults.
18. This parameter is guaranteed by design; however, it is not production tested.
19. Rise and Fall time of incoming SI, $\overline{CS}$, and SCLK signals suggested for design consideration to prevent the occurrence of double pulsing.
20. Time required for valid output status data to be available on SO pin.
21. Time required for output states data to be terminated at SO pin.
22. Time required to obtain valid data out from SO following the rise of SCLK with 200pF load.
23. This parameter is guaranteed by design. Production test equipment used 4.16MHz, 5.5/3.1V SPI Interface.

TIMING DIAGRAM

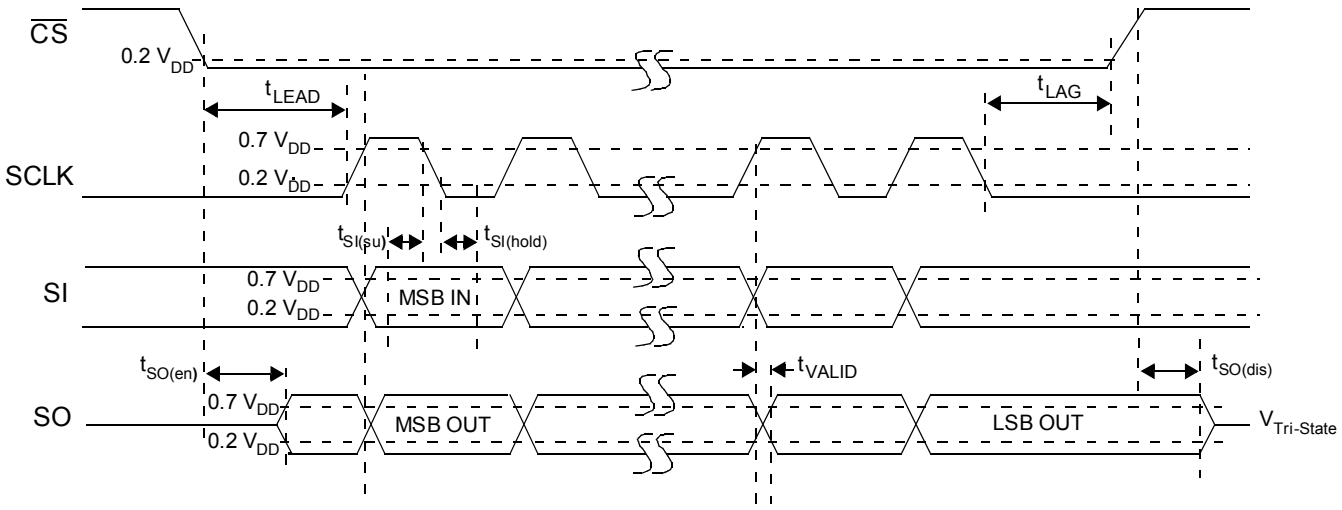


Figure 4. SPI Timing Characteristics

ELECTRICAL PERFORMANCE CURVES

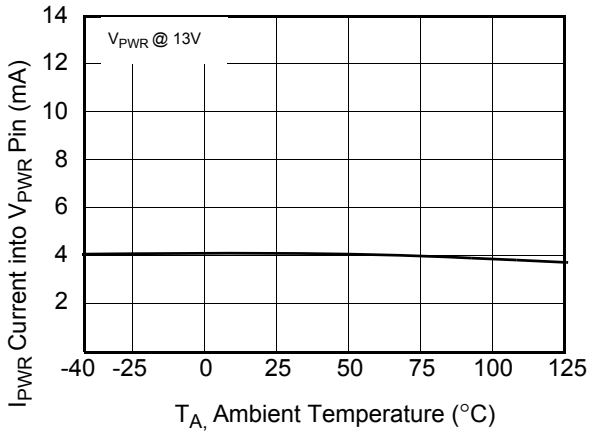


Figure 5. I_{PWR} vs. Temperature

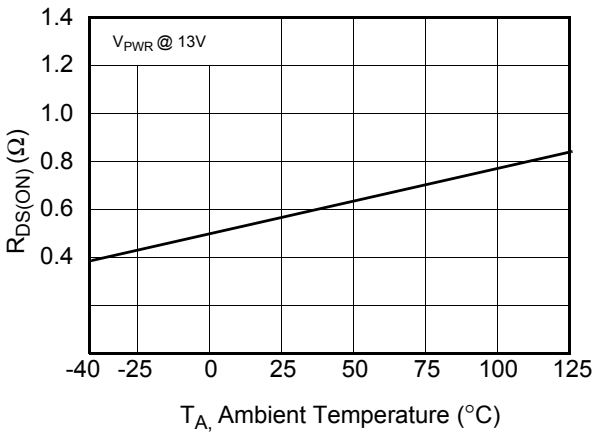


Figure 7. $R_{DS(ON)}$ vs. Temperature

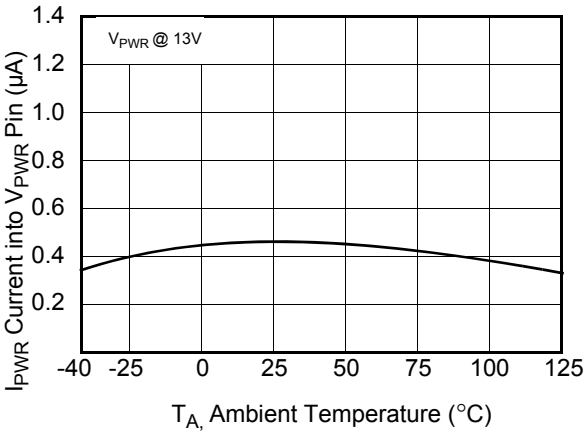


Figure 6. Sleep State I_{PWR} vs. Temperature

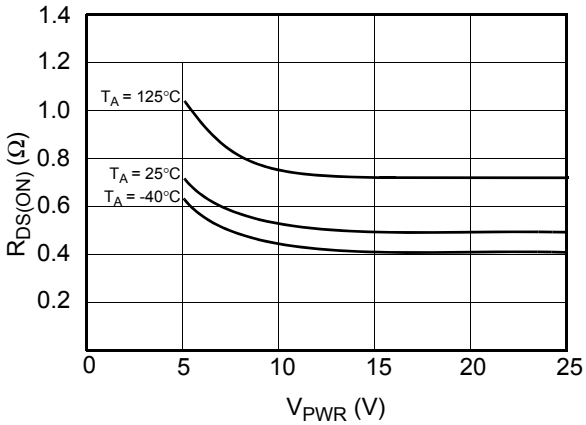


Figure 8. $R_{DS(ON)}$ vs. V_{PWR}

FUNCTIONAL DESCRIPTION

The 33996 is designed and developed for automotive and industrial applications. It is a 16 output power switch having 24 bit serial control. The 33996 incorporates SMARTMOS technology having CMOS logic, bipolar/MOS analog circuitry, and independent DMOS power output transistors. Many benefits are realized as a direct result of using this mixed technology. A simplified internal block diagram of the 33996 is shown in Figure 2, page 2.

FUNCTIONAL PIN DESCRIPTION

CHIP SELECT ($\overline{CS}$)

The system MCU selects the 33996 to be communicated with through the use of the Chip Select ($\overline{CS}$) pin. When the $\overline{CS}$ pin is in a logic low state, data can be transferred from the MCU to the 33996 and vise versa. Clocked-in data from the MCU is transferred from the 33996 Shift register and latched into the power outputs on the rising edge of the $\overline{CS}$ signal. On the falling edge of the $\overline{CS}$ signal, output fault status information is transferred from the Power Outputs Status register into the device's SO Shift register. The SO pin output driver is enabled when $\overline{CS}$ is low, allowing information to be transferred from the 33996 to the MCU. To avoid any spurious data, it is essential the high-to-low transition of the $\overline{CS}$ signal occur only when SCLK is in a logic low state.

SYSTEM CLOCK (SCLK)

The System Clock (SCLK) pin clocks the Internal Shift registers of the 33996. The Serial Input (SI) pin accepts data into the Input Shift register on the falling edge of the SCLK signal, while the Serial Output (SO) pin shifts data information out of the Shift register on the rising edge of the SCLK signal. False clocking of the Shift register must be avoided, ensuring validity of data. It is essential that the SCLK pin be in a logic low state whenever the $\overline{CS}$ pin makes any transition. For this reason, it is recommended, though not necessary, that the SCLK pin is commanded to a low logic state as long as the device is not accessed ($\overline{CS}$ in logic high state). When the $\overline{CS}$ is in a logic high state, any signal at the SCLK and SI pins is ignored and the SO is tri-stated (high impedance).

SERIAL INPUT (SI)

The Serial Input (SI) pin is used to enter one of seven serial instructions into the 33996. SI SPI bits are latched into the Input Shift register on each falling edge of SCLK. The Shift register is full after 24 bits of information are entered. The 33996 operates on the command word on the rising edge of $\overline{CS}$. To preserve data integrity, exercise care not to transition SI as SCLK transitions from high to low state (see Figure 4, page 8).

SERIAL OUTPUT (SO)

The Serial Output (SO) pin transfers fault status data from the 33996 to the MCU. The SO pin remains tri-state until the $\overline{CS}$ pin transitions to a logic low state. All faults on the 33996 are reported to the MCU as logic [1]. Conversely, normal operating outputs with nonfaulted loads are reported as logic [0]. On the falling edge of the $\overline{CS}$ signal, output fault status information is transferred from the Power Outputs Status register into the device's SO Shift register. The first eight positive transitions of SCLK will provide Any Fault (bit 23), over-voltage fault (bit 22), followed by six logic [0]s (bits 21 to 16). The next 16 successive positive transitions of SCLK provides fault status for output 15 to output 0. Refer to the LOGIC OPERATION section (below) for more information. The SI/SO shifting of data follows a first-in, first-out protocol, with both input and output words transferring the Most Significant Bit (MSB) first.

OUTPUT DRIVER POWER SUPPLY (SOPWR)

The SOPWR pin is used to supply power to the 33996 SO output driver and Power-ON Reset (POR) circuit. To achieve low standby current on VPWR supply, power must be removed from the SOPWR pin. The 33996 will be in reset with all drivers OFF when SO_{PWR} is below 2.5V. The 33996 does not detect over-voltage on the SOPWR supply pin.

OUTPUT/INPUT (OUT0–OUT15)

These pins are low side output switches controlling the load.

RESET ($\overline{RST}$)

The Reset ($\overline{RST}$) pin is the active low reset input pin used to turn OFF all outputs, thereby clearing all internal registers.

BATTERY INPUT (VPWR)

The VPWR pin is used as the input power source for the 33996. The voltage on VPWR is monitored for over-voltage protection and shutdown. An over-voltage condition (> 50µs) on the VPWR pin will cause the 33996 to shut down all outputs until the over-voltage condition is removed. Upon return to normal input voltage, the outputs will respond as programmed by the over-voltage bit in the Global Shutdown/Retry Control register. The over-voltage threshold on the VPWR pin is specified as 27.5 to 35 V with 1.4V typical hysteresis. Following an over-voltage shutdown of output drivers, the over-voltage Fault and the Any Fault bits in the SO bit stream will be logic [1].

PWM CONTROL (PWM)

The PWM Control pin is provided to support PWM of any combination of outputs. The LOGIC OPERATION section describes the logic for PWM control.

OPERATIONAL MODES

On each SPI communication, a 24 bit command word is sent to the 33996 and 24 bit fault word is received from the 33996. The Most Significant Bit (MSB) is sent and received first.

Command Register Definition:
0 = Output Command Off
1 = Output Command On

SO Definition:
0 = No fault
1 = Fault

Table 5. Fault Operation

Serial Output (SO) Pins Reports

Over-temperature	Fault reported by Serial Output (SO) pin.
Over-current	SO pin reports short to battery/supply or over-current condition.
Output “ON’ Open Load Fault	Not reported.
Output “OFF’” Open Load Fault	SO pin reports output “OFF’” open load condition.

Device Shutdowns

Over-voltage	Total device shutdown at V_{PWR} = 27.5 V to 35 V. Resumes normal operation with proper voltage. Upon recovery all outputs assume previous state or OFF based on the Overvoltage bit in the Global Shutdown/Retry Control Register.
Over-temperature	Only the output experiencing an over-temperature fault shuts down. Output may auto-retry or remain off according to the control bits in the Global Shutdown/Retry Control Register.
Over-current	Output will remain in current limit 0.9 A to 2.5 A until thermal limit is reached. When thermal limit is reached, device will enter over-temperature shutdown. Output will operate as programmed in the Global Shutdown/Retry Control Register. Fault flag in SO Response word will be set.

MCU INTERFACE DESCRIPTION

In operation the 33996 functions as a 16-output serial switch serving as a microcontroller (MCU) bus expander and buffer with fault management and fault reporting features. In doing so, the device directly relieves the MCU of the fault management functions.

The 33996 directly interfaces to an MCU and operates at system clock serial frequencies up to 6.0MHz using a Serial Peripheral Interface (SPI) for control and diagnostic readout.

Figure 9 shows the basic SPI configuration between an MCU and one 33996.

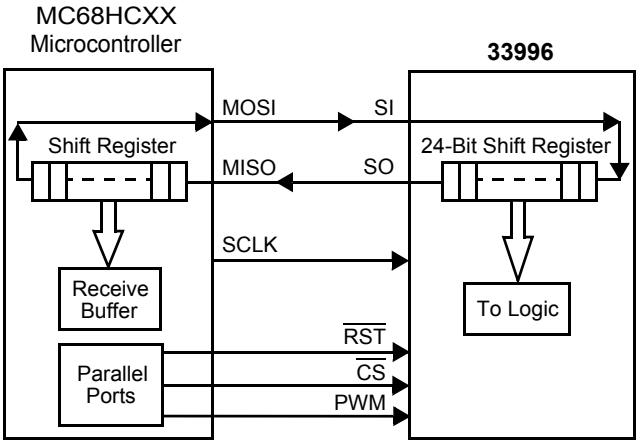


Figure 9. 33996 SPI Interface with Microcontroller

All inputs are compatible with 3.3/5.0V CMOS logic levels and incorporate positive logic. An input that is programmed to a logic low state (< 0.8V) will have the corresponding output OFF. Conversely, an input programmed to a logic high state (> 2.2V) will have the output being controlled ON.

Diagnostics is treated in a similar manner—outputs with a fault will feedback (via SO) to the MCU a logic [1], while normal operating outputs will provide a logic [0].

The 33996 may be controlled and provide diagnostics using a daisy chain configuration or in parallel mode. Figure 10 shows the daisy chain configuration using the 33996. Data from the MCU is clocked daisy chain through each device while the Chip Select bit ($\overline{CS}$) is commanded low by the MCU. During each clock cycle, output status from the daisy-chained 33996s is being transferred back to the MCU via the Master In Slave Out (MISO) line. On rising edge of $\overline{CS}$, data stored in the input register is transferred to the output driver. Daisy chain control of the 33996 requires 24 bits per device.

Multiple 33996 devices can be controlled in a parallel input fashion using the SPI. Figure 11, page 12, illustrates potentially 32 loads being controlled by two dedicated parallel MCU ports used for chip select.

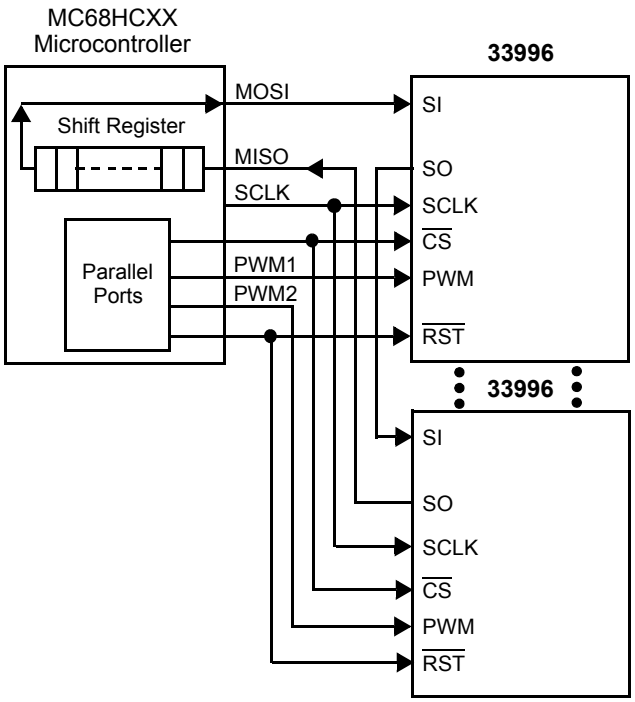


Figure 10. 33996 SPI System Daisy Chain

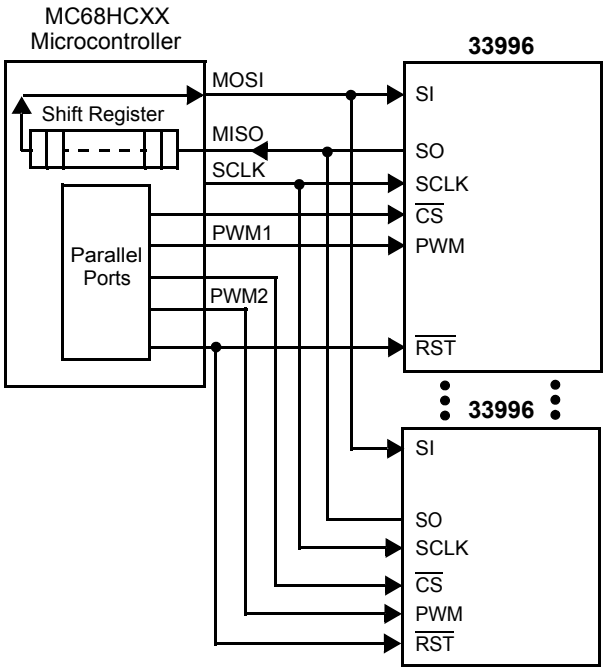


Figure 11. Parallel Inputs SPI Control

LOGIC COMMANDS AND REGISTERS

INTRODUCTION

The 33996 provides flexible control of 16 low-side driver outputs. The device allows PWM and ON/OFF control through the use of several 24 bit input command words. This section describes the logic operation and command registers of the 33996.

The 33996 message set consists of seven messages as shown in Table 6. Bits 23 through18 determine the specific command and bits 15 through 0 determine how a specific output will operate. The 33996 operates on the command word on the rising edge of $\overline{CS}$.

Note Upon Power-ON Reset all bits are defined as shown in Table 6.

Table 6. SPI Control Commands

	MSB																							LSB
									Bits															
Commands	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ON/OFF Control 0=off, 1=on	0	0	0	0	0	0	X	X	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Open Load Current Enable 0=disable, 1=enable	0	0	0	0	0	1	X	X	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Global Shutdown/Retry Control 0=shutdown, 1=retry	0	0	0	0	1	0	Thermal Bit 0	Over-voltage 0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
SFPD Control 1=therm only, 0=V_{DS}	0	0	0	0	1	1	X	X	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
PWM Enable 0=SPI only, 1=PWM	0	0	0	1	0	0	X	X	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
AND/OR Control 0=PWM pin AND with SPI 1=PWM pin OR with SPI	0	0	0	1	0	1	X	X	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Reset	0	0	0	1	1	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
SO Response 0=No Fault, 1=Fault	Any Fault	over-volt-age	0	0	0	0	0	0	OUT 15	OUT 14	OUT 13	OUT 12	OUT 11	OUT 10	OUT 9	OUT 8	OUT 7	OUT 6	OUT 5	OUT 4	OUT 3	OUT 2	OUT 1	OUT 0

ON/OFF CONTROL REGISTER

To program the 16 outputs of the 33996 ON or OFF, a 24 bit serial stream of data is entered into the SI pin. The first 8 bits of the control word are used to identify the on/off command and the remaining 16 bits are used to turn ON or OFF the specific output driver.

OPEN LOAD CURRENT ENABLE CONTROL REGISTER

The Open Load Current Enable Control register is provided to enable or disable the 50µA open load detect pull-down current. This feature allows the device to be used in LED applications. Power-ON Reset (POR) or the $\overline{RST}$ pin or the RESET command disables the 50µA pull-down current. No open load fault will be reported with the pull-down current disabled. For open load to be active, the user must program the Open Load Current Enable Control register with logic [1].

GLOBAL SHUTDOWN/RETRY CONTROL REGISTER

The Global Shutdown/Retry Control register allows the user to select the global fault strategy for the outputs. The over-voltage control bit (bit 16) sets the operation of the outputs when returning from over-voltage. Setting the over-voltage bit to logic [0] will force all outputs to remain off when V_{PWR} returns to normal level. Setting the over-voltage bit to logic [1] will command outputs to resume their previous state when V_{PWR} returns to normal level. Bit 17 is the global thermal bit. When bit 17 is set to logic [0], all outputs will shut down when thermal limit is reached and remain off even after cooled. With bit 17 set to logic [1], all outputs will shut down when thermal limit is reached and will retry when cooled.

SHORT FAULT PROTECT DISABLE (SFPD) CONTROL REGISTER

All outputs contain current limit and thermal shutdown with programmable retry. The SFPD control bits are used for fast shutdown of the output when over-current condition is detected but thermal shutdown has not been achieved.

The SFPD Control register allows the user to select specific outputs for incandescent lamp loads and specific outputs for inductive loads. By programming the specific SFPD bit as logic [1], output will rely on over-temperature shutdown only. Programming the specific SFPD bit as logic [0] will shut down the output after 100 to 450µs during turn on into short circuit. The decision for shutdown is based

on output drain-to-source voltage (V_{DS}) > 2.7V. This feature is designed to provide protection to loads that experience more than expected currents and require fast shutdown. The 33996 is designed to operate in both modes with full device protection.

PWM ENABLE REGISTER

The PWM Enable register determines the outputs that are PWM controlled. The first 8 bits of the 24 bit SPI message word are used to identify the PWM enable command, and the remaining 16 bits are used to enable and disable the PWM of the output drivers.

A logic [0] in the PWM Enable register will disable the outputs as PWM. A logic [1] in the PWM Enable register will set the specific output as a PWM. Power-ON Reset or the $\overline{RST}$ pin or the RESET command will set the PWM Enable register to logic [0].

AND/OR CONTROL REGISTER

The AND/OR Control register describes the condition by which the PWM pin controls the output driver. A logic [0] in the AND/OR Control register will AND the PWM input pin with the ON/OFF Control register bit. Likewise, a logic [1] in the AND/OR Control register will OR the PWM input pin with the ON/OFF Control register bit (see Figure 12). For the AND/OR control to occur, the PWM Enable bit must be set to logic [1].

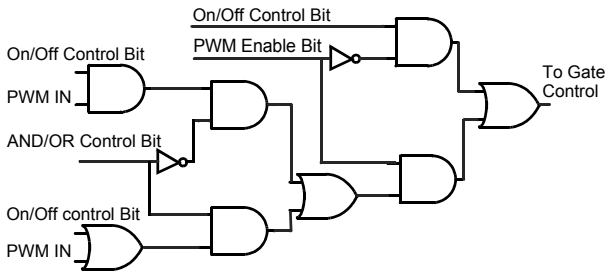


Figure 12. PWM Control Logic Diagram

SERIAL OUTPUT (SO) RESPONSE REGISTER

Fault reporting is accomplished through the SPI interface. All logic [1s] received by the MCU via the SO pin indicate fault. All logic [0s] received by the MCU via the SO pin indicate no fault. All fault bits are cleared on the positive edge of $\overline{CS}$. SO bits 15 to 0 represent the fault status of outputs 15 to 0. SO bits 21 to 16 will always return logic [0]. Bit 22 provides over-voltage condition status and bit 23 is set when any fault is present in the IC. The timing between two write words must be greater than 450µs to allow adequate time to sense and report the proper fault status.

RESET COMMAND

The RESET command turns all outputs OFF and sets the following registers to a POR state (refer to Table 6).

- ON/OFF Control Register
- SFPD Control Register
- PWM Enable Register
- AND/OR Control Register

The Open Load Current Enable and the Global Shutdown Registers are not affected by the RESET command.

TYPICAL APPLICATIONS

Power Consumption

The 33996 has been designed with one Sleep mode and one Operational mode. In Sleep mode ($SO_{PWR} \leq 2.0V$) the current consumed by the VPWR pin is less than 10µA. To place the 33996 in Sleep mode, turn all outputs OFF and remove power from the SOPWR pin. During normal operation, 500µA is drawn from the SO_{PWR} supply and 8.0mA from the V_{PWR} supply.

Paralleling of Outputs

Using MOSFETs as output switches allows the connection of any combination of outputs together. The $R_{DS(ON)}$ of MOSFETs has an inherent positive temperature coefficient, providing balanced current sharing between outputs without destructive operation. This mode of operation may be desirable in the event the application requires lower power dissipation or the added capability of switching higher currents. Performance of parallel operation results in a corresponding decrease in $R_{DS(ON)}$, while the Output Current Limit increases correspondingly. Output OFF Open Load Detect current may increase based on how the Output OFF Open Load Detect is programmed. Paralleling outputs from two or more different IC devices is possible but not recommended.

Care must be taken when paralleling outputs for inductive loads. The Output Voltage Clamp of the output drivers may not match. One MOSFET output must be capable of the inductive energy from the load turn OFF.

SPI Integrity Check

Checking the integrity of the SPI communication is recommended upon initial power-up of the SOPWR pin. After initial system start-up or reset, the MCU writes one 48-bit pattern to the 33996.

The first 24 bits read by the MCU is the fault status of the outputs, while the second 24 bits is the first bit pattern sent. By the MCU receiving the same bit pattern it sent, bus integrity is confirmed. Please note the second 24 bits the MCU sends to the 33996 are the command bits and will program registers or activate outputs on the rising edge of $\overline{CS}$.

Output OFF Open Load Fault

An Output OFF Open Load Fault is the detection and reporting of an *open* load when the corresponding output is disabled (input bit programmed to a logic low state). The Output OFF Open Load Fault is detected by comparing the drain-to-source voltage of the specific MOSFET output to an internally generated reference. Each output has one dedicated comparator for this purpose.

Each 33996 output has an internal 50µA pull-down current source. The pull-down current is disabled on power-up and must be enabled for Open Load Detect to function. Once enabled, the 33996 will only shut down the pull-down current in Sleep mode or when disabled via the SPI.

During output switching, especially with capacitive loads, a false Output OFF Open Load Fault may be triggered. To prevent this false fault from being reported, an internal fault filter of 100 to 450µs is incorporated. The duration for which a false fault may be reported is a function of the load impedance, $R_{DS(ON)}$, C_{OUT} of the MOSFET, as well as the supply voltage, V_{PWR}. The rising edge of $\overline{CS}$ triggers the built-in fault delay timer. The timer must time out before the fault comparator is enabled to detect a faulted threshold. Once the condition causing the Open Load Fault is removed, the device resumes normal operation. The Open Load Fault, however, will be latched in the output SO Response register for the MCU to read.

Shorted Load Fault

A shorted load (over-current) fault can be caused by any output being shorted directly to supply, or by an output experiencing a current greater than the current limit.

Three safety circuits progressively in operation during load short conditions afford system protection:

1. The device's output current is monitored in an analog fashion using a SENSEFET approach and is current limited.
2. With the output in current limit, the drain-to-source voltage will increase. By setting the SFPD bit to 0, the output will shut down on $V_{DS} > 2.7V$ typical after 450µs.
3. The device's output thermal limit is sensed and when attained causes only the specific faulted output to shutdown. The device remains OFF until cooled. The device then operates as programmed by the shutdown/retry bit. The cycle continues until the fault is removed or the command bit instructs the output OFF.

All three protection schemes set the Fault Status bit (bit 23 in the SO Response register) to logic [1].

Under-voltage Shutdown

An under voltage SO_{PWR} condition results in the global shutdown of all outputs and reset of all control registers. The under-voltage threshold is between 2.0 and 3.0V.

An under-voltage condition at the VPWR pin results in an output shutdown and reset. The under-voltage threshold is between 3.2 and 3.5V. When V_{PWR} is between 5.0 and 3.5V, the output may operate per the command word and the status is reported on SO pin, though this is not guaranteed.

Output Voltage Clamp

Each output of the 33996 incorporates an internal voltage clamp to provide fast turn-OFF and transient protection of each output. Each clamp independently limits the drain-to-source voltage to 50V. The total energy clamped (E_J) can be

calculated by multiplying the current area under the current curve (I_A) times the clamp voltage (V_{CL}) (see Figure 13).

Characterization of the output clamps, using a single pulse non-repetitive method at 0.3A, indicates the maximum energy to be 50mJ at 150°C junction temperature per output.

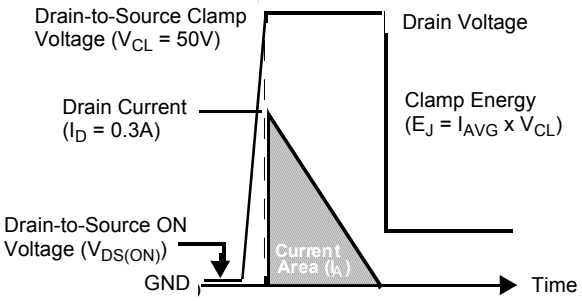


Figure 13. Output Voltage Clamping

Reverse Battery Protection

The 33996 device requires external reverse battery protection on the VPWR pin.

All outputs consist of a power MOSFET with an integral substrate diode. During reverse battery condition, current will flow through the load via the substrate diode. Under this circumstance relays may energize and lamps will turn on. If load reverse battery protection is desired, a diode must be placed in series with the load.

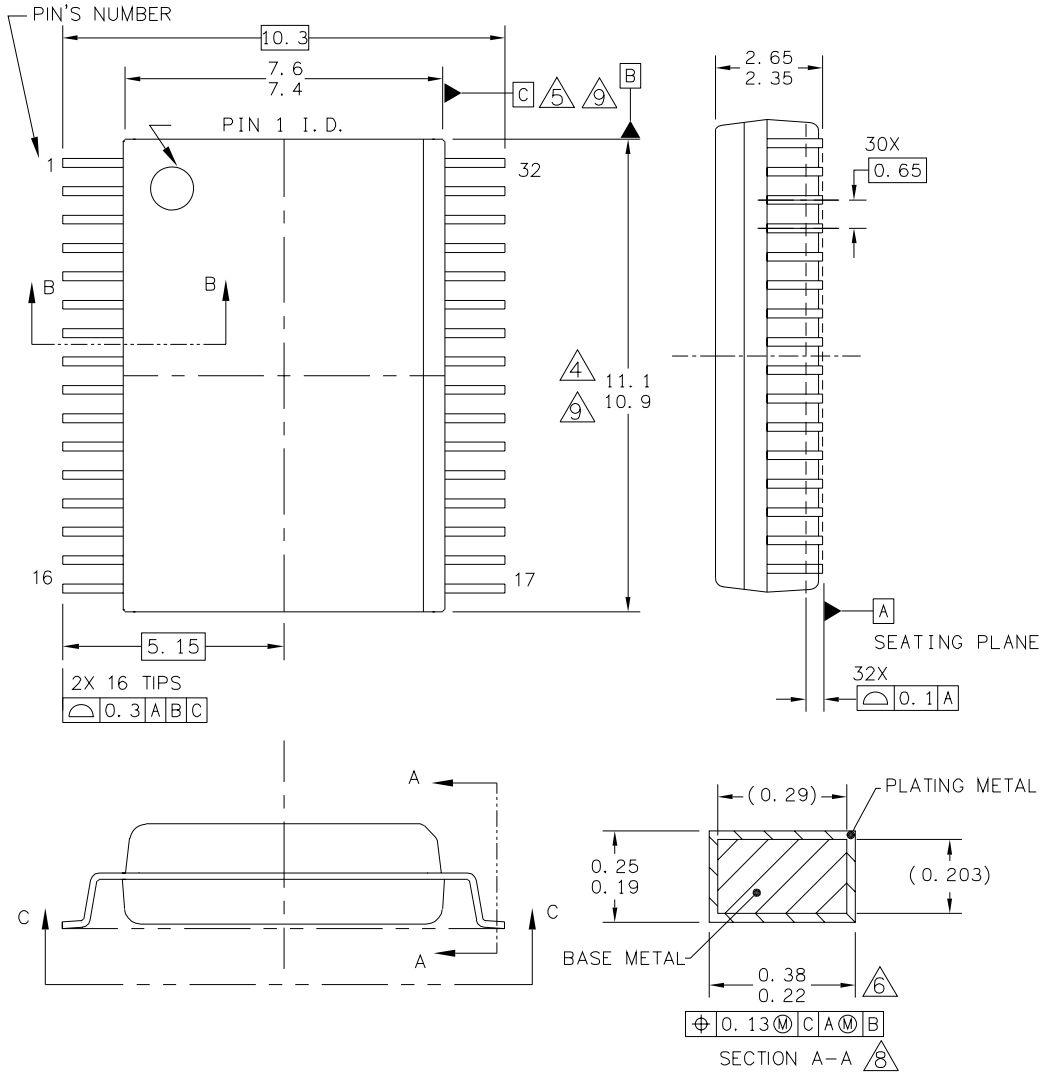
Over-temperature Fault

Over-temperature detect circuits are specifically incorporated for each individual output. The shutdown following an over temperature condition depends on the control bit set in the Global Shutdown/Retry Control register. Each independent output shuts down at 155°C to 180°C. When an output shuts down due to an Over-temperature Fault, no other outputs are affected. The MCU recognizes the fault by a logic [1] in the Fault Status bit (bit 23 in the SO Response register). After the 33996 has cooled below the switch point temperature and 10°C hysteresis, the output will function as defined by the shutdown/retry bit 17 in the Global Shutdown/Retry Control register.

PACKAGING

PACKAGE DIMENSIONS

Important: For the most current package revision, visit www.freescale.com and search on keyword for 98A number listed below.



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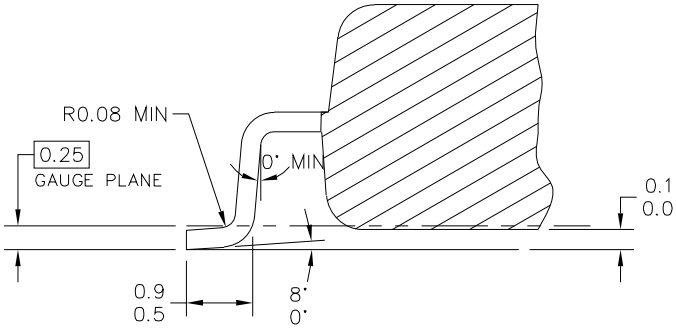
TITLE: 32LD SOIC W/B, 0.65 PITCH 5.7 X 4.6 EXPOSED PAD CASE OUTLINE	DOCUMENT NO: 98ARL10543D	REV: C
	CASE NUMBER: 1437–03	08 MAY 2008
	STANDARD: NON–JEDEC	

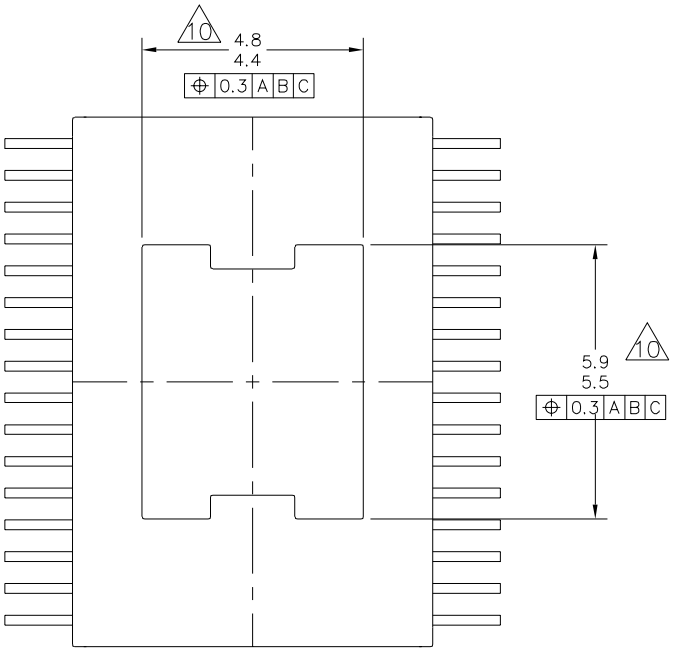
EK SUFFIX (PB-FREE)
32-PIN SOICW EP
98ARL10543D
REVISION C

33996

PACKAGE DIMENSIONS (CONTINUED)



SECTION B–B



VIEW C–C

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	CASE NUMBER: 1437-03	08 MAY 2008
	STANDARD: NON-JEDEC	

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NOTES:

1. DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994.
3. DATUMS B AND C TO BE DETERMINED AT THE PLANE WHERE THE BOTTOM OF THE LEADS EXIT THE PLASTIC BODY.
4. THIS DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURRS. MOLD FLASH, PROTRUSION OR GATE BURRS SHALL NOT EXCEED 0.15 MM PER SIDE. THIS DIMENSION IS DETERMINED AT THE PLANE WHERE THE BOTTOM OF THE LEADS EXIT THE PLASTIC BODY.
5. THIS DIMENSION DOES NOT INCLUDE INTER–LEAD FLASH OR PROTRUSIONS. INTER–LEAD FLASH AND PROTRUSIONS SHALL NOT EXCEED 0.25 MM PER SIDE. THIS DIMENSION IS DETERMINED AT THE PLANE WHERE THE BOTTOM OF THE LEADS EXIT THE PLASTIC BODY.
6. THIS DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 0.4 mm. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD SHALL NOT LESS THAN 0.07 mm.
7. EXACT SHAPE OF EACH CORNER IS OPTIONAL.
8. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10 mm AND 0.3 mm FROM THE LEAD TIP.
9. THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM. THIS DIMENSION IS DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, TIE BAR BURRS, GATE BURRS AND INTER–LEAD FLASH, BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.
10. THESE DIMENSIONS RANGES DEFINE THE PRIMARY KEEP–OUT AREA. MOLD LOCKING AND RESIN BLEED CONTROL FEATURES MAY BE VISIBLE AND THEY MAY EXTEND TO 0.9mm FROM MAXIMUM EXPOSED PAD SIZE

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	CASE NUMBER: 1437–03		08 MAY 2008
	STANDARD: NON–JEDEC		

EK SUFFIX (PB-FREE)
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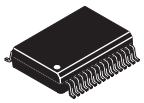
REVISION C

ADDITIONAL DOCUMENTATION

THERMAL ADDENDUM (REV 2.0)

33996EK

32-PIN SOICW-EP



EK (PB-FREE) SUFFIX
98ARL10543D
32-PIN SOICW-EP

Note For package dimensions, refer to the 33996 data sheet.

Introduction

This thermal addendum is provided as a supplement to the MC33996 technical datasheet. The addendum provides thermal performance information that may be critical in the design and development of system applications. All electrical, application, and packaging information is provided in the datasheet.

Packaging and Thermal Considerations

The MC33996 is offered in a 32 pin SOICW exposed pad, single die package. There is a single heat source (P), a single junction temperature (T_J), and thermal resistance ($R_{\theta JA}$).

$$\{ T_J \} = [R_{\theta JA}] \cdot \{ P \}$$

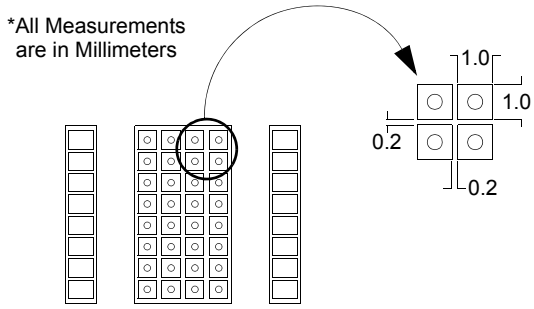
The stated values are solely for a thermal performance comparison of one package to another in a standardized environment. This methodology is not meant to and will not predict the performance of a package in an application-specific environment. Stated values were obtained by measurement and simulation according to the standards listed below.

Standards

Table 7. Thermal Performance Comparisons

Thermal Resistance	[°C/W]
$R_{\theta JA}$ (1), (2)	29
$R_{\theta JB}$ (2), (3)	9.0
$R_{\theta JA}$ (1), (4)	69
$R_{\theta JC}$ (5)	2.0

Notes:
1. Per JEDEC JESD51-2 at natural convection, still air condition.
2. 2s2p thermal test board per JEDEC JESD51-5 and JESD51-7.
3. Per JEDEC JESD51-8, with the board temperature on the center trace near the center lead.
4. Single layer thermal test board per JEDEC JESD51-3 and JESD51-5.
5. Thermal resistance between the die junction and the exposed pad surface; cold plate attached to the package bottom side, remaining surfaces insulated.



32 Pin SOICW-EP
0.65 Pitch
11.0 mm x 7.5mm Body
4.6 mm x 5.7 mm Exposed Pad

Figure 14. Surface Mount for SOICW Exposed Pad

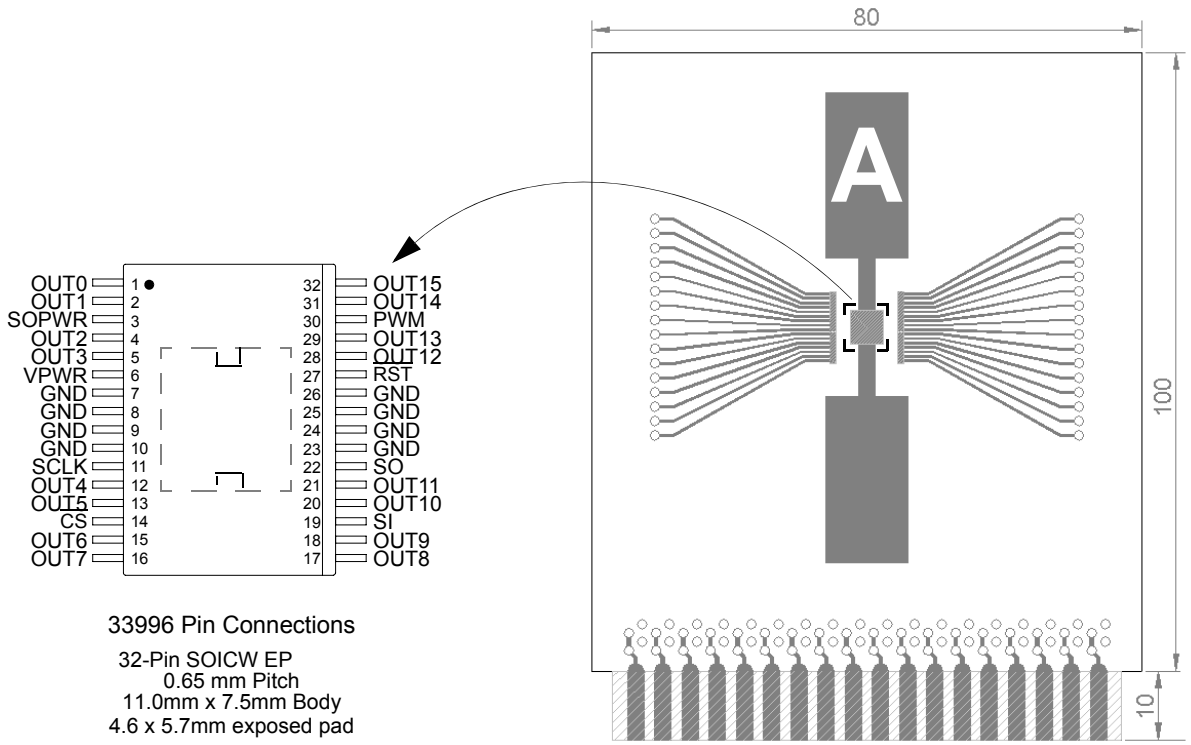


Figure 15. Thermal Test Board

Device on Thermal Test Board

Material:	Single layer printed circuit board FR4, 1.6mm thickness Cu traces, 0.07 mm thickness
Outline:	80 mm x 100mm board area, including edge connector for thermal testing
Area A:	Cu heat-spreading areas on board surface
Ambient Conditions:	Natural convection, still air

Table 8. Thermal Resistance Performance

A [mm^2]	$R_{\theta JA}$ [°C/W]
0	70
300	49
600	47

$R_{\theta JA}$ is the thermal resistance between die junction and ambient air.

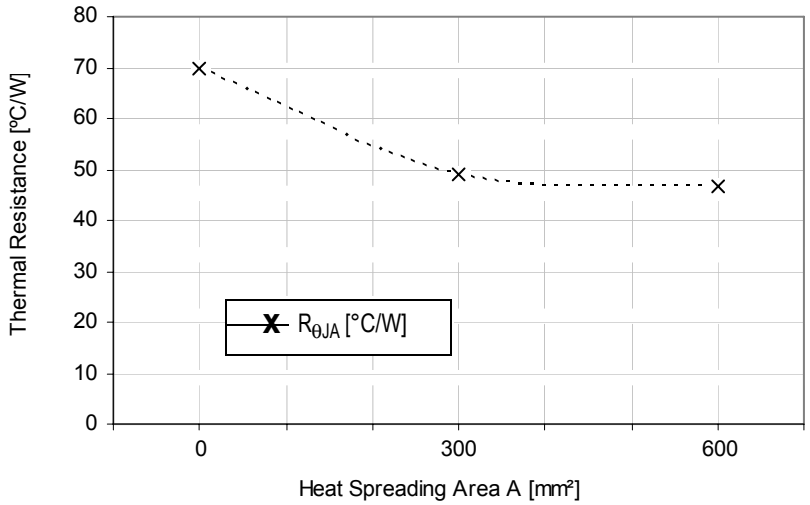


Figure 16. Device on Thermal Test Board $R_{\theta JA}$

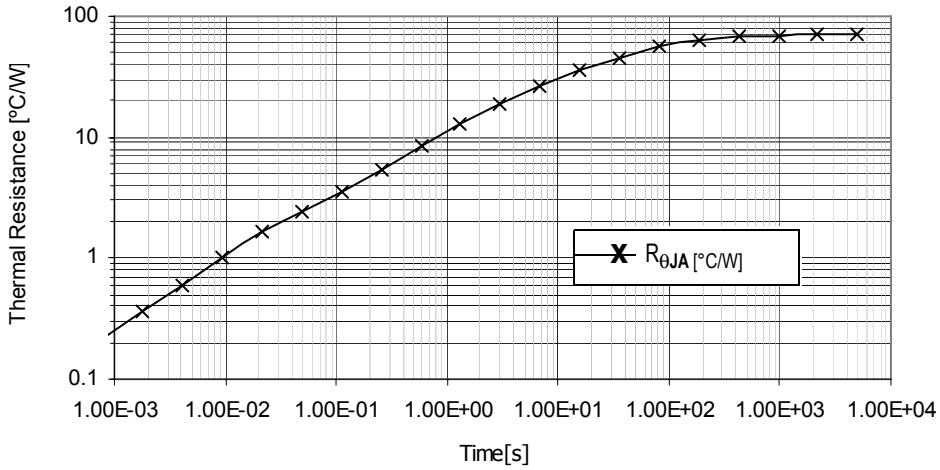


Figure 17. Transient Thermal Resistance $R_{\theta JA}$,
1 W Step response, Device on Thermal Test Board Area A = 600 (mm^2)

REVISION HISTORY

REVISION	DATE	DESCRIPTION OF CHANGES
3	12/2005	• Implemented Revision History page • Changed Static Electrical Table, $I_{PWR(SS)}$ Min characteristics, from “-10” to “-”.
4	9/2006	• Added Thermal Addendum
5	4/2007	• Minor labeling corrections to 33996 Simplified Internal Block Diagram on page 2 - changed pins SCLK to $\overline{CS}$ and CSB to SCLK. • Removed Peak Package Reflow Temperature During Reflow (solder reflow) parameter from MAXIMUM RATINGS on page 4. Added note with instructions from www.freescale.com. • Added the EK package type to the included thermal addendum.
6	6/2007	• Added MCZ33996EK/R2.
7	8/2008	• Updated package drawing
8.0	8/2008	• Added Exposed Pad pin to Pin Definitions (**Table 1**) on page 3.

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