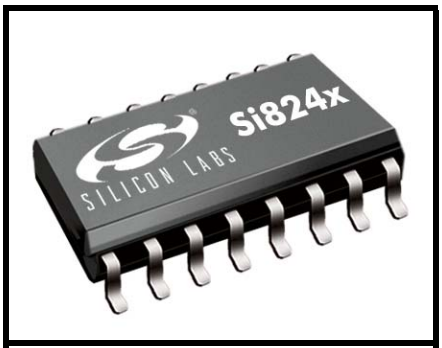
Class D Audio Driver with Precision Dead-Time Generator

Features

- 0.5 A peak output (Si8241)
- 4.0 A peak output (Si8244)
- PWM input
- High-precision linear programmable dead-time generator
  - 0.4 ns to 1 µs
- High latchup immunity >100 V/ns
- Up to 1500 Vrms output-output isolation, supply voltage of ±750 V
- Input to output isolation for low noise (up to 2500 V)
- Up to 8 MHz operation
- Wide operating range
  - –40 to +125 °C
- Transient immunity >45 kV/µs
- RoHS-compliant
  - SOIC-16 narrow body



Ordering Information:
See page 25.

Applications

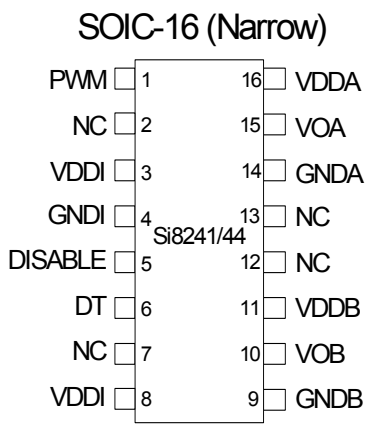
- Class D audio amplifiers

Description

The Si824x isolated driver family combines two isolated drivers in a single package. The Si8241/44 are high-side/low-side drivers specifically targeted at high-power (>30 W) audio applications. Versions with peak output currents of 0.5 A (Si8241) and 4.0 A (Si8244) are available. All drivers operate with a maximum supply voltage of 24 V.

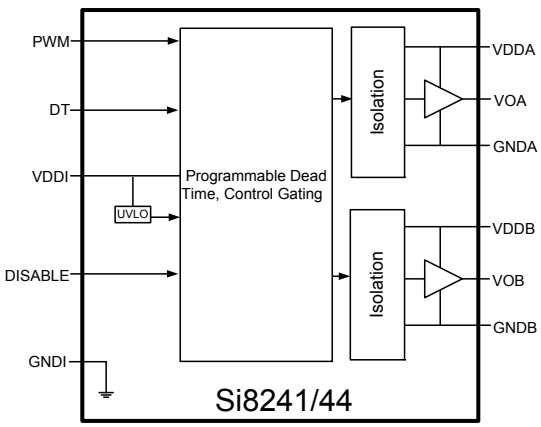
Based on Silicon Labs' proprietary isolation technology, the Si824x audio drivers incorporate input-to-output and output-to-output isolation, which enables level-translation of signals without additional external circuits as well as use of bipolar supply voltage up to ±750 V. The Si824x audio drivers feature an integrated dead-time generator that provides highly precise control for achieving optimal THD. These products also have overlap protection that safeguards against shoot-through current damage. The CMOS-based design also provides robust immunity from latch-up and high-voltage transients. The extremely low propagation delays enable faster modulation frequencies for an enhanced audio experience. The TTL level compatible inputs with >400 mV hysteresis are available in PWM input configuration; other options include UVLO levels of 8 V or 10 V. These products are available in narrow body SOIC packages.

Pin Assignments



Patents Pending

Functional Block Diagram



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1. Top-Level Block Diagram

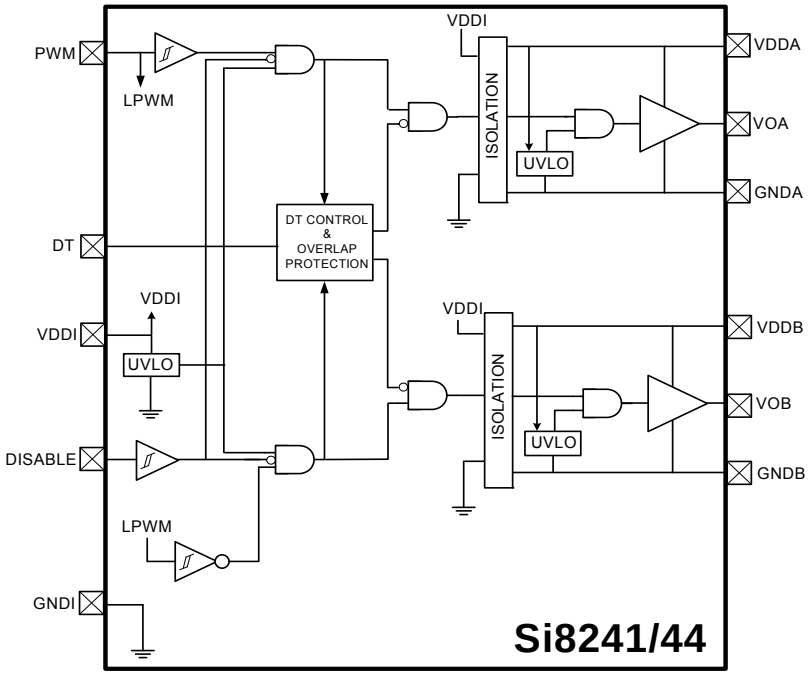


Figure 1. Si8241/44 Single-Input High-Side/Low-Side Isolated Drivers

2. Electrical Specifications

Table 1. Electrical Characteristics[1]

4.5 V < VDDI < 5.5 V, VDDA = VDDB = 12 V or 15 V. TA = –40 to +125 °C. Typical specs at 25 °C

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
DC Specifications						
Input-Side Power Supply Voltage	VDDI		4.5	—	5.5	V
Driver Supply Voltage	VDDA, VDDB	Voltage between VDDA and GNDA, and VDDB and GNDB (See “6. Ordering Guide”)	6.5	—	24	V
Input Supply Quiescent Current	IDDI(Q)	Si8241/44	—	2	3	mA
Output Supply Quiescent Current	IDDA(Q), IDDB(Q)	Current per channel	—	—	3.0	mA
Input Supply Active Current	IDDI	PWM freq = 500 kHz	—	2.5	—	mA
Output Supply Active Current	IDDO	PWM freq = 500 kHz	—	3.6	—	mA
Input Pin Leakage Current	IPWM		–10	—	+10	µA dc
Input Pin Leakage Current	IDISABLE		–10	—	+10	µA dc
Logic High Input Threshold	VIH		2.0	—	—	V
Logic Low Input Threshold	VIL		—	—	0.8	V
Input Hysteresis	VI_{HYST}		400	450	—	mV
Logic High Output Voltage	VOAH, VOBH	IOA, IOB = –1 mA	(VDDA /VDDB) — 0.04	—	—	V
Logic Low Output Voltage	VOAL, VOBL	IOA, IOB = 1 mA	—	—	0.04	V
Output Short-Circuit Pulsed Sink Current	IOA(SCL), IOB(SCL)	Si8241, Figure 2	—	0.5	—	A
		Si8244, Figure 2	—	4.0	—	A
Output Short-Circuit Pulsed Source Current	IOA(SCH), IOB(SCH)	Si8241, Figure 3	—	0.25	—	A
		Si8244, Figure 3	—	2.0	—	A
Output Sink Resistance	$R_{ON(SINK)}$	Si8241	—	5.0	—	Ω
		Si8244	—	1.0	—	Ω
Output Source Resistance	$R_{ON(SOURCE)}$	Si8241	—	15	—	Ω
		Si8244	—	2.7	—	Ω

Notes:
1. VDDA = VDDB = 12 V for 8 V UVLO and 10 V UVLO devices.
2. The largest RDT resistor that can be used is 220 kΩ.

Table 1. Electrical Characteristics[1] (Continued)
4.5 V < VDDI < 5.5 V, VDDA = VDDB = 12 V or 15 V. TA = –40 to +125 °C. Typical specs at 25 °C

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
VDDI Undervoltage Threshold	$VDDI_{UV+}$	VDDI rising	3.60	4.0	4.45	V
VDDI Undervoltage Threshold	$VDDI_{UV-}$	VDDI falling	3.30	3.70	4.15	V
VDDI Lockout Hysteresis	$VDDI_{HYS}$		—	250	—	mV
VDDA, VDDB Undervoltage Threshold	$VDDA_{UV+}$, $VDDB_{UV+}$	VDDA, VDDB rising				
8 V Threshold		See Figure 35 on page 21.	7.50	8.60	9.40	V
10 V Threshold		See Figure 36 on page 21.	9.60	11.1	12.2	V
VDDA, VDDB Undervoltage Threshold	$VDDA_{UV-}$, $VDDB_{UV-}$	VDDA, VDDB falling				
8 V Threshold		See Figure 35 on page 21.	7.20	8.10	8.70	V
10 V Threshold		See Figure 36 on page 21.	9.40	10.1	10.9	V
VDDA, VDDB Lockout Hysteresis	$VDDA_{HYS}$, $VDDB_{HYS}$	UVLO voltage = 8 V	—	600	—	mV
VDDA, VDDB Lockout Hysteresis	$VDDA_{HYS}$, $VDDB_{HYS}$	UVLO voltage = 10 V	—	1000	—	mV
AC Specifications						
Minimum Pulse Width			—	10	—	ns
Propagation Delay	t_{PHL}, t_{PLH}	CL = 1 nF	—	25	60	ns
Pulse Width Distortion $\lvert t_{PLH} - t_{PHL} \rvert$	PWD		—	1.0	5.60	ns
Programmed Dead Time[2]	DT	See Figures 37 and 38	0.4	—	1000	ns
Output Rise and Fall Time	t_R,t_F	C_L = 1 nF (Si8241)	—	—	20	ns
		C_L = 1 nF (Si8244)	—	—	12	ns
Shutdown Time from Disable True	t_{SD}		—	—	60	ns
Restart Time from Disable False	$t_{RESTART}$		—	—	60	ns
Device Start-up Time	t_{START}	Time from VDD_ = VDD_UV+ to VOA, VOB = VIA, VIB	—	5	7	µs
Common Mode Transient Immunity	CMTI	VIA, VIB, PWM = VDDI or 0 V V_{CM} = 1500 V (see Figure 4)	25	45	—	kV/µs

Notes:
1. VDDA = VDDB = 12 V for 8 V UVLO and 10 V UVLO devices.
2. The largest RDT resistor that can be used is 220 kΩ.

2.1. Test Circuits

Figures 2 and 3 depict sink current and source current test circuits.

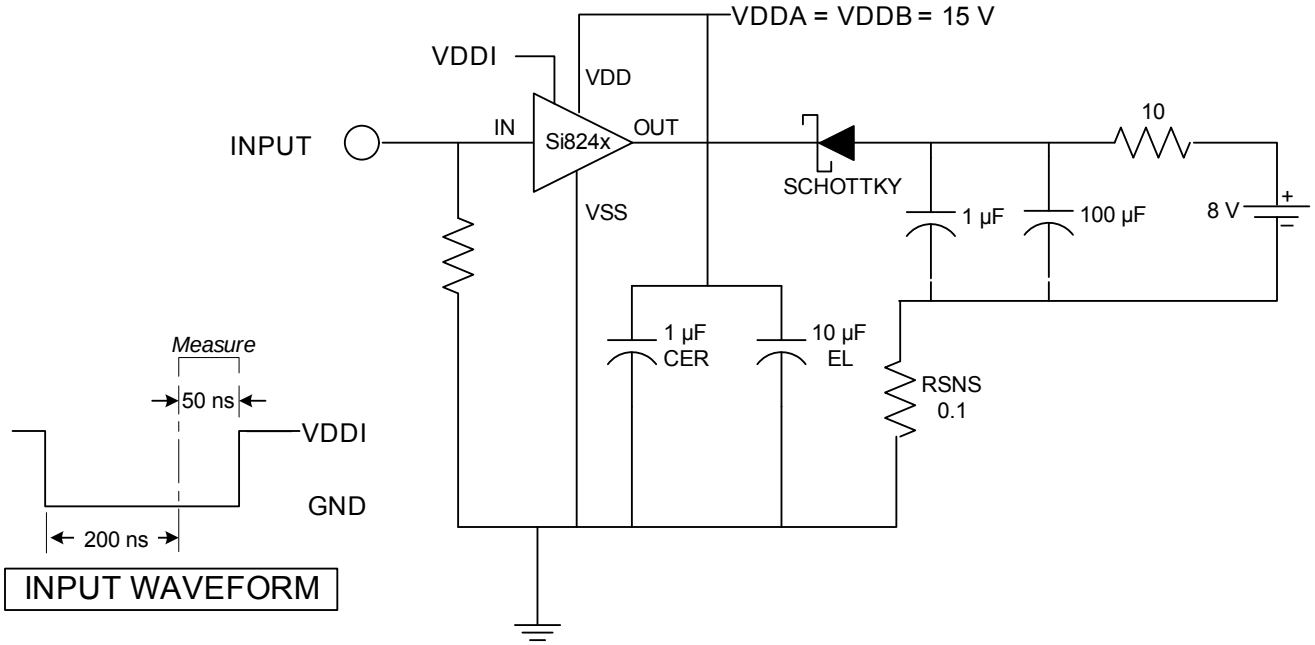


Figure 2. IOL Sink Current Test Circuit

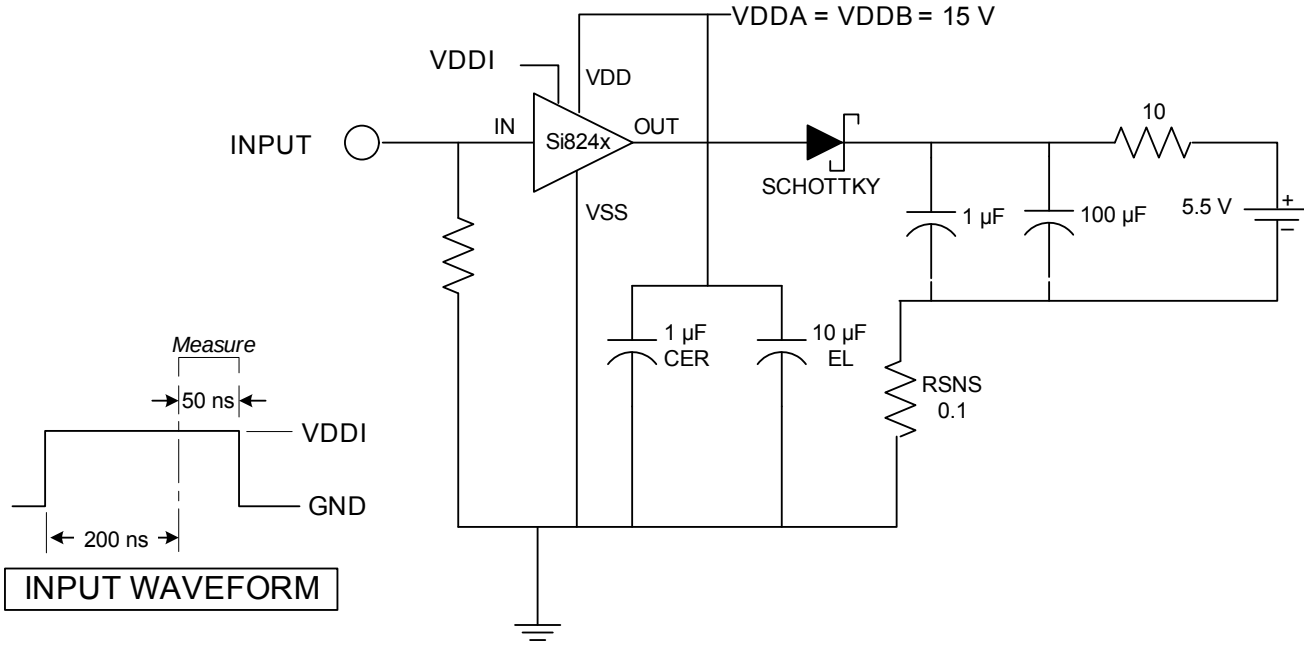


Figure 3. IOH Source Current Test Circuit

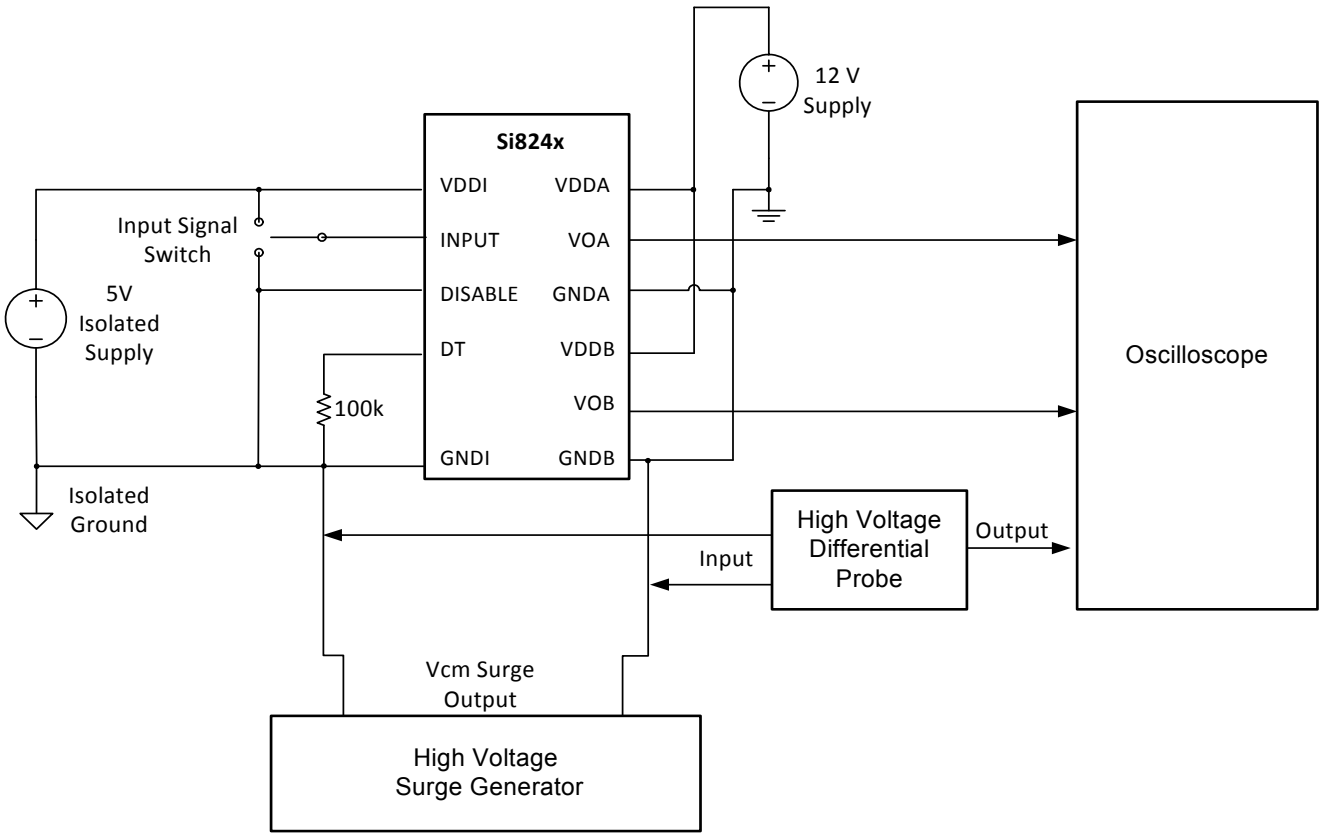


Figure 4. Common Mode Transient Immunity Test Circuit

Table 2. Regulatory Information*

CSA
The Si824x is certified under CSA Component Acceptance Notice 5A. For more details, see File 232873.
61010-1: Up to 300 V_{RMS} reinforced insulation working voltage; up to 600 V_{RMS} basic insulation working voltage.
60950-1: Up to 300 V_{RMS} reinforced insulation working voltage; up to 600 V_{RMS} basic insulation working voltage.
VDE
The Si824x is certified according to IEC 60747-5-2. For more details, see File 5006301-4880-0001.
60747-5-2: Up to 560 V_{peak} for basic insulation working voltage.
UL
The Si824x is certified under UL1577 component recognition program. For more details, see File E257455.
Rated up to 2500 V_{RMS} isolation voltage for basic protection.
***Note:** Regulatory Certifications apply to 2.5 kV_{RMS} rated devices, which are production tested to 3.0 kV_{RMS} for 1 sec. For more information, see "6.Ordering Guide" on page 25.

Table 3. Insulation and Safety-Related Specifications

Parameter	Symbol	Test Condition	Value	Unit
			NBSOIC-16 2.5 kV_{RMS}	
Nominal Air Gap (Clearance)[1]	L(1O1)		4.01	mm
Nominal External Tracking (Creepage)[1]	L(1O2)		4.01	mm
Minimum Internal Gap (Internal Clearance)			0.011	mm
Tracking Resistance (Proof Tracking Index)	PTI	IEC60112	600	V
Erosion Depth	ED		0.019	mm
Resistance (Input-Output)[2]	R_{IO}		10^{12}	Ω
Capacitance (Input-Output)[2]	C_{IO}	f = 1 MHz	1.4	pF
Input Capacitance[3]	C_I		4.0	pF

Notes:
1. The values in this table correspond to the nominal creepage and clearance values as detailed in “7. Package Outline: 16-Pin Narrow Body SOIC” . VDE certifies the clearance and creepage limits as 4.7 mm minimum for the NB SOIC-16. UL does not impose a clearance and creepage minimum for component level certifications. CSA certifies the clearance and creepage limits as 3.9 mm minimum for the NB SOIC 16.
2. To determine resistance and capacitance, the Si824x is converted into a 2-terminal device. Pins 1–8 are shorted together to form the first terminal and pins 9–16 are shorted together to form the second terminal. The parameters are then measured between these two terminals.
3. Measured from input pin to ground.

Table 4. IEC 60664-1 (VDE 0884 Part 2) Ratings

Parameter	Test Conditions	Specification
		NB SOIC-16
Basic Isolation Group	Material Group	I
Installation Classification	Rated Mains Voltages ≤ 150 V_{RMS}	I-IV
	Rated Mains Voltages ≤ 300 V_{RMS}	I-III
	Rated Mains Voltages ≤ 400 V_{RMS}	I-II
	Rated Mains Voltages ≤ 600 V_{RMS}	I-II

Table 5. IEC 60747-5-2 Insulation Characteristics*

Parameter	Symbol	Test Condition	Characteristic	Unit
			NB SOIC-16	
Maximum Working Insulation Voltage	V_{IORM}		560	V peak
Input to Output Test Voltage	V_{PR}	Method b1 (V_{IORM} x 1.875 = V_{PR}, 100% Production Test, t_m = 1 sec, Partial Discharge < 5 pC)	1050	V peak
Transient Overvoltage	V_{IOTM}	t = 60 sec	4000	V peak
Pollution Degree (DIN VDE 0110, Table 1)			2	
Insulation Resistance at T_S, V_{IO} = 500 V	R_S		$>10^9$	Ω

***Note:** Maintenance of the safety data is ensured by protective circuits. The Si824x provides a climate classification of 40/125/21.

Table 6. IEC Safety Limiting Values[1]

Parameter	Symbol	Test Condition	NB SOIC-16	Unit
Case Temperature	T_S		150	°C
Safety Input Current	I_S	θ_{JA} = 105 °C/W (NB SOIC-16), V_{DDI} = 5.5 V, V_{DDA} = V_{DDB}= 24 V, T_J = 150 °C, T_A = 25 °C	50	mA
Device Power Dissipation[2]	P_D		1.2	W

Notes:
1. Maximum value allowed in the event of a failure. Refer to the thermal derating curve in Figure 5.
2. The Si82xx is tested with V_{DDI} = 5.5 V, V_{DDA} = V_{DDB} = 24 V, T_J = 150 ºC, C_L = 100 pF, input 2 MHz 50% duty cycle square wave.

Table 7. Thermal Characteristics

Parameter	Symbol	NB SOIC-16	Unit
IC Junction-to-Air Thermal Resistance	θ_{JA}	105	°C/W

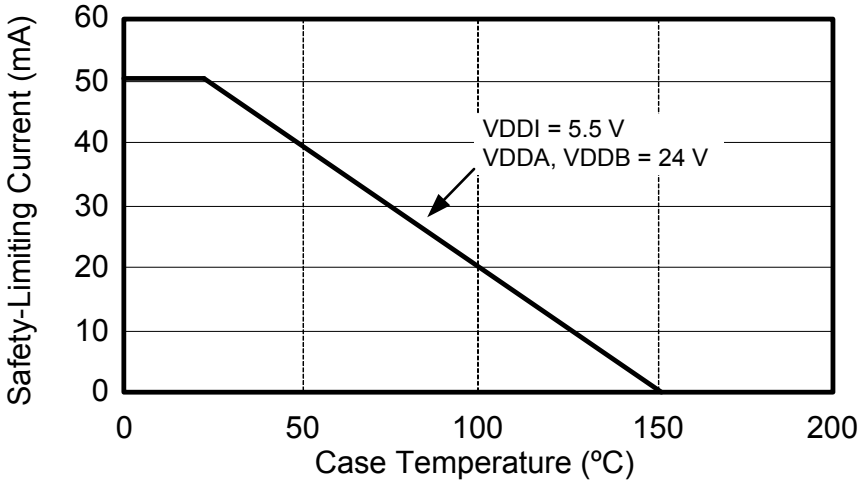


Figure 5. NB SOIC-16, Thermal Derating Curve, Dependence of Safety Limiting Values with Case Temperature per DIN EN 60747-5-2

Table 8. Absolute Maximum Ratings[1]

Parameter	Symbol	Min	Typ	Max	Units
Storage Temperature[2]	T_{STG}	–65	—	+150	°C
Ambient Temperature under Bias	T_A	–40	—	+125	°C
Input-side Supply Voltage	VDDI	–0.6	—	6.0	V
Driver-side Supply Voltage	VDDA, VDDB	–0.6	—	30	V
Voltage on any Pin with respect to Ground	VIN	–0.5	—	VDD + 0.5	V
Output Drive Current per Channel	I_O	—	—	10	mA
Lead Solder Temperature (10 sec)		—	—	260	°C
Latchup Immunity[3]		—	—	100	V/ns
Maximum Isolation (Input to Output)		—	—	2500	V_{RMS}
Maximum Isolation (Output to Output)		—	—	1500	V_{RMS}

Notes:
1. Permanent device damage may occur if the absolute maximum ratings are exceeded. Functional operation should be restricted to the conditions as specified in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
2. VDE certifies storage temperature from –40 to 150 °C.
3. Latchup immunity specification is for slew rate applied across GNDI and GNDA or GNDB.

3. Functional Description

The operation of an Si824x channel is analogous to that of an opto coupler and gate driver, except an RF carrier is modulated instead of light. This simple architecture provides a robust isolated data path and requires no special considerations or initialization at start-up. A simplified block diagram for a single Si824x channel is shown in Figure 6.

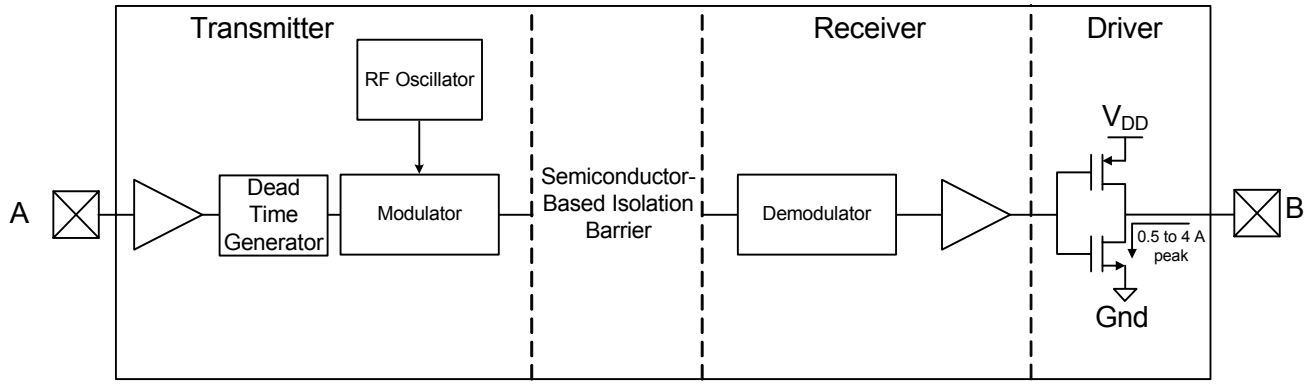


Figure 6. Simplified Channel Diagram

A channel consists of an RF Transmitter and RF Receiver separated by a semiconductor-based isolation barrier. Referring to the Transmitter, input A modulates the carrier provided by an RF oscillator using on/off keying. The Receiver contains a demodulator that decodes the input state according to its RF energy content and applies the result to output B via the output driver. This RF on/off keying scheme is superior to pulse code schemes as it provides best-in-class noise immunity, low power consumption, and better immunity to magnetic fields. See Figure 7 for more details.

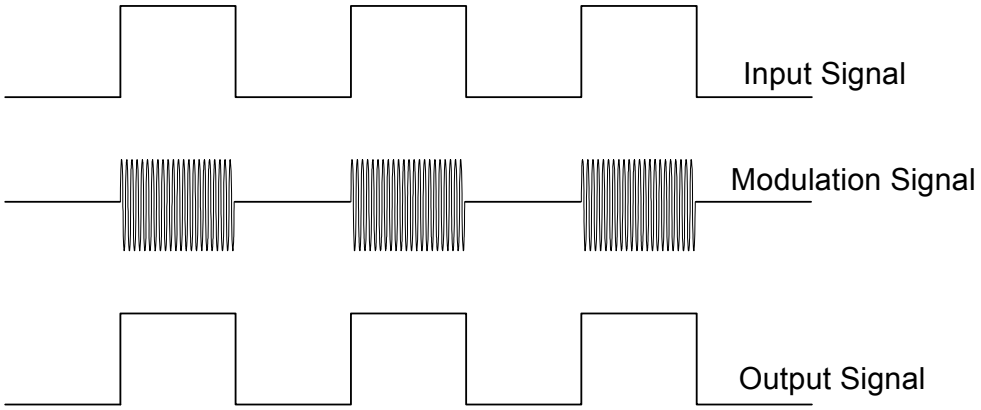


Figure 7. Modulation Scheme

3.1. Typical Performance Characteristics (0.5 Amp)

The typical performance characteristics depicted in Figures 8 through 19 are for information purposes only. Refer to Table 1 on page 5 for actual specification limits.

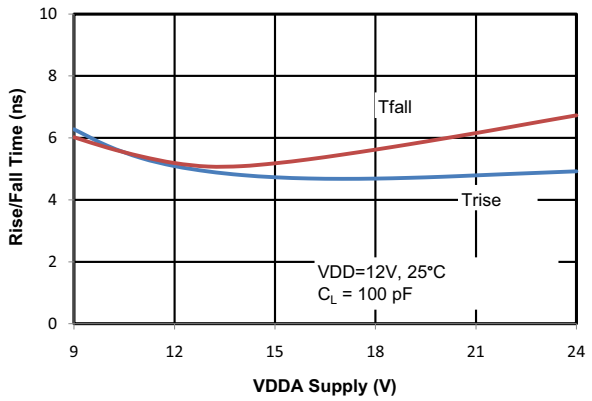


Figure 8. Rise/Fall Time vs. Supply Voltage

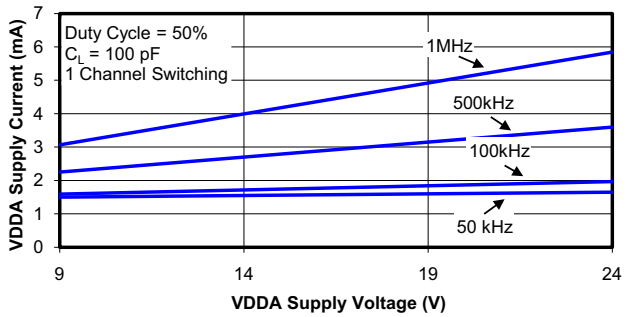


Figure 11. Supply Current vs. Supply Voltage

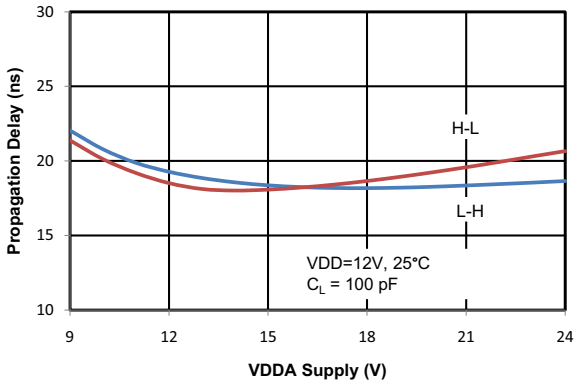


Figure 9. Propagation Delay vs. Supply Voltage

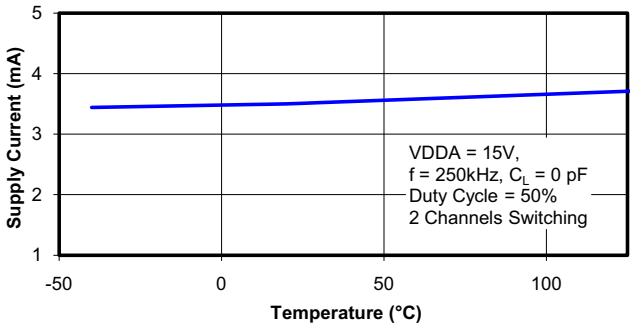


Figure 12. Supply Current vs. Temperature

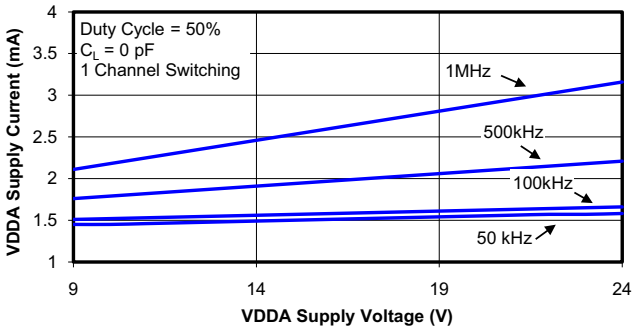


Figure 10. Supply Current vs. Supply Voltage

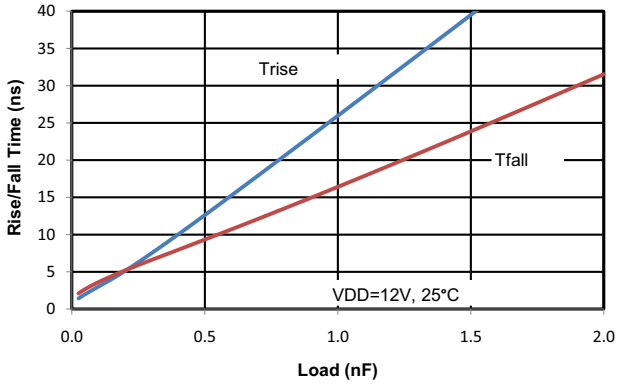


Figure 13. Rise/Fall Time vs. Load

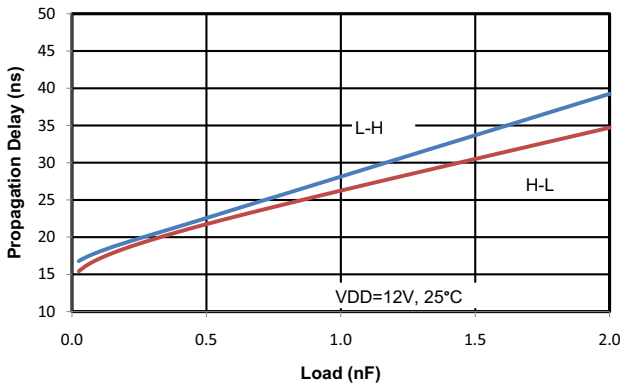


Figure 14. Propagation Delay vs. Load

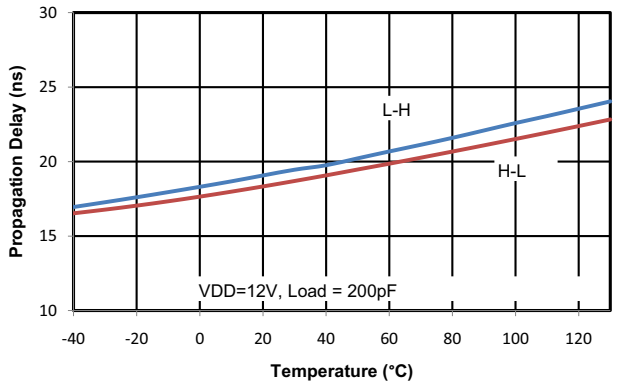


Figure 15. Propagation Delay vs. Temperature

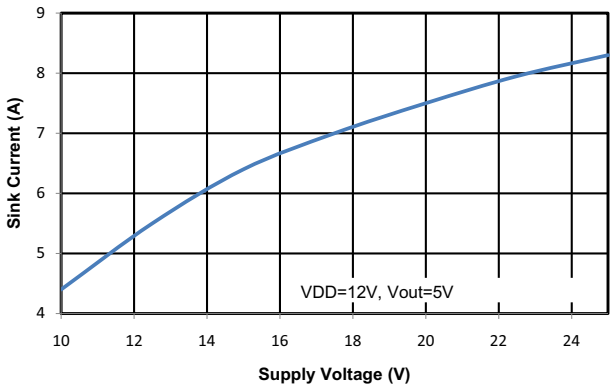


Figure 16. Output Sink Current vs. Supply Voltage

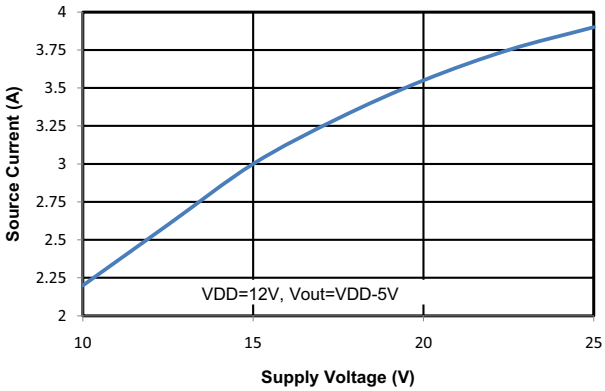


Figure 17. Output Source Current vs. Supply Voltage

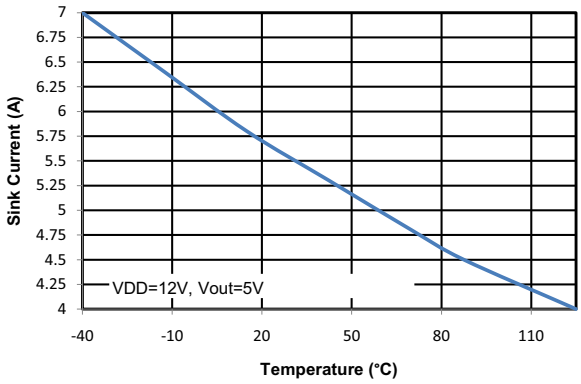


Figure 18. Output Sink Current vs. Temperature

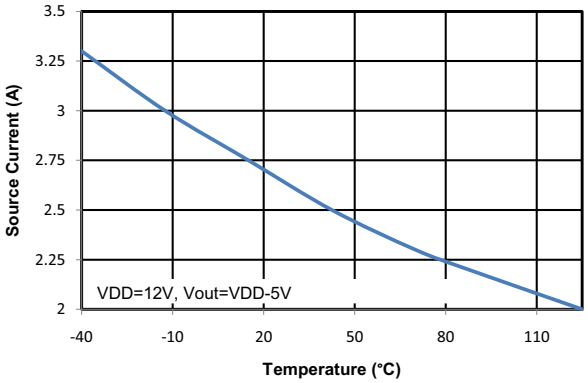


Figure 19. Output Source Current vs. Temperature

3.2. Typical Performance Characteristics (4.0 Amp)

The typical performance characteristics depicted in Figures 20 through 31 are for information purposes only. Refer to Table 1 on page 5 for actual specification limits.

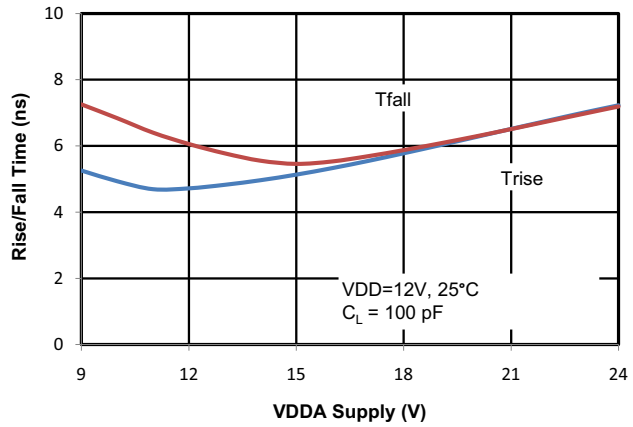


Figure 20. Rise/Fall Time vs. Supply Voltage

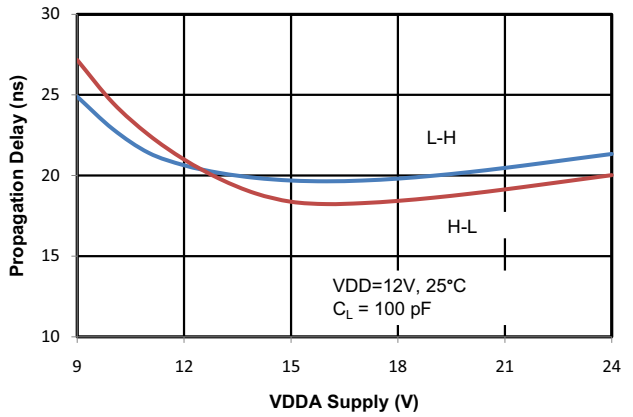


Figure 21. Propagation Delay vs. Supply Voltage

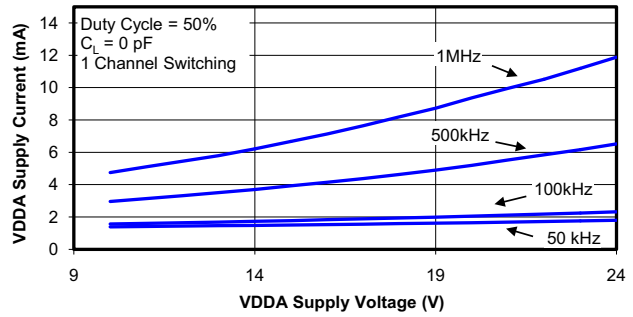


Figure 22. Supply Current vs. Supply Voltage

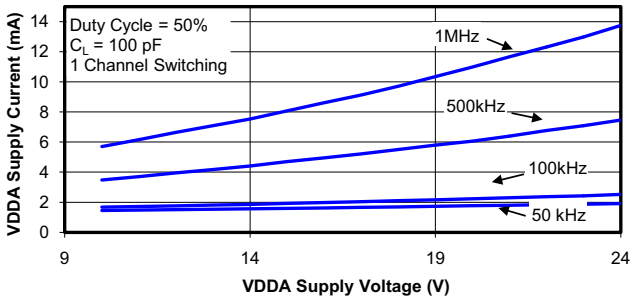


Figure 23. Supply Current vs. Supply Voltage

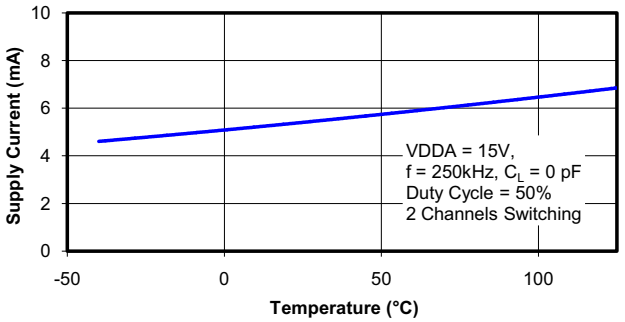


Figure 24. Supply Current vs. Temperature

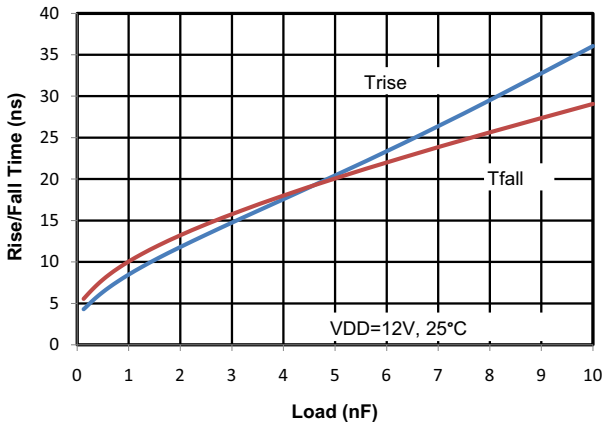


Figure 25. Rise/Fall Time vs. Load

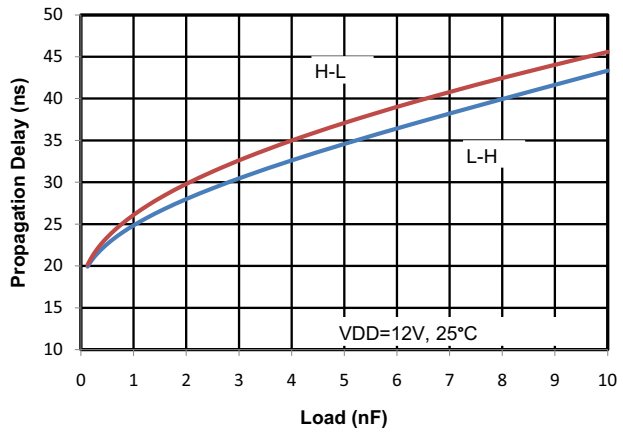


Figure 26. Propagation Delay vs. Load

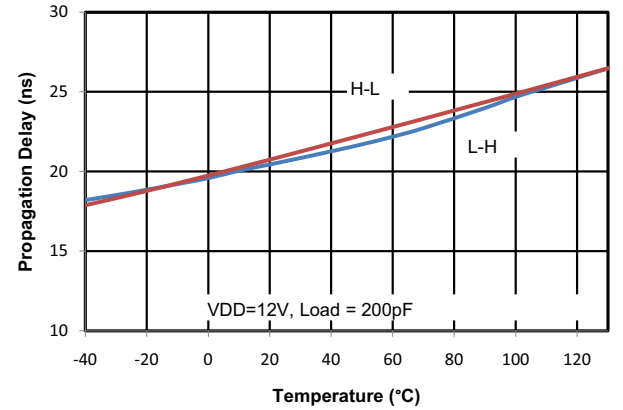


Figure 27. Propagation Delay vs. Temperature

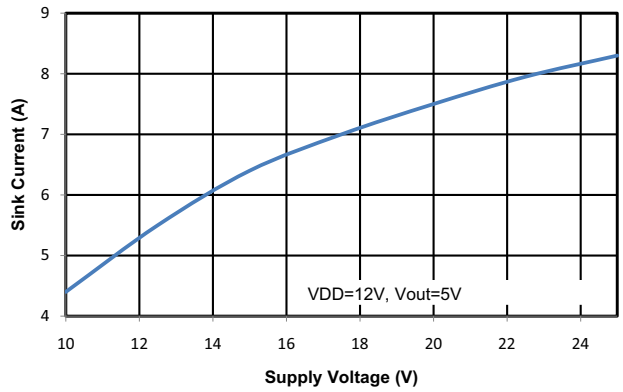


Figure 28. Output Sink Current vs. Supply Voltage

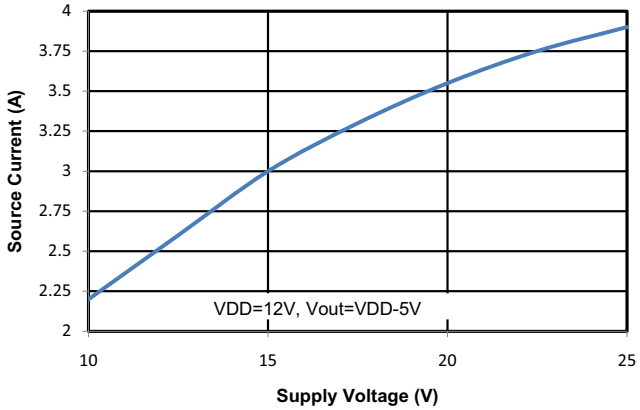


Figure 29. Output Source Current vs. Supply Voltage

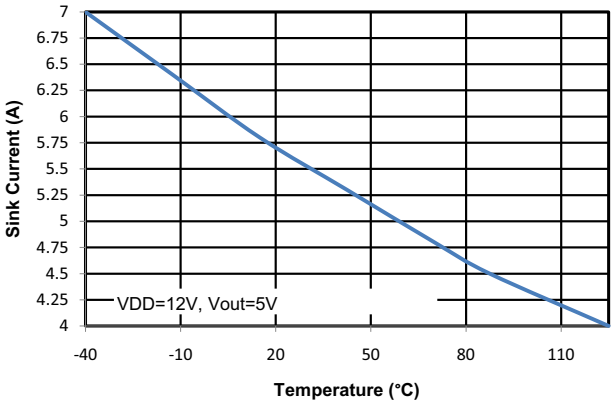


Figure 30. Output Sink Current vs. Temperature

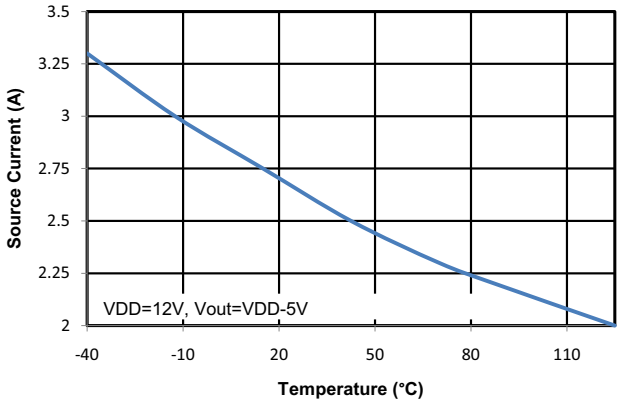


Figure 31. Output Source Current vs. Temperature

3.3. Family Overview and Logic Operation During Startup

The Si824x family of isolated drivers consists of high-side, low-side, and dual driver configurations.

3.3.1. Products

Table 9 shows the configuration and functional overview for each product in this family.

Table 9. Si824x Family Overview

Part Number	Configuration	UVLO Voltage	Programmable Dead Time	Inputs	Peak Output Current (A)
Si8241	High-Side/Low-Side	8 V/10 V	✓	PWM	0.5
Si8244	High-Side/Low-Side	8 V/10 V	✓	PWM	4.0

3.3.2. Device Behavior

Table 10 contains truth tables for the Si8241/4 families.

Table 10. Si824x Family Truth Table*

Si8241/4 (PWM Input High-Side/Low-Side) Truth Table					
PWM Input	VDDI State	Disable	Output		Notes
			VOA	VOB	
H	Powered	L	H	L	Output transition occurs after internal dead time expires.
L	Powered	L	L	H	Output transition occurs after internal dead time expires.
X	Unpowered	X	L	L	Output returns to input state within 7 µs of VDDI power restoration.
X	Powered	H	L	L	Device is disabled.
***Note:** This truth table assumes VDDA and VDDB are powered. If VDDA and VDDB are below UVLO, see "3.7.2.Undervoltage Lockout" on page 20 for more information.					

3.4. Power Supply Connections

Isolation requirements mandate individual supplies for VDDI, VDDA, and VDDB. The decoupling caps for these supplies must be placed as close to the VDD and GND pins of the Si824x as possible. The optimum values for these capacitors depend on load current and the distance between the chip and the regulator that powers it. Low effective series resistance (ESR) capacitors, such as Tantalum, are recommended.

3.5. Power Dissipation Considerations

Proper system design must assure that the Si824x operates within safe thermal limits across the entire load range. The Si824x total power dissipation is the sum of the power dissipated by bias supply current, internal switching losses, and power delivered to the load. Equation 1 shows total Si824x power dissipation. In a non-overlapping system, such as a high-side/low-side driver, n = 1.

$$P_D = V_{DDI}I_{DDI} + 2(V_{DDO}I_{QOUT} + C_{int}V_{DDO}^2F) + 2n(C_LV_{DDO}^2F)$$

where:

P_D is the total Si824x device power dissipation (W)

I_{DDI} is the input-side maximum bias current (3 mA)

I_{QOUT} is the driver die maximum bias current (2.5 mA)

C_{int} is the internal parasitic capacitance (75 pF for the 0.5 A driver and 370 pF for the 4.0 A driver)

V_{DDI} is the input-side VDD supply voltage (4.5 to 5.5 V)

V_{DDO} is the driver-side supply voltage (10 to 24 V)

F is the switching frequency (Hz)

n is the overlap constant (max value = 2)

Equation 1.

The maximum power dissipation allowable for the Si824x is a function of the package thermal resistance, ambient temperature, and maximum allowable junction temperature, as shown in Equation 2:

$$P_{Dmax} \leq \frac{T_{jmax} - T_A}{\theta ja}$$

where:

P_{Dmax} = Maximum Si824x power dissipation (W)

T_{jmax} = Si824x maximum junction temperature (150 °C)

T_A = Ambient temperature (°C)

θja = Si824x junction-to-air thermal resistance (105 °C/W)

F = Si824x switching frequency (Hz)

Equation 2.

Substituting values for P_{Dmax} T_{jmax}, T_A, and θ_{ja} into Equation 2 results in a maximum allowable total power dissipation of 1.19 W. Maximum allowable load is found by substituting this limit and the appropriate datasheet values from Table 1 on page 5 into Equation 1 and simplifying. The result is Equation 3 (0.5 A driver) and Equation 4 (4.0 A driver), both of which assume VDDI = 5 V and VDDA = VDDB = 18 V.

$$C_{L(MAX)} = \frac{1.4 \times 10^{-3}}{F} - 7.5 \times 10^{-11}$$

Equation 3.

$$C_{L(MAX)} = \frac{1.4 \times 10^{-3}}{F} - 3.7 \times 10^{-10}$$

Equation 4.

Equation 1 and Equation 2 are graphed in Figure 32 where the points along the load line represent the package dissipation-limited value of CL for the corresponding switching frequency.

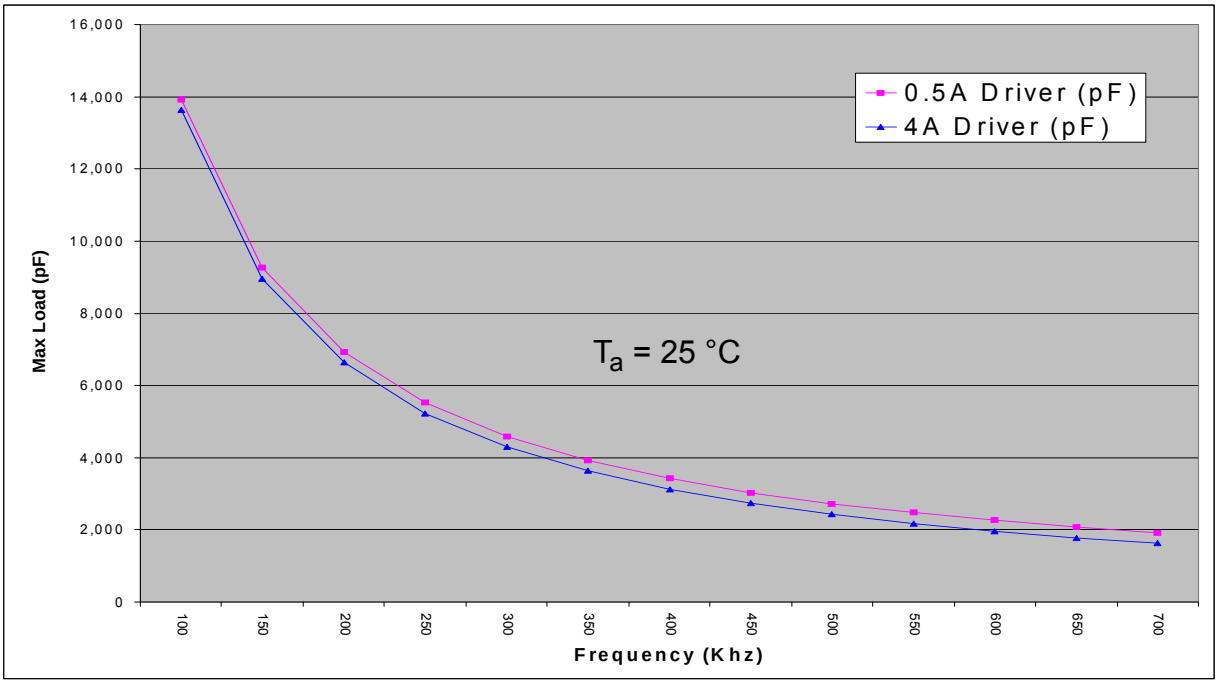


Figure 32. Max Load vs. Switching Frequency

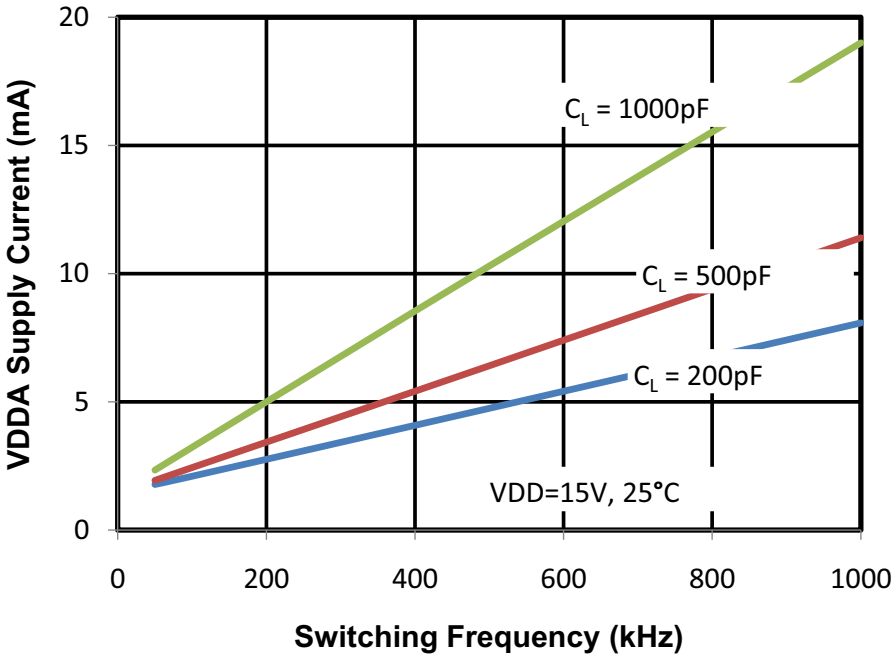


Figure 33. Switching Frequency vs. Load Current

3.6. Layout Considerations

It is most important to minimize ringing in the drive path and noise on the Si824x VDD lines. Care must be taken to minimize parasitic inductance in these paths by locating the Si824x as close to the device it is driving as possible. In addition, the VDD supply and ground trace paths must be kept short. For this reason, the use of power and ground planes is highly recommended. A split ground plane system having separate ground and VDD planes for power devices and small signal components provides the best overall noise performance.

3.7. Undervoltage Lockout Operation

Device behavior during start-up, normal operation and shutdown is shown in Figure 34, where UVLO+ and UVLO- are the positive-going and negative-going thresholds respectively. Note that outputs VOA and VOB default low when input side power supply (VDDI) is not present.

3.7.1. Device Startup

Outputs VOA and VOB are held low during power-up until VDD is above the UVLO threshold for time period tSTART. Following this, the outputs follow the states of inputs VIA and VIB.

3.7.2. Undervoltage Lockout

Undervoltage Lockout (UVLO) is provided to prevent erroneous operation during device startup and shutdown or when VDD is below its specified operating circuits range. The input (control) side, Driver A and Driver B, each have their own undervoltage lockout monitors.

The Si824x input side enters UVLO when VDDI $\leq$ $VDDI_{UV-}$, and exits UVLO when VDDI > $VDDI_{UV+}$. The driver outputs, VOA and VOB, remain low when the input side of the Si824x is in UVLO and their respective VDD supply (VDDA, VDDB) is within tolerance. Each driver output can enter or exit UVLO independently. For example, VOA unconditionally enters UVLO when VDDA falls below $VDDA_{UV-}$ and exits UVLO when VDDA rises above $VDDA_{UV+}$.

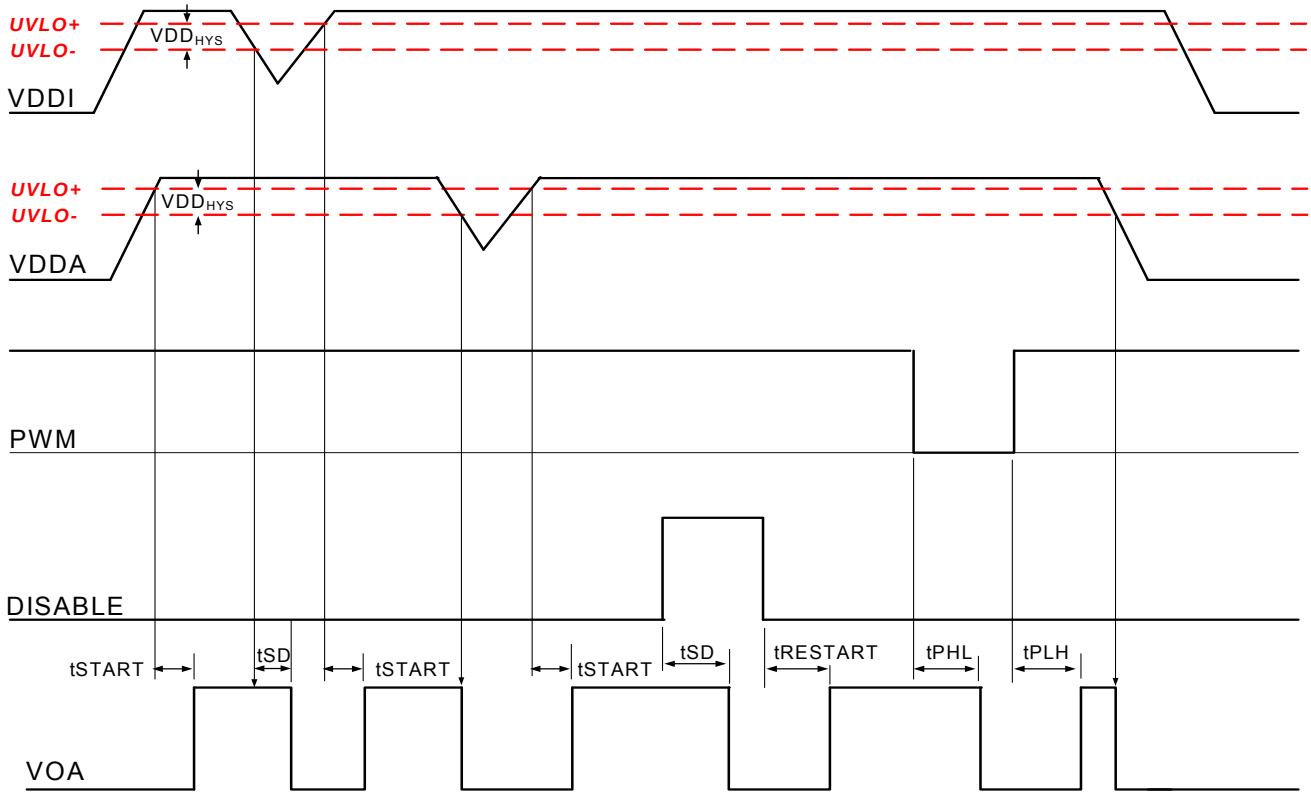


Figure 34. Device Behavior during Normal Operation and Shutdown

3.7.3. Undervoltage Lockout (UVLO)

The UVLO circuit unconditionally drives VO low when VDD is below the lockout threshold. Referring to Figures 35 and 36, upon power up, the Si824x is maintained in UVLO until VDD rises above VDD_{UV+}. During power down, the Si824x enters UVLO when VDD falls below the UVLO threshold plus hysteresis (i.e., VDD ≤ VDD_{UV+} – VDD_{HYS}).

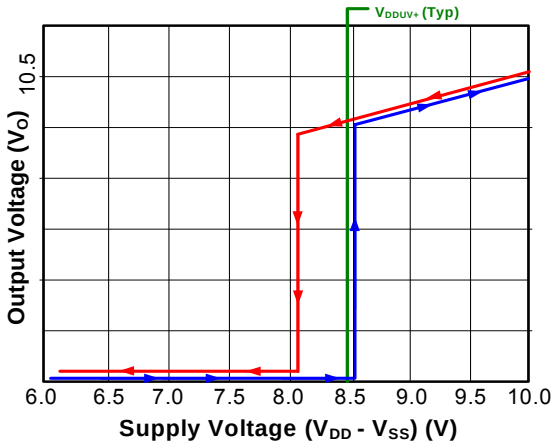


Figure 35. Si824x UVLO Response (8 V)

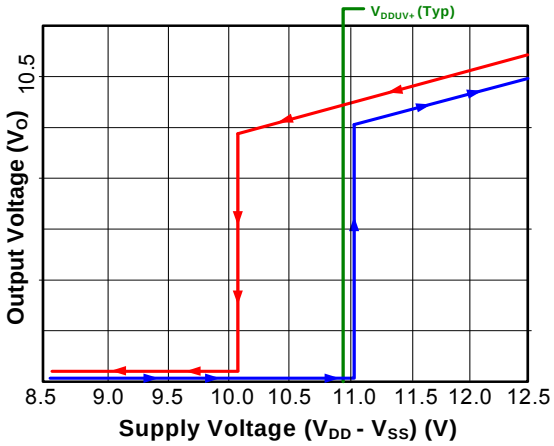


Figure 36. Si824x UVLO Response (10 V)

3.7.4. Control Inputs

PWM inputs are high-true, TTL level-compatible logic inputs. VOA is high and VOB is low when the PWM input is high, and VOA is low and VOB is high when the PWM input is low.

3.7.5. Disable Input

When brought high, the DISABLE input unconditionally drives VOA and VOB low regardless of the states of input. Device operation terminates within tSD after DISABLE = V_{IH} and resumes within tRESTART after DISABLE = V_{IL}. The DISABLE input has no effect if VDDI is below its UVLO level (i.e. VOA, VOB remain low). The DISABLE input is typically connected to external protection circuitry to unconditionally halt driver operation in the event of a fault.

3.8. Programmable Dead Time and Overlap Protection

All high-side/low-side drivers (Si8241/4) include programmable overlap protection to prevent outputs VOA and VOB from being high at the same time. These devices also include programmable dead time, which adds a user-programmable delay between transitions of VOA and VOB. When enabled, dead time is present on all transitions, even after overlap recovery. The amount of dead time delay (DT) is programmed by a single resistor (RDT) connected from the DT input to ground per Equation 5. Minimum dead time (approximately 400 ps) can be achieved by connecting the DT pin to VDDI. Note that dead time accuracy is limited by the resistor's (R_{DT}) tolerance and temperature coefficient. See Figures 37 and 38 for additional information about dead time operation.

$$DT \approx 10 \times RDT$$

where:

DT= dead time (ns)

and

RDT= dead time programming resistor (kΩ)

Equation 5.

Figure 37. Dead Time vs.Resistance (R_{DT})

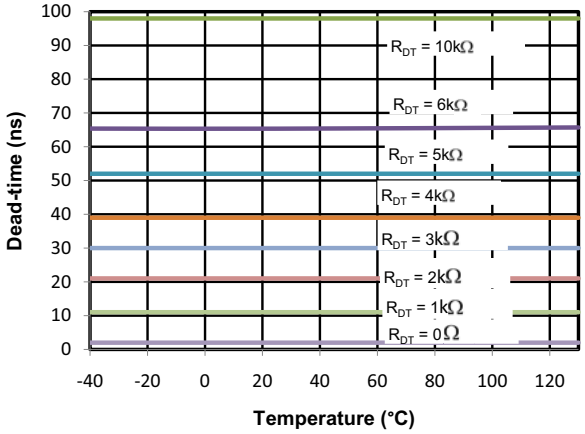


Figure 38. Dead Time vs.Temperature

4. Applications

The following examples illustrate typical circuit configurations using the Si824x.

4.1. Class D Digital Audio Driver

Figures 39 and 40 show the Si8241/4 controlled by a single PWM signal. Supply can be unipolar (0 to 1500 V) or bipolar (± 750 V).

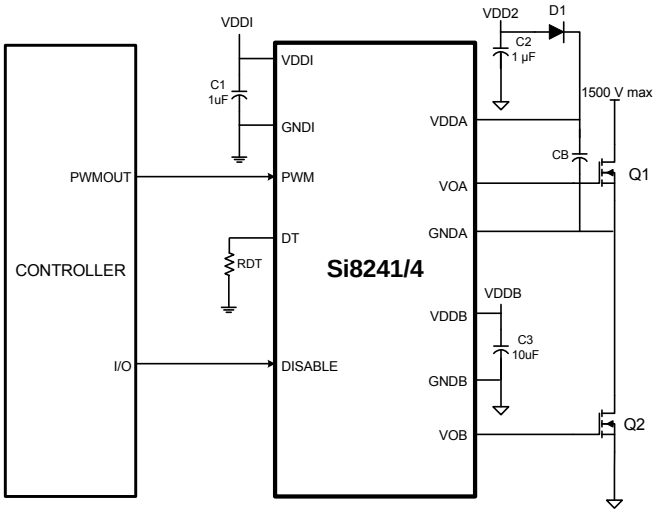


Figure 39. Si824x in Half-Bridge Audio Application

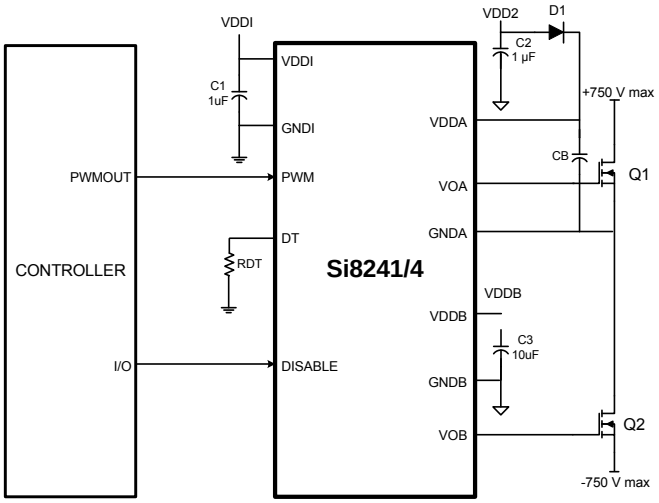


Figure 40. Si824x in Half-Bridge Audio Application

D1 and CB form a conventional bootstrap circuit that allows VOA to operate as a high-side driver for Q1, which has a maximum drain voltage of 1500 V. VOB is connected as a conventional low-side driver. Note that the input side of the Si824x requires VDD in the range of 4.5 to 5.5 V, while the VDDA and VDDB output side supplies must be between 6.5 and 24 V with respect to their respective grounds. The boot-strap start up time will depend on the CB cap chosen. VDD2 is usually the same as VDDB. Also note that the bypass capacitors on the Si824x should be located as close to the chip as possible. Moreover, it is recommended that 0.1 and 10 µF bypass capacitors be used to reduce high frequency noise and maximize performance. The D1 diode should be a fast-recovery diode; it should be able to withstand the maximum high voltage (e.g. 1500 V) and be low-loss. See “AN486: High-Side Bootstrap Design Using Si823x ISODrivers in Power Delivery Systems” for more details in selecting the bootstrap cap (CB) and diode (D1).

5. Pin Descriptions

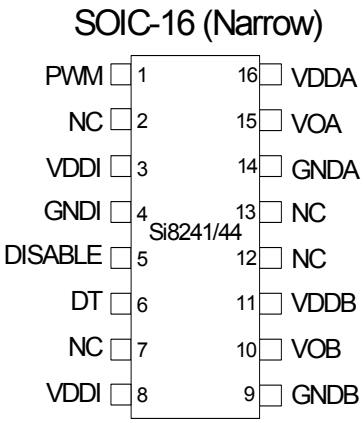


Table 11. Si8241/44 PWM Input HS/LS Isolated Driver (SOIC-16)

Pin	Name	Description
1	PWM	PWM input.
2	NC	No connection.
3	VDDI	Input-side power supply terminal; connect to a source of 4.5 to 5.5 V.
4	GNDI	Input-side ground terminal.
5	DISABLE	Device Disable. When high, this input unconditionally drives outputs VOA, VOB LOW. It is strongly recommended that this input be connected to external logic level to avoid erroneous operation due to capacitive noise coupling.
6	DT	Dead time programming input. The value of the resistor connected from DT to ground sets the dead time between output transitions of VOA and VOB. Defaults to 1 ns dead time when connected to VDDI or left open (see "3.8.Programmable Dead Time and Overlap Protection" on page 22).
7	NC	No connection.
8	VDDI	Input-side power supply terminal; connect to a source of 4.5 to 5.5 V.
9	GNDB	Ground terminal for Driver B.
10	VOB	Driver B output (low-side driver).
11	VDDB	Driver B power supply voltage terminal; connect to a source of 6.5 to 24 V.
12	NC	No connection.
13	NC	No connection.
14	GNDA	Ground terminal for Driver A.
15	VOA	Driver A output (high-side driver).
16	VDDA	Driver A power supply voltage terminal; connect to a source of 6.5 to 24 V.

6. Ordering Guide

The currently available OPNs are listed in Table 12.

Table 12. Ordering Part Numbers*

Ordering Part Number (OPN)	Input Type	Package	Drive Strength	Output	UVLO Voltage	Isolation Rating (Input to Output)
Si8241BB-D-IS1	PWM	NB SOIC-16	0.5 A	High-Side/Low-Side	8 V	2.5 kVrms
Si8241CB-D-IS1	PWM	NB SOIC-16			10 V	
Si8244BB-D-IS1	PWM	NB SOIC-16	4 A		8 V	
Si8244CB-D-IS1	PWM	NB SOIC-16			10 V	

***Note:** All packages are RoHS-compliant with peak reflow temperatures of 260 °C according to the JEDEC industry standard classifications and peak solder temperatures. Tape and reel options are specified by adding an “R” suffix to the ordering part number. “Si” and “SI” are used interchangeably.

7. Package Outline: 16-Pin Narrow Body SOIC

Figure 41 illustrates the package details for the Si824x in a 16-pin narrow-body SOIC (SO-16). Table 13 lists the values for the dimensions shown in the illustration.

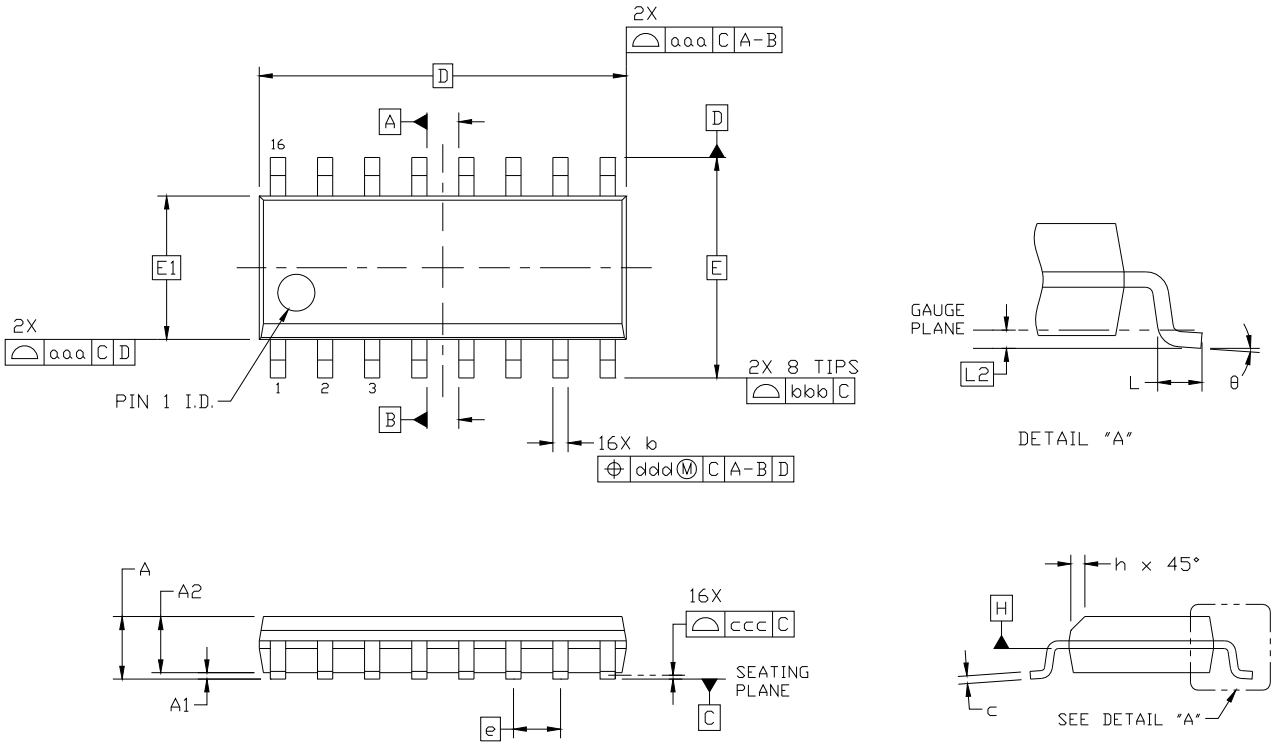


Figure 41. 16-pin Small Outline Integrated Circuit (SOIC) Package

Table 13. Package Diagram Dimensions

Dimension	Min	Max		Dimension	Min	Max
A	—	1.75		L	0.40	1.27
A1	0.10	0.25		L2	0.25 BSC	
A2	1.25	—		h	0.25	0.50
b	0.31	0.51		θ	0°	8°
c	0.17	0.25		aaa	0.10	
D	9.90 BSC			bbb	0.20	
E	6.00 BSC			ccc	0.10	
E1	3.90 BSC			ddd	0.25	
e	1.27 BSC					

Notes:
1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to the JEDEC Solid State Outline MS-012, Variation AC.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

8. Land Pattern: 16-Pin Narrow Body SOIC

Figure 42 illustrates the recommended land pattern details for the Si824x in a 16-pin narrow-body SOIC. Table 14 lists the values for the dimensions shown in the illustration.

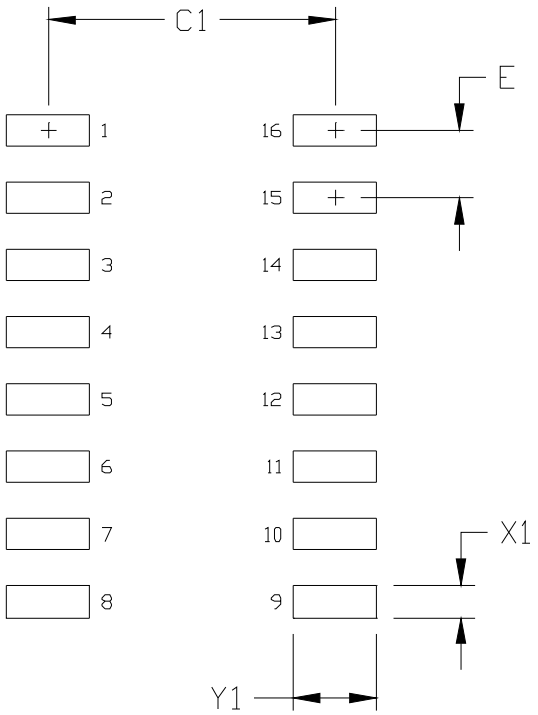


Figure 42. 16-Pin Narrow Body SOIC PCB Land Pattern

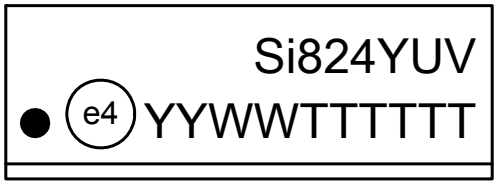
Table 14. 16-Pin Narrow Body SOIC Land Pattern Dimensions

Dimension	Feature	(mm)
C1	Pad Column Spacing	5.40
E	Pad Row Pitch	1.27
X1	Pad Width	0.60
Y1	Pad Length	1.55

Notes:
1. This Land Pattern Design is based on IPC-7351 pattern SOIC127P600X165-16N for Density Level B (Median Land Protrusion).
2. All feature sizes shown are at Maximum Material Condition (MMC) and a card fabrication tolerance of 0.05 mm is assumed.

9. Top Marking: 16-Pin Narrow Body SOIC

9.1. Si824x Top Marking (16-Pin Narrow Body SOIC)



9.2. Top Marking Explanation (16-Pin Narrow Body SOIC)

Line 1 Marking:	Base Part Number Ordering Options See Ordering Guide for more information.	Si824 = ISOdriver product series Y = Peak output current ■ 1 = 0.5 A ■ 4 = 4.0 A U = UVLO level ■ B = 8 V; C = 10 V V = Isolation rating ■ B = 2.5 kV
Line 2 Marking:	YY = Year WW = Workweek	Assigned by the Assembly House. Corresponds to the year and workweek of the mold date.
	TTTTTT = Mfg Code	Manufacturing Code from Assembly Purchase Order form.

DOCUMENT CHANGE LIST

Revision 0.1 to Revision 0.2

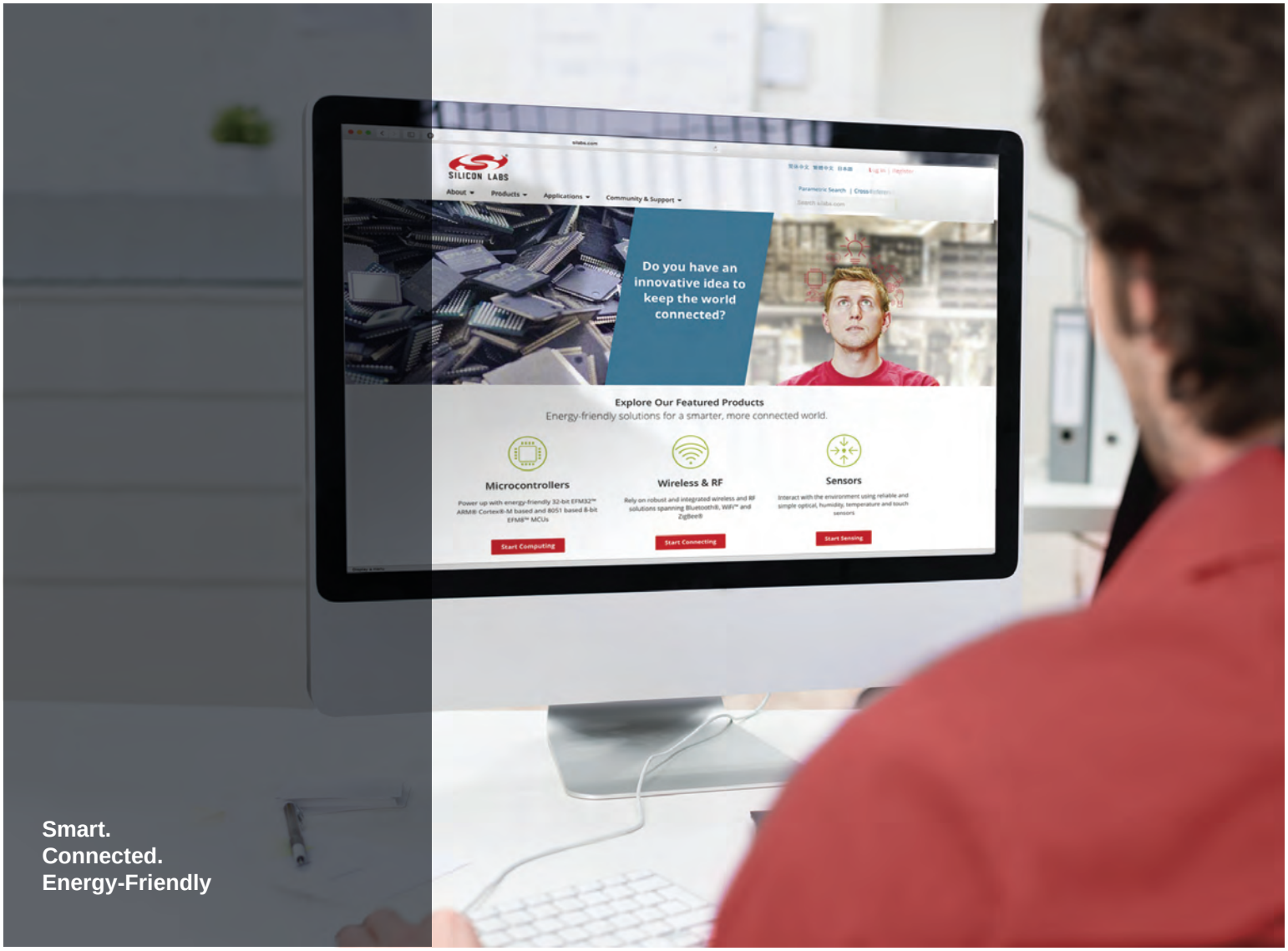
- Deleted Table 3.
- Added Tables 2 through 7.
- Added Figure 5.
- Updated common-mode transient immunity specification throughout.

Revision 0.2 to Revision 0.3

- Updated Figures 2 and 3 on page 7.
- Added Figure 4 on page 8.
- Updated Table 12 on page 25.

Revision 0.3 to Revision 1.0

- Updated Table 12, Ordering Part Numbers.
  - Added Revision D Ordering Part Numbers.
  - Removed all Ordering Part Numbers of previous revisions.
  - Removed moisture sensitivity level table notes.



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