



P-Channel 20 V (D-S) MOSFET

PRODUCT SUMMARY

V_{DS} (V)	$R_{DS(on)}$ (Ω)	I_D (A) ^a	Q_g (Typ.)
- 20	0.061 at $V_{GS} = - 4.5$ V	- 4.4	7.6 nC
	0.080 at $V_{GS} = - 2.5$ V	- 3.8	
	0.110 at $V_{GS} = - 1.8$ V	- 3.3	
	0.165 at $V_{GS} = - 1.5$ V	- 0.5	

FEATURES

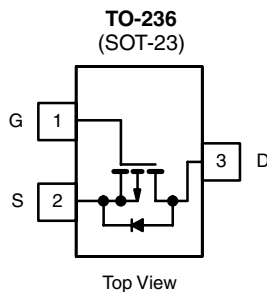
- Halogen-free According to IEC 61249-2-21 Definition
- TrenchFET[®] Power MOSFET
- 100 % R_g Tested
- Typical ESD Performance 2000 V
- Built in ESD Protection with Zener Diode
- Compliant to RoHS Directive 2002/95/EC



RoHS
COMPLIANT
HALOGEN
FREE

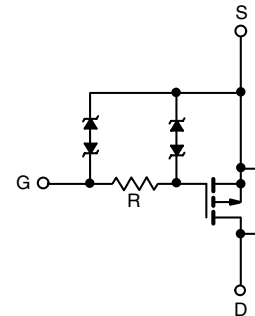
APPLICATIONS

- Load Switch for Portable Devices



Si2377EDS (P6)*

* Marking Code



P-Channel MOSFET

Ordering Information: Si2377EDS-T1-GE3 (Lead (Pb)-free and Halogen-free)

ABSOLUTE MAXIMUM RATINGS $T_A = 25^\circ\text{C}$, unless otherwise noted

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	- 20	V
Gate-Source Voltage	V_{GS}	± 8	
Continuous Drain Current ($T_J = 150^\circ\text{C}$)	$T_C = 25^\circ\text{C}$	- 4.4	A
	$T_C = 70^\circ\text{C}$	- 3.5	
	$T_A = 25^\circ\text{C}$	- 3.7 ^{b, c}	
	$T_A = 70^\circ\text{C}$	- 2.9 ^{b, c}	
Pulsed Drain Current	I_{DM}	- 20	A
Continuous Source-Drain Diode Current	$T_C = 25^\circ\text{C}$	- 1.5	
	$T_A = 25^\circ\text{C}$	- 1.0 ^{b, c}	
Maximum Power Dissipation	$T_C = 25^\circ\text{C}$	1.8	W
	$T_C = 70^\circ\text{C}$	1.1	
	$T_A = 25^\circ\text{C}$	1.25 ^{b, c}	
	$T_A = 70^\circ\text{C}$	0.8 ^{b, c}	
Operating Junction and Storage Temperature Range	T_J, T_{stg}	- 55 to 150	$^\circ\text{C}$
Soldering Recommendations (Peak Temperature) ^{d, e}		260	

THERMAL RESISTANCE RATINGS

Parameter	Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient ^{b, d}	R_{thJA}	80	100	$^\circ\text{C/W}$
Maximum Junction-to-Foot (Drain)	R_{thJF}	55	70	

Notes:

a. $T_C = 25^\circ\text{C}$.

b. Surface Mounted on 1" x 1" FR4 board.

c. $t = 5$ s.

d. Maximum under Steady State conditions is 130°C/W .

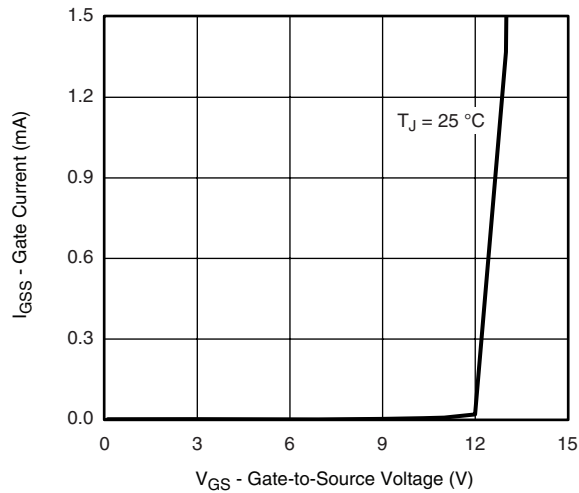
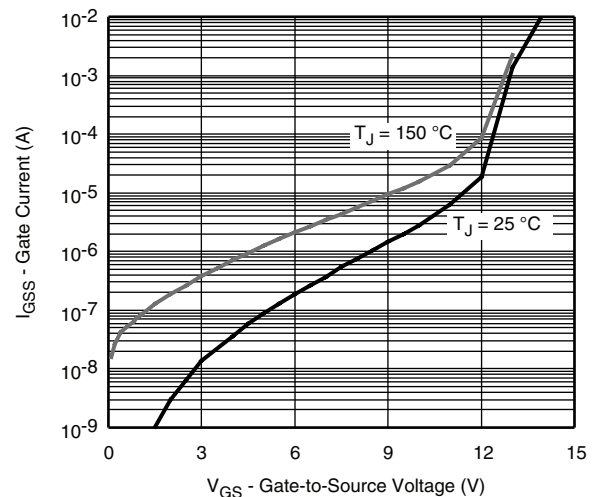
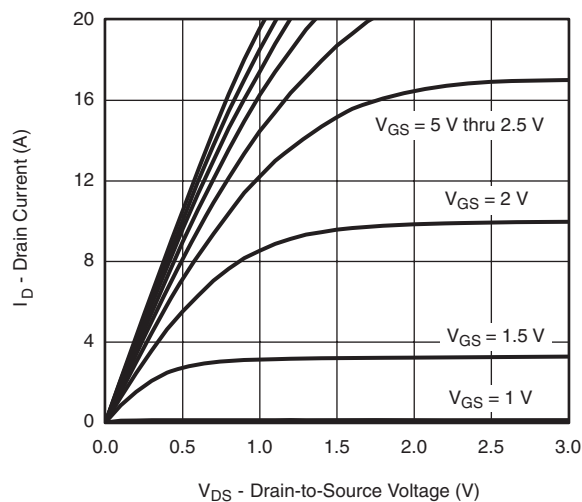
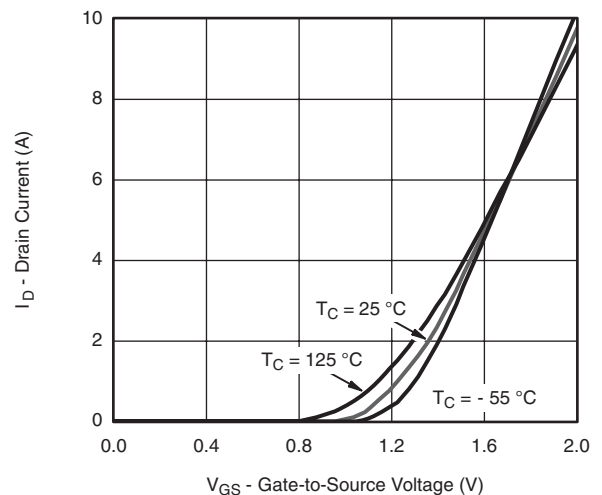
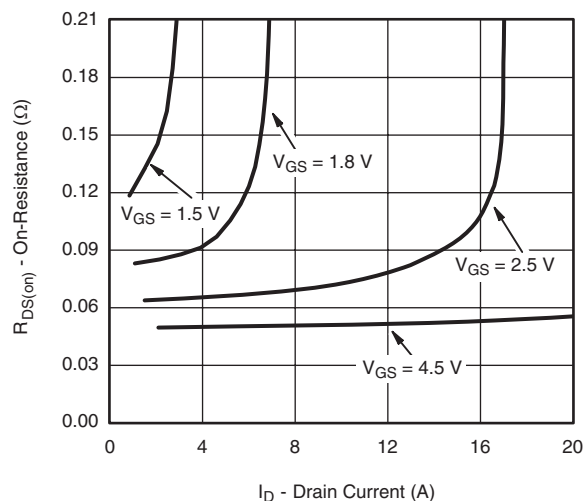
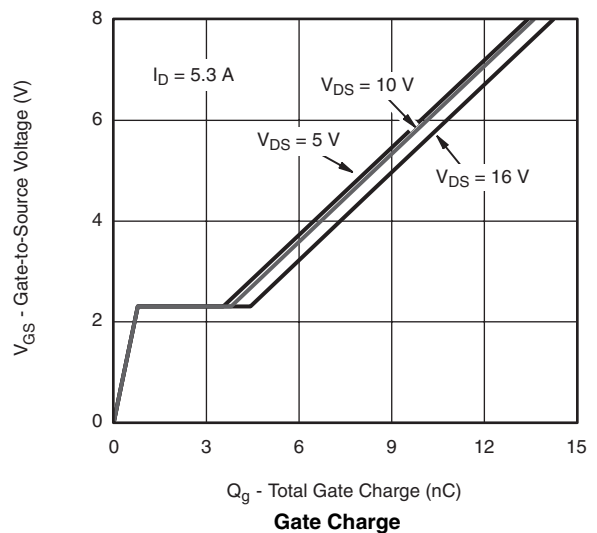
SPECIFICATIONS $T_J = 25\text{ }^{\circ}\text{C}$, unless otherwise noted

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Static						
Drain-Source Breakdown Voltage	V _{DS}	V _{GS} = 0 V, I _D = - 250 μA	- 20			V
V _{DS} Temperature Coefficient	ΔV _{DS} /T _J	I _D = - 250 μA		- 13		mV/°C
V _{GS(th)} Temperature Coefficient	ΔV _{GS(th)} /T _J			2.5		
Gate-Source Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = - 250 μA	- 0.4		- 1	V
Gate-Source Leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ± 8 V			± 6	μA
		V _{DS} = 0 V, V _{GS} = ± 4.5 V			± 0.5	
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = - 20 V, V _{GS} = 0 V			- 1	
		V _{DS} = - 20 V, V _{GS} = 0 V, T _J = 55 °C			- 10	
On-State Drain Current ^a	I _{D(on)}	V _{DS} ≤ - 5 V, V _{GS} = - 4.5 V	- 15			A
Drain-Source On-State Resistance ^a	R _{DS(on)}	V _{GS} = - 4.5 V, I _D = - 3.2 A		0.050	0.061	Ω
		V _{GS} = - 2.5 V, I _D = - 2.8 A		0.065	0.080	
		V _{GS} = - 1.8 V, I _D = - 1.5 A		0.090	0.110	
		V _{GS} = - 1.5 V, I _D = - 0.5 A		0.110	0.165	
Forward Transconductance ^a	g _{fs}	V _{DS} = - 10 V, I _D = - 3.2 A		12		S
Dynamic ^b						
Total Gate Charge	Q _g	V _{DS} = - 10 V, V _{GS} = - 8 V, I _D = - 5.3 A		14	21	nC
Gate-Source Charge		V _{DS} = - 10 V, V _{GS} = - 4.5 V, I _D = - 5.3 A		7.6	12	
			Q _{gs}		0.8	
Gate-Drain Charge	Q _{gd}			3.1		
Gate Resistance	R _g	f = 1 MHz	0.4	2	4	kΩ
Turn-On Delay Time	t _{d(on)}	V _{DD} = - 10 V, R _L = 2.3 Ω I _D ≅ - 4.3 A, V _{GEN} = - 4.5 V, R _g = 1 Ω		0.20	0.3	μs
Rise Time	t _r			1.00	1.50	
Turn-Off Delay Time	t _{d(off)}			4.00	6.00	
Fall Time	t _f			2.00	3.00	
Turn-On Delay Time	t _{d(on)}	V _{DD} = - 10 V, R _L = 2.3 Ω I _D ≅ - 4.3 A, V _{GEN} = - 8 V, R _g = 1 Ω		0.09	0.14	
Rise Time	t _r			0.40	0.60	
Turn-Off Delay Time	t _{d(off)}			5.20	7.80	
Fall Time	t _f			2.30	3.50	
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Diode Current	I _S	T _C = 25 °C			- 1.5	A
Pulse Diode Forward Current	I _{SM}				- 20	
Body Diode Voltage	V _{SD}	I _S = - 3 A, V _{GS} = 0 V		- 0.8	- 1.2	V
Body Diode Reverse Recovery Time	t _{rr}	I _F = - 3 A, dI/dt = 100 A/μs, T _J = 25 °C		30	60	ns
Body Diode Reverse Recovery Charge	Q _{rr}			20	40	nC
Reverse Recovery Fall Time	t _a			13		ns
Reverse Recovery Rise Time	t _b			17		

Notes:

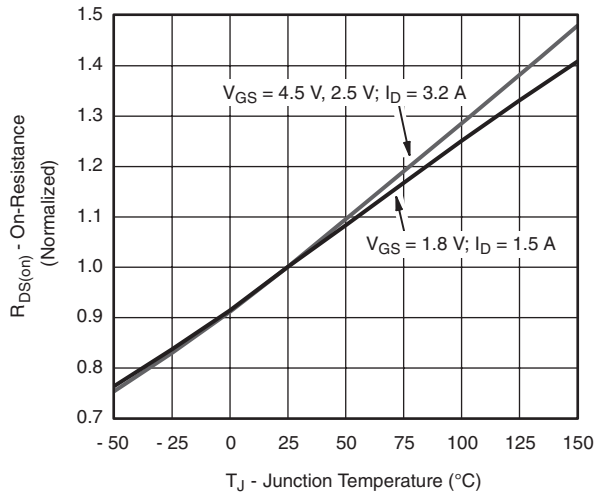
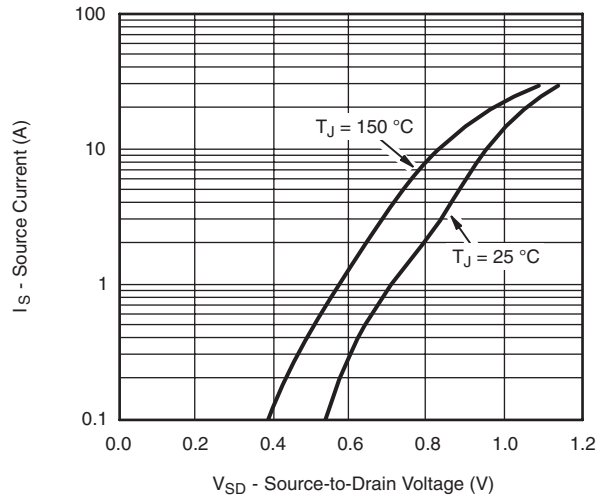
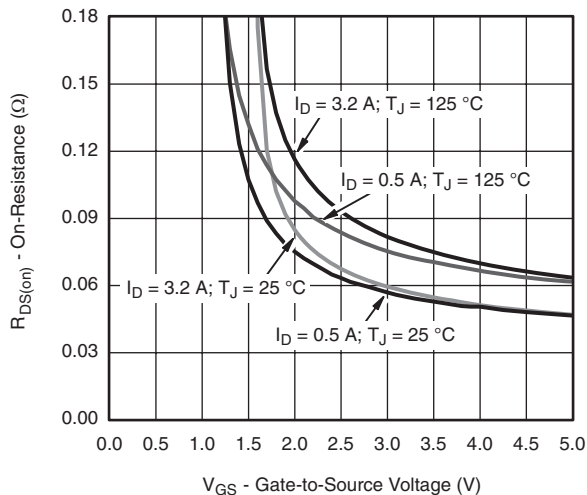
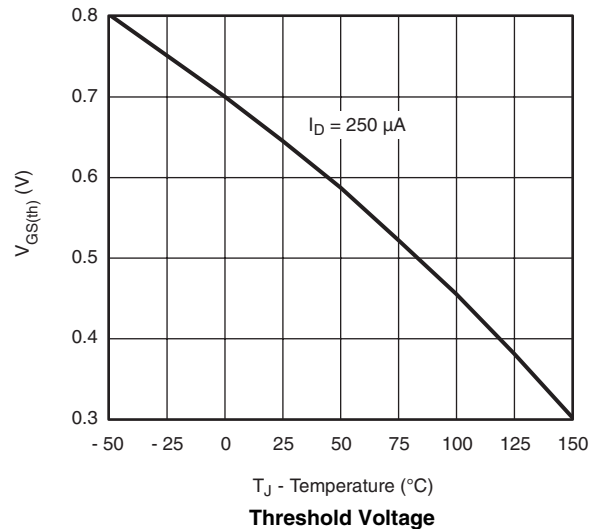
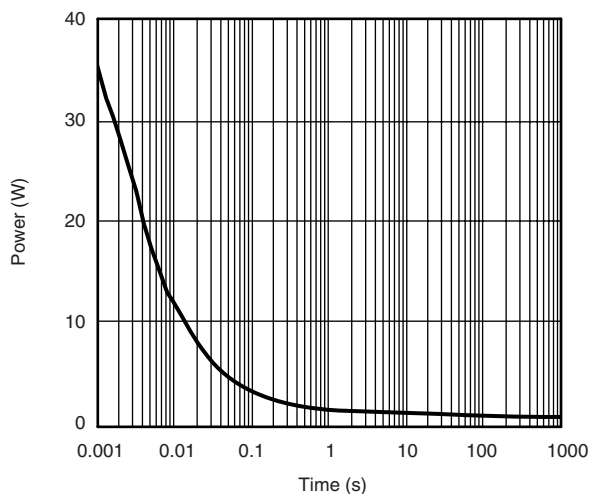
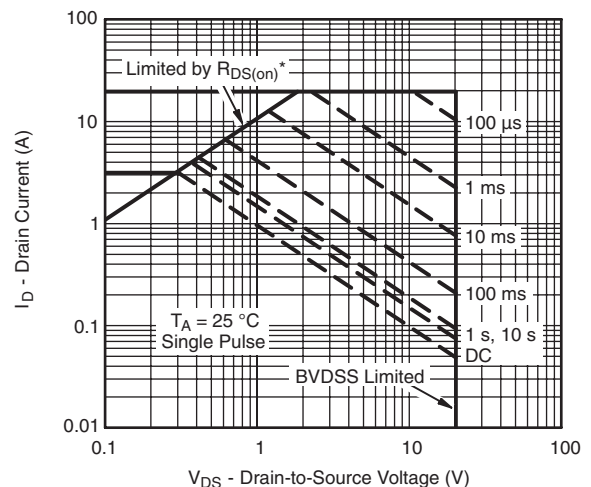
- a. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.
b. Guaranteed by design, not subject to production testing.

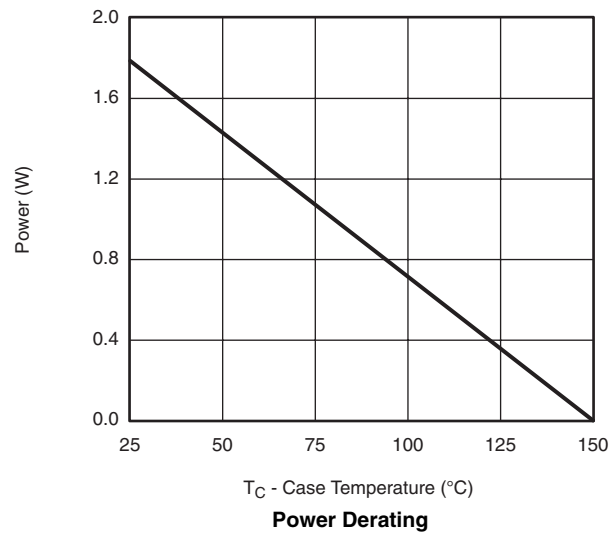
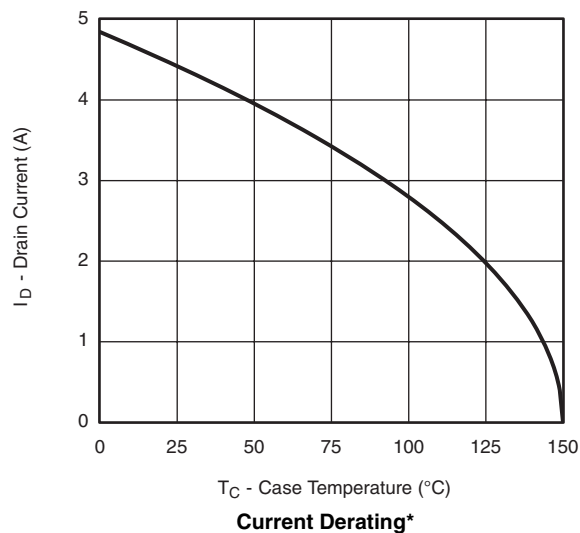
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.


TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

Gate Current vs. Gate-Source Voltage

Gate Current vs. Gate-Source Voltage

Output Characteristics

Transfer Characteristics

On-Resistance vs. Drain Current

Gate Charge

Si2377EDS

Vishay Siliconix

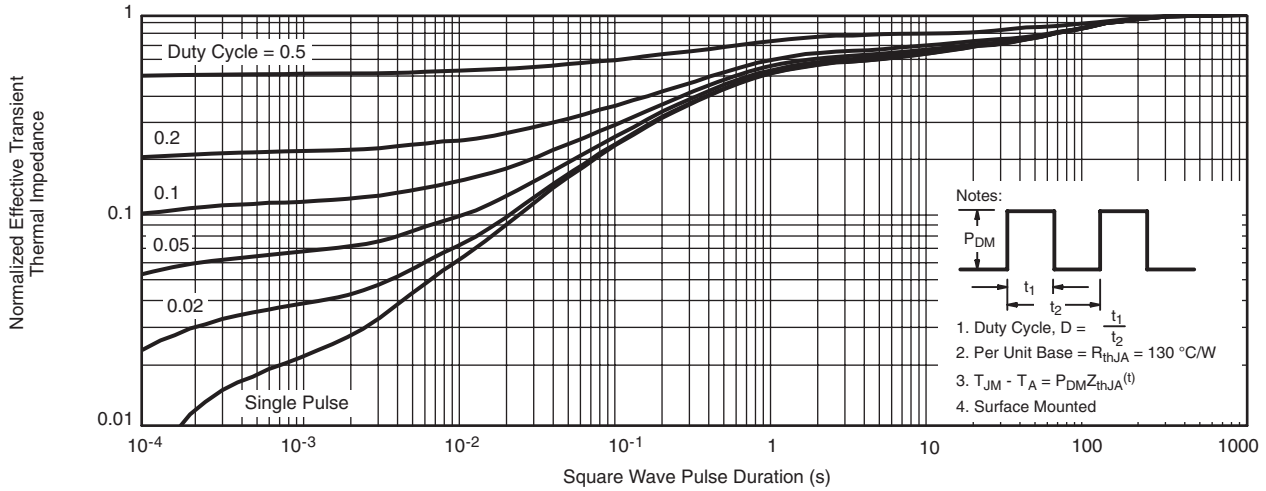
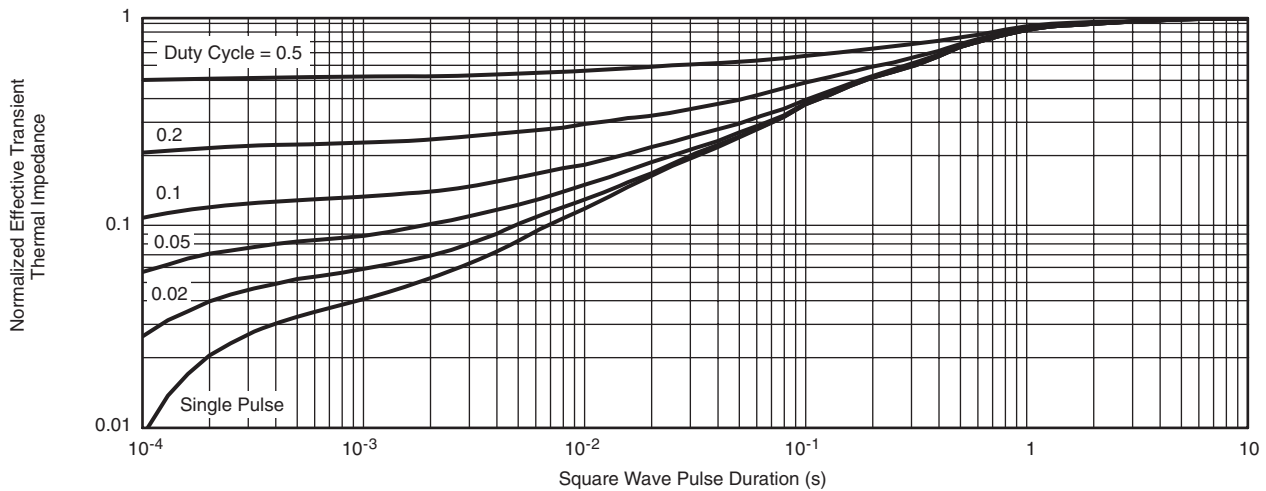
**TYPICAL CHARACTERISTICS** 25 °C, unless otherwise noted**On-Resistance vs. Junction Temperature****Source-Drain Diode Forward Voltage****On-Resistance vs. Gate-to-Source Voltage****Threshold Voltage****Single Pulse Power, Junction-to-Ambient*** $V_{GS} >$ minimum V_{GS} at which $R_{DS(on)}$ is specified**Safe Operating Area, Junction-to-Ambient**

**TYPICAL CHARACTERISTICS** 25 °C, unless otherwise noted

* The power dissipation P_D is based on $T_{J(max)} = 150$ °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

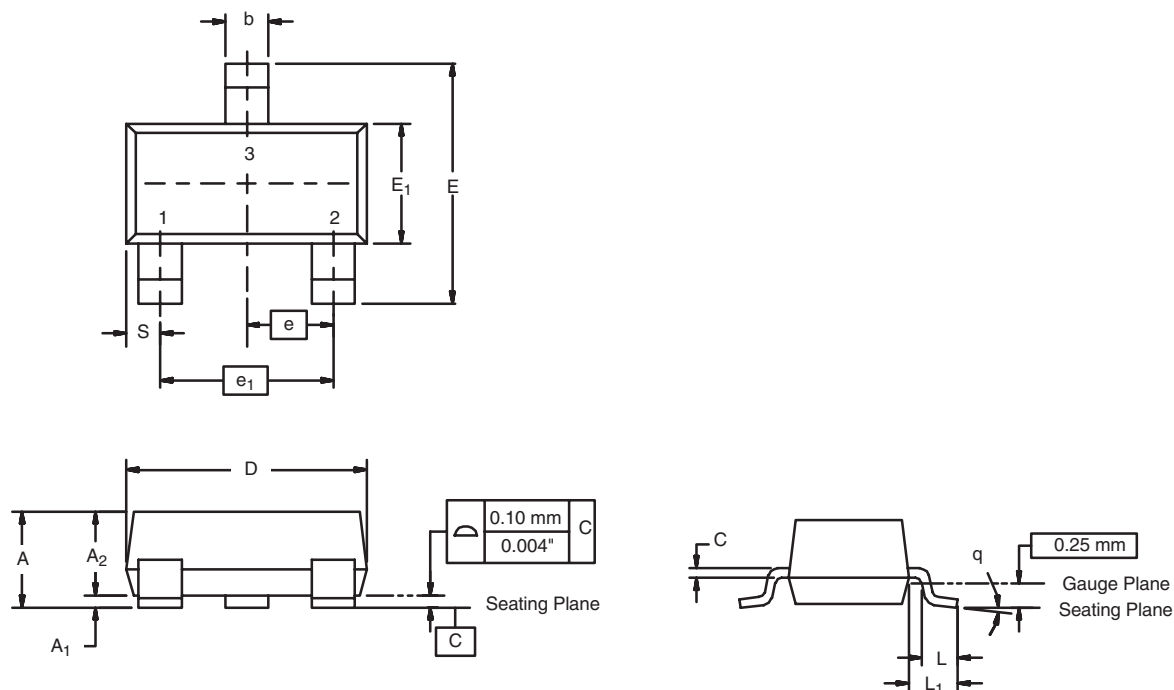
Si2377EDS

Vishay Siliconix

**TYPICAL CHARACTERISTICS** 25 °C, unless otherwise noted**Normalized Thermal Transient Impedance, Junction-to-Ambient****Normalized Thermal Transient Impedance, Junction-to-Foot**

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?65905.

SOT-23 (TO-236): 3-LEAD



Dim	MILLIMETERS		INCHES	
	Min	Max	Min	Max
A	0.89	1.12	0.035	0.044
A ₁	0.01	0.10	0.0004	0.004
A ₂	0.88	1.02	0.0346	0.040
b	0.35	0.50	0.014	0.020
c	0.085	0.18	0.003	0.007
D	2.80	3.04	0.110	0.120
E	2.10	2.64	0.083	0.104
E ₁	1.20	1.40	0.047	0.055
e	0.95 BSC		0.0374 Ref	
e ₁	1.90 BSC		0.0748 Ref	
L	0.40	0.60	0.016	0.024
L ₁	0.64 Ref		0.025 Ref	
S	0.50 Ref		0.020 Ref	
q	3°	8°	3°	8°
ECN: S-03946-Rev. K, 09-Jul-01				
DWG: 5479				

Mounting LITTLE FOOT® SOT-23 Power MOSFETs

Wharton McDaniel

Surface-mounted LITTLE FOOT power MOSFETs use integrated circuit and small-signal packages which have been modified to provide the heat transfer capabilities required by power devices. Leadframe materials and design, molding compounds, and die attach materials have been changed, while the footprint of the packages remains the same.

See Application Note 826, *Recommended Minimum Pad Patterns With Outline Drawing Access for Vishay Siliconix MOSFETs*, (<http://www.vishay.com/doc?72286>), for the basis of the pad design for a LITTLE FOOT SOT-23 power MOSFET footprint. In converting this footprint to the pad set for a power device, designers must make two connections: an electrical connection and a thermal connection, to draw heat away from the package.

The electrical connections for the SOT-23 are very simple. Pin 1 is the gate, pin 2 is the source, and pin 3 is the drain. As in the other LITTLE FOOT packages, the drain pin serves the additional function of providing the thermal connection from the package to the PC board. The total cross section of a copper trace connected to the drain may be adequate to carry the current required for the application, but it may be inadequate thermally. Also, heat spreads in a circular fashion from the heat source. In this case the drain pin is the heat source when looking at heat spread on the PC board.

Figure 1 shows the footprint with copper spreading for the SOT-23 package. This pattern shows the starting point for utilizing the board area available for the heat spreading copper. To create this pattern, a plane of copper overlies the drain pin and provides planar copper to draw heat from the drain lead and start the process of spreading the heat so it can be dissipated into the

ambient air. This pattern uses all the available area underneath the body for this purpose.

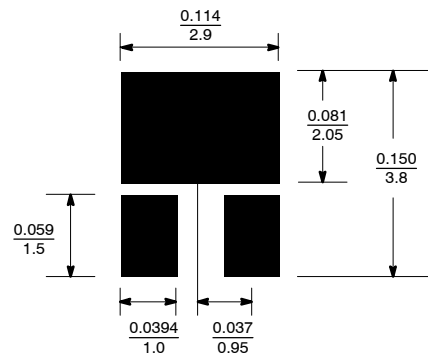
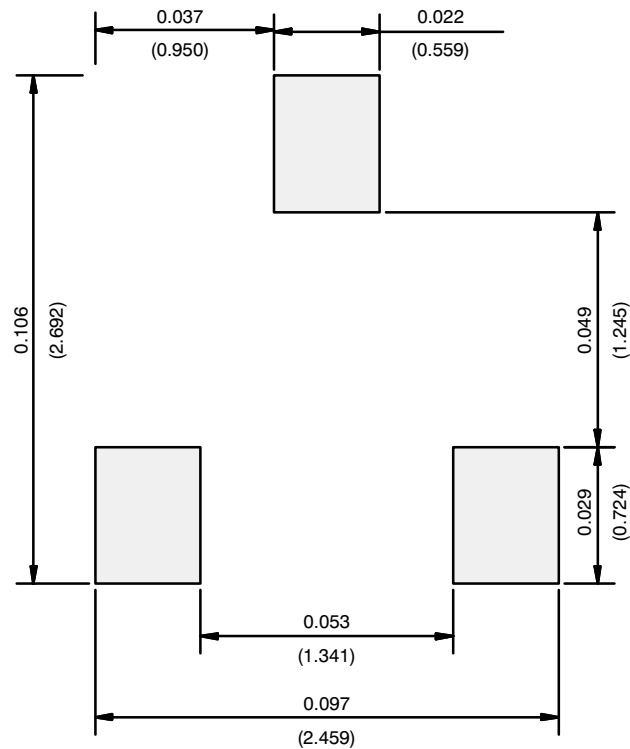


FIGURE 1. Footprint With Copper Spreading

Since surface-mounted packages are small, and reflow soldering is the most common way in which these are affixed to the PC board, "thermal" connections from the planar copper to the pads have not been used. Even if additional planar copper area is used, there should be no problems in the soldering process. The actual solder connections are defined by the solder mask openings. By combining the basic footprint with the copper plane on the drain pins, the solder mask generation occurs automatically.

A final item to keep in mind is the width of the power traces. The absolute minimum power trace width must be determined by the amount of current it has to carry. For thermal reasons, this minimum width should be at least 0.020 inches. The use of wide traces connected to the drain plane provides a low-impedance path for heat to move away from the device.

RECOMMENDED MINIMUM PADS FOR SOT-23



Recommended Minimum Pads
Dimensions in Inches/(mm)

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