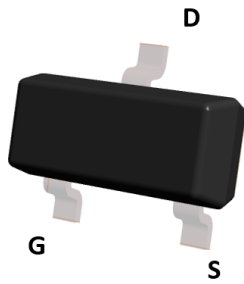
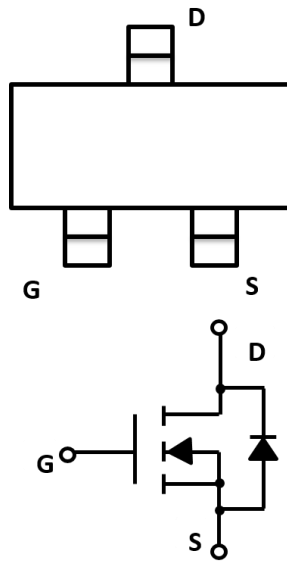


N-Channel Enhancement Mode Field Effect Transistor



Top View

SOT-23



Product Summary

- V_{DS} 100V
- I_D 2A
- $R_{DS(ON)}$ (at $V_{GS}=10V$) <280 mohm
- $R_{DS(ON)}$ (at $V_{GS}=4.5V$) <310 mohm

General Description

- Trench Power MV MOSFET technology
- Excellent package for heat dissipation
- High density cell design for low $R_{DS(ON)}$
- MSL LEVEL1

Applications

- DC-DC Converters
- Power management functions

■ Absolute Maximum Ratings ($T_A=25^\circ\text{C}$ unless otherwise noted)

Parameter		Symbol	Limit	Unit
Drain-source Voltage		V_{DS}	100	V
Gate-source Voltage		V_{GS}	± 20	V
Drain Current	$T_A=25^\circ\text{C}$	I_D	2	A
	$T_A=70^\circ\text{C}$		1.6	
Pulsed Drain Current ^A		I_{DM}	8	A
Total Power Dissipation @ $T_A=25^\circ\text{C}$		P_D	1.2	W
Thermal Resistance Junction-to-Ambient ^B		$R_{\theta JA}$	105	$^\circ\text{C}/\text{W}$
Junction and Storage Temperature Range		T_J, T_{STG}	-55~+150	$^\circ\text{C}$

■ Ordering Information (Example)

PREFERED P/N	PACKING CODE	Marking	MINIMUM PACKAGE(pcs)	INNER BOX QUANTITY(pcs)	OUTER CARTON QUANTITY(pcs)	DELIVERY MODE
YJL02N10A	F2	1002.	3000	30000	120000	7" reel



YJL02N10A

■ Electrical Characteristics (T_J=25℃ unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static Parameter						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} = 0V, I _D =250μA	100			V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =100V,V _{GS} =0V			1	μA
Gate-Body Leakage Current	I _{GSS1}	V _{GS} = ±20V, V _{DS} =0V			±100	nA
	I _{GSS2}	V _{GS} = ±10V, V _{DS} =0V			±50	nA
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D =250μA	1.0	1.8	3.0	V
Static Drain-Source On-Resistance	R _{DS(ON)}	V _{GS} = 10V, I _D =2A		250	280	mΩ
		V _{GS} = 4.5V, I _D =1.5A		260	310	
Diode Forward Voltage	V _{SD}	I _S =2A,V _{GS} =0V		0.8	1.2	V
Maximum Body-Diode Continuous Current	I _S				2	A
Dynamic Parameters						
Input Capacitance	C _{iss}	V _{DS} =50V,V _{GS} =0V,f=1MHZ		320		pF
Output Capacitance	C _{oss}			88		
Reverse Transfer Capacitance	C _{rss}			17		
Switching Parameters						
Total Gate Charge	Q _g	V _{GS} =10V,V _{DS} =50V,I _D =1.3A		5.3		nC
Gate-Source Charge	Q _{gs}			1.4		
Gate-Drain Charge	Q _{gd}			1.8		
Turn-on Delay Time	t _{D(on)}	V _{GS} =10V,V _{DD} =50V, I _D =1.3A,R _L =39Ω R _{GEN} =1Ω		14		ns
Turn-on Rise Time	t _r			54		
Turn-off Delay Time	t _{D(off)}			18		
Turn-off fall Time	t _f			11		

A. Pulse Test: Pulse Width≤300us, Duty cycle ≤2%.

B. Device mounted on FR-4 PCB, 1 inch x 0.85 inch x 0.062 inch.

■ Typical Performance Characteristics

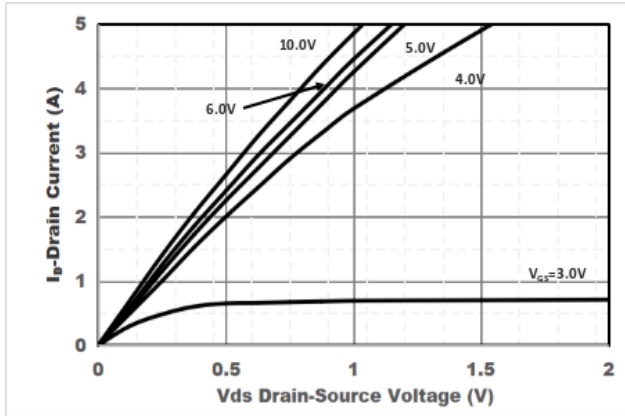


Figure1. Output Characteristics

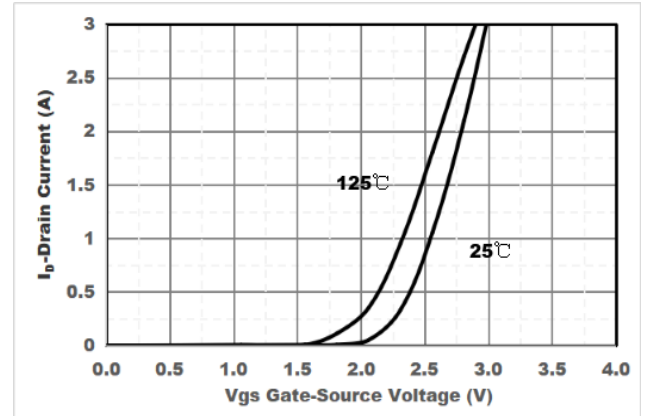


Figure2. Transfer Characteristics

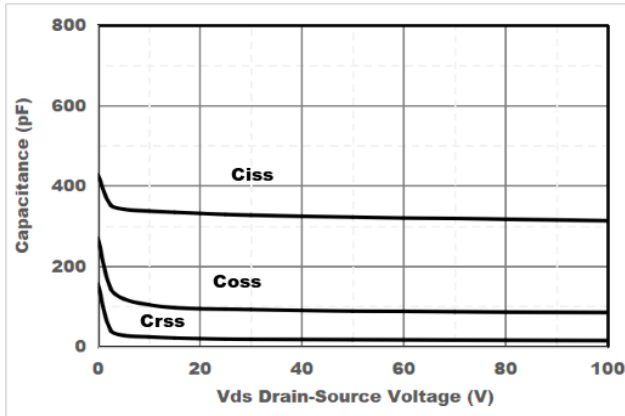


Figure3. Capacitance Characteristics

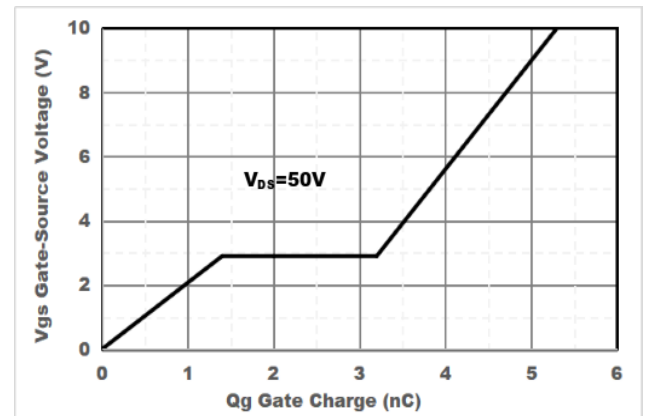


Figure4. Gate Charge

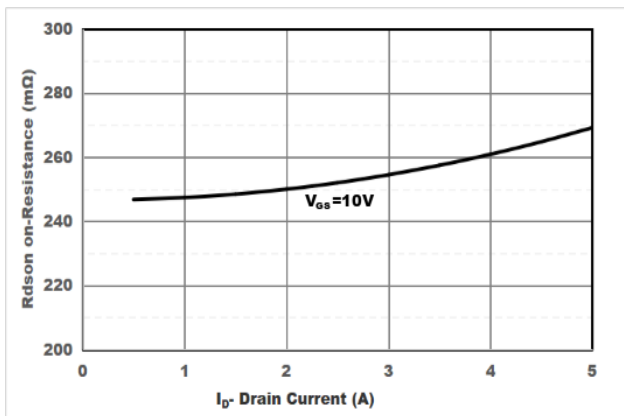


Figure5. Drain-Source on Resistance

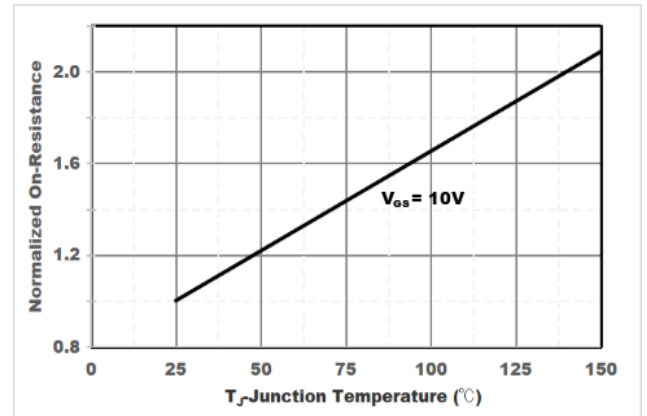


Figure6. Drain-Source on Resistance

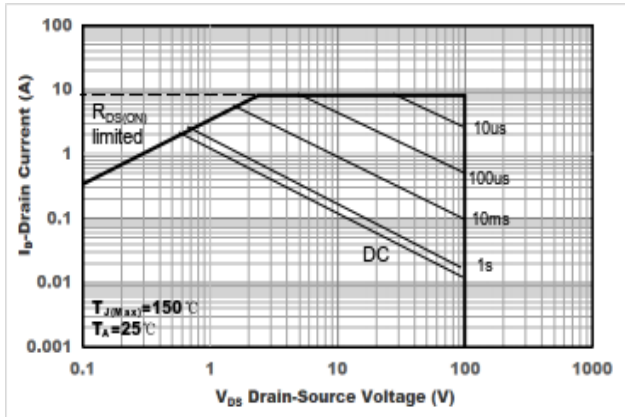


Figure7. Safe Operation Area

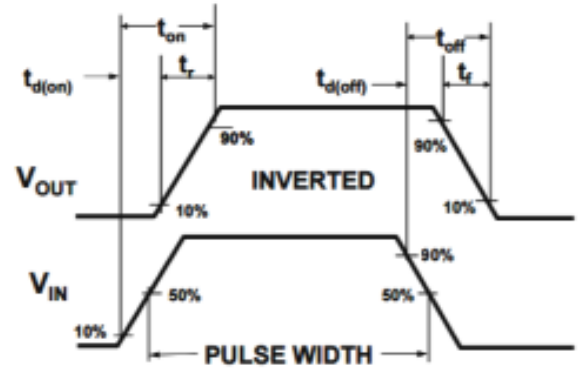
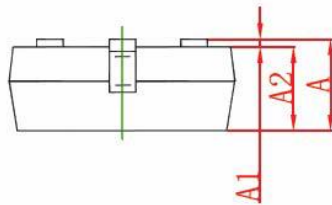
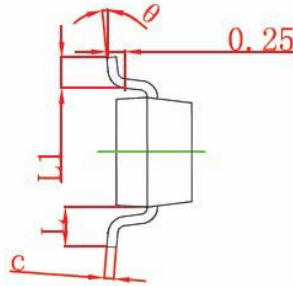
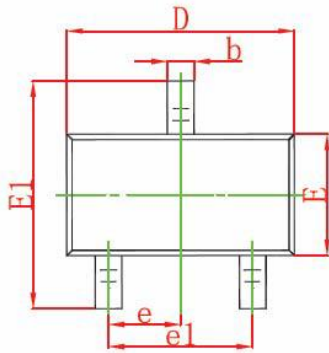


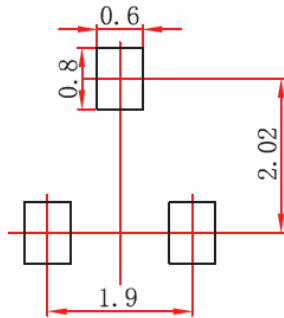
Figure8. Switching wave

■ SOT-23 Package information



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.900	1.150	0.035	0.045
A1	0.000	0.100	0.000	0.004
A2	0.900	1.050	0.035	0.041
b	0.300	0.500	0.012	0.020
c	0.080	0.150	0.003	0.006
D	2.800	3.000	0.110	0.118
E	1.200	1.400	0.047	0.055
E1	2.250	2.550	0.089	0.100
e	0.950 TYP		0.037 TYP	
e1	1.800	2.000	0.071	0.079
L	0.550 REF		0.022 REF	
L1	0.300	0.500	0.012	0.020
θ	0°	8°	0°	8°

■ SOT-23 Suggested Pad Layout



Note:

1. Controlling dimension: in millimeters.
2. General tolerance: $\pm 0.05\text{mm}$.
3. The pad layout is for reference purposes only.



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