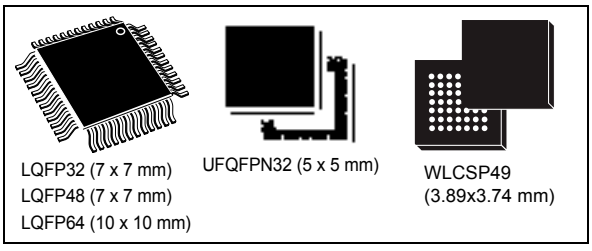
STM32F334x4 STM32F334x6 STM32F334x8

Arm®Cortex®-M4 32b MCU+FPU,up to 64KB Flash,16KB SRAM, 2 ADCs,3 DACs,3 comp.,op-amp, 217ps 10-ch (HRTIM1)

Datasheet - production data

Features

- Core: Arm® Cortex®-M4 32-bit CPU with FPU (72 MHz max), single-cycle multiplication and HW division DSP instruction
- Memories
  - Up to 64 Kbytes of Flash memory
  - Up to 12 Kbytes of SRAM with HW parity check
  - Routine booster: 4 Kbytes of SRAM on instruction and data bus with HW parity check (CCM)
- CRC calculation unit
- Reset and supply management
  - Low-power modes: Sleep, Stop, Standby
  - $V_{DD,}V_{DDA}$ voltage range: 2.0 to 3.6 V
  - Power-on/Power-down reset (POR/PDR)
  - Programmable voltage detector (PVD)
  - V_{BAT} supply for RTC and backup registers
- Clock management
  - 4 to 32 MHz crystal oscillator
  - 32 kHz oscillator for RTC with calibration
  - Internal 8 MHz RC (up to 64 MHz with PLL option)
  - Internal 40 kHz oscillator
- Up to 51 fast I/O ports, all mappable on external interrupt vectors, several 5 V-tolerant
- Interconnect matrix
- 7-channel DMA controller
- Up to two ADC 0.20 µs (up to 21 channels) with selectable resolution of 12/10/8/6 bits, 0 to 3.6 V conversion range, single-ended / differential mode, separate analog supply from 2.0 to 3.6 V
- Temperature sensor
- Up to three 12-bit DAC channels with analog supply from 2.4 V to 3.6 V



- Three ultra-fast rail-to-rail analog comparators with analog supply from 2 to 3.6 V
- One operational amplifiers that can be used in PGA mode, all terminals accessible with analog supply from 2.4 to 3.6 V
- Up to 18 capacitive sensing channels supporting touchkeys, linear and rotary touch sensors
- Up to 12 timers
  - HRTIM: 6 x16-bit counters, 217 ps resolution, 10 PWM, 5 fault inputs, 10 ext event input, 1 synchro. input,1 synchro. out
  - One 32-bit timer and one 16-bit timer with up to 4 IC/OC/PWM or pulse counter and quadrature (incremental) encoder input
  - One 16-bit 6-channel advanced-control timer, with up to 6 PWM channels, deadtime generation and emergency stop
  - One 16-bit timer with 2 IC/OCs, 1 OCN/PWM, deadtime generation, emergency stop
  - Two 16-bit timers with IC/OC/OCN/PWM, deadtime generation and emergency stop
  - Two watchdog timers (independent, window)
  - SysTick timer: 24-bit downcounter
  - Up to two 16-bit basic timers to drive DAC
- Calendar RTC with alarm, periodic wakeup from Stop
- Communication interfaces
  - CAN interface (2.0 B Active) and one SPI

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- One I^2C with 20 mA current sink to support Fast mode plus, SMBus/PMBus
- Up to 3 USARTs, one with ISO/IEC 7816 interface, LIN, IrDA, modem control

- Debug mode: serial wire debug (SWD), JTAG
- 96-bit unique ID
- All packages ECOPACK®2 compliant

Table 1. Device summary

Reference	Part number
STM32F334Kx	STM32F334K4/K6/K8
STM32F334Cx	STM32F334C4/C6/C8
STM32F334Rx	STM32F334R6/R8

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1 Introduction

This datasheet provides the ordering information and the mechanical device characteristics of the STM32F334x4/6/8 microcontrollers.

This document must be read in conjunction with the STM32F334xx, reference manual (RM0364) available from the STMicroelectronics website *www.st.com*.

For information on the Cortex®-M4 core with FPU, refer to:

- Arm®[a] Cortex®-M4 Processor Technical Reference Manual available from the www.arm.com website.
- STM32F3xxx and STM32F4xxx Cortex®-M4 programming manual (PM0214) available from the *www.st.com* website.

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2 Description

The STM32F334x4/6/8 family incorporates the high-performance Arm® Cortex®-M4 32-bit RISC core operating at up to 72 MHz frequency embedding a floating point unit (FPU), high-speed embedded memories (up to 64 Kbytes of Flash memory, up to 12 Kbytes of SRAM), and an extensive range of enhanced I/Os and peripherals connected to two APB buses.

The STM32F334x4/6/8 microcontrollers offer two fast 12-bit ADCs (5 Msps), up to three ultra-fast comparators, an operational amplifier, three DAC channels, a low-power RTC, one high-resolution timer, one general-purpose 32-bit timer, one timer dedicated to motor control, and four general-purpose 16-bit timers. They also feature standard and advanced communication interfaces: one I^2C, one SPI, up to three USARTs and one CAN.

The STM32F334x4/6/8 family operates in the –40 to +85 °C and –40 to +105 °C temperature ranges from 2.0 to 3.6 V power supply. A comprehensive set of power-saving modes allow the design of low-power applications.

The STM32F334x4/6/8 family offers devices in 32, 48 and 64-pin packages.

Depending on the device chosen, different sets of peripherals are included.

Table 2. STM32F334x4/6/8 family device features and peripheral counts

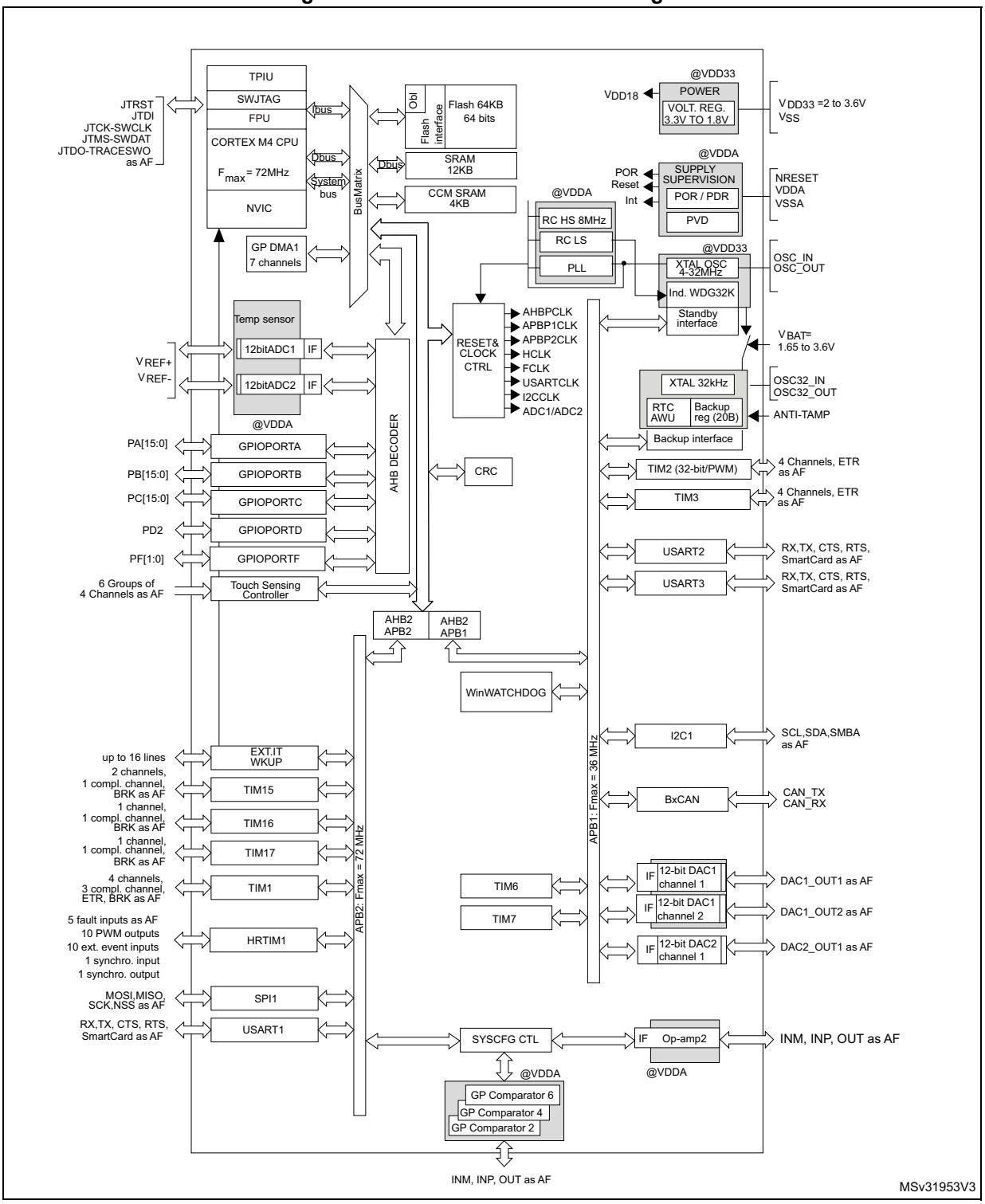
Peripheral		STM32F334Kx			STM32F334Cx			STM32F334Rx		
Flash memory (Kbyte)		16	32	64	16	32	64	16	32	64
SRAM on data bus (Kbyte)		12								
Core coupled memory SRAM on instruction bus (CCM SRAM) (Kbyte)		4								
Timers	High-resolution timer	1 (16-bit / 10 channels)								
	Advanced control	1 (16-bit)								
	General purpose	4 (16-bit) 1 (32 bit)								
	Basic	2 (16-bit)								
	SysTick timer	1								
	Watchdog timers (independent, window)	2								
	PWM channels (all)(1)	20			26			28		
	PWM channels (except complementary)	14			20			22		

Table 2. STM32F334x4/6/8 family device features and peripheral counts (continued)

Peripheral		STM32F334Kx	STM32F334Cx	STM32F334Rx
Comm. interfaces	SPI	1		
	I^2C	1		
	USART	2	3	
	CAN	1		
GPIOs	Normal I/Os (TC, TTa)	10	20	26
	5-Volt tolerant I/Os (FT,FTf)	15	17	25
Capacitive sensing channels		14	17	18
DMA channels		7		
12-bit ADCs Number of channels		2 10	2 15	2 21
12-bit DAC channels		3		
Ultra-fast analog comparator		2	3	
Operational amplifiers		1		
CPU frequency		72 MHz		
Operating voltage		2.0 to 3.6 V		
Operating temperature		Ambient operating temperature: - 40 to 85 °C / - 40 to 105 °C Junction temperature: - 40 to 125 °C		
Packages		LQFP32, UFQFPN32	LQFP48, WLCSP49	LQFP64

1. This total considers also the PWMs generated on the complementary output channels.

Figure 1. STM32F334x4/6/8 block diagram



1. AF: alternate function on I/O pins.

3 Functional overview

3.1 Arm® Cortex®-M4 core with FPU with embedded Flash memory and SRAM

The Arm Cortex-M4 processor with FPU is the latest generation of Arm processors for embedded systems. It has been developed to provide a low-cost platform that meets the needs of MCU implementation, with a reduced pin count and low-power consumption, while delivering outstanding computational performance and an advanced response to interrupts.

The Arm 32-bit Cortex-M4 RISC processor with FPU features exceptional code-efficiency, delivering the high performance expected from an Arm core, with memory sizes usually associated with 8- and 16-bit devices.

The processor supports a set of DSP instructions that allows efficient signal processing and complex algorithm execution.

Its single precision FPU speeds up software development by using metalanguage development tools, while avoiding saturation.

With its embedded Arm core, the STM32F334x4/6/8 family is compatible with all Arm tools and software.

Figure 1 shows the general block diagram of the STM32F334x4/6/8 family devices.

3.2 Memories

3.2.1 Embedded Flash memory

All STM32F334x4/6/8 devices feature up to 64 Kbytes of embedded Flash memory available for storing programs and data. The Flash memory access time is adjusted to the CPU clock frequency (0 wait state from 0 to 24 MHz, 1 wait state from 24 to 48 MHz and 2 wait states above).

3.2.2 Embedded SRAM

The STM32F334x4/6/8 devices feature up to 12 Kbytes of embedded SRAM with hardware parity check. The memory can be accessed in read/write at CPU clock speed with 0 wait states, allowing the CPU to achieve 90 Dhrystone Mips at 72 MHz when running code from CCM (core coupled memory) RAM.

The SRAM is organized as follows:

- 4 Kbytes of SRAM on instruction and data bus with parity check (core coupled memory or CCM) and used to execute critical routines or to access data
- 12 Kbytes of SRAM with parity check mapped on the data bus

3.2.3 Boot modes

At startup, BOOT0 pin and BOOT1 option bit are used to select one of the three boot options:

- Boot from user Flash memory
- Boot from system memory
- Boot from embedded SRAM

The boot loader is located in system memory. It is used to reprogram the Flash memory by using USART1 (PA9/PA10), USART2 (PA2/PA3), I2C1 (PB6/PB7).

3.3 Cyclic redundancy check calculation unit (CRC)

The CRC (cyclic redundancy check) calculation unit is used to get a CRC code using a configurable generator polynomial value and size.

Among other applications, CRC-based techniques are used to verify data transmission or storage integrity. In the scope of the EN/IEC 60335-1 standard, they offer a means of verifying the Flash memory integrity. The CRC calculation unit helps to compute a signature of the software during runtime, to be compared with a reference signature generated at link-time and stored at a given memory location.

3.4 Power management

3.4.1 Power supply schemes

- V_{SS}, V_{DD} = 2.0 to 3.6 V: external power supply for I/Os and the internal regulator. It is provided externally through V_{DD} pins.
- V_{SSA}, V_{DDA} = 2.0 to 3.6 V: external analog power supply for ADC, DACs, comparators operational amplifiers, reset blocks, RCs and PLL.The minimum voltage to be applied to V_{DDA} differs from one analog peripherals to another. See *Table 3* below, summarizing the V_{DDA} ranges for analog peripherals. The V_{DDA} voltage level must be always greater or equal to the V_{DD} voltage level and must be provided first.
- V_{DD18} = 1.65 to 1.95 V (V_{DD18} domain): power supply for digital core, SRAM and Flash memory. V_{DD18} is internally generated through an internal voltage regulator.

Table 3. V_{DDA} ranges for analog peripherals

Analog peripheral	Min. V_{DDA}supply	Max. V_{DDA}supply
ADC/COMP	2 V	3.6 V
DAC/OPAMP	2.4 V	3.6 V

- V_{BAT} = 1.65 to 3.6 V: power supply for RTC, external clock 32 kHz oscillator and backup registers (through power switch) when V_{DD} is not present.

3.4.2 Power supply supervisor

The device has an integrated power-on reset (POR) and power-down reset (PDR) circuits. They are always active, and ensure proper operation above a threshold of 2 V. The device

remains in reset mode when the monitored supply voltage is below a specified threshold, $V_{POR/PDR}$, without the need for an external reset circuit.

- The POR monitors only the V_{DD} supply voltage. During the startup phase it is required that V_{DDA} must arrive first and be greater than or equal to V_{DD}.
- The PDR monitors both the V_{DD} and V_{DDA} supply voltages, however the V_{DDA} power supply supervisor can be disabled (by programming a dedicated Option bit) to reduce the power consumption if the application design ensures that V_{DDA} is higher than or equal to V_{DD}.

The device features an embedded programmable voltage detector (PVD) that monitors the V_{DD} power supply and compares it to the V_{PVD} threshold. An interrupt can be generated when V_{DD} drops below the V_{PVD} threshold and/or when V_{DD} is higher than the V_{PVD} threshold. The interrupt service routine can then generate a warning message and/or put the MCU into a safe state. The PVD is enabled by software.

3.4.3 Voltage regulator

The regulator has three operation modes: main (MR), low-power (LPR), and power-down.

- The MR mode is used in the nominal regulation mode (Run)
- The LPR mode is used in Stop mode.
- The power-down mode is used in Standby mode: the regulator output is in high impedance, and the kernel circuitry is powered down thus inducing zero consumption.

The voltage regulator is always enabled after reset. It is disabled in Standby mode.

3.4.4 Low-power modes

The STM32F334x4/6/8 supports three low-power modes to achieve the best compromise between low power consumption, short startup time and available wakeup sources:

- **Sleep mode**

  In Sleep mode, only the CPU is stopped. All peripherals continue to operate and can wake up the CPU when an interrupt/event occurs.
- **Stop mode**

  Stop mode achieves the lowest power consumption while retaining the content of SRAM and registers. All clocks in the 1.8 V domain are stopped, the PLL, the HSI RC and the HSE crystal oscillators are disabled. The voltage regulator can also be put either in normal or in low-power mode.

  The device can be woken up from Stop mode by any of the EXTI line. The EXTI line source can be one of the 16 external lines, the PVD output, the RTC alarm, COMPx, I^2C or USARTx.
- **Standby mode**

  The Standby mode is used to achieve the lowest power consumption. The internal voltage regulator is switched off so that the entire 1.8 V domain is powered off. The PLL, the HSI RC and the HSE crystal oscillators are also switched off. After entering Standby mode, SRAM and register contents are lost except for registers in the Backup domain and Standby circuitry.

  The device exits Standby mode when an external reset (NRST pin), an IWDG reset, a rising edge on the WKUP pin, or an RTC alarm occurs.

Note: The RTC, the IWDG, and the corresponding clock sources are not stopped by entering Stop or Standby mode.

3.5 Interconnect matrix

Several peripherals have direct connections between them. This allows autonomous communication between peripherals, saving CPU resources thus power supply consumption. In addition, these hardware connections allow fast and predictable latency.

Table 4. STM32F334x4/6/8 peripheral interconnect matrix

Interconnect source	Interconnect destination	Interconnect action
TIMx	TIMx	Timers synchronization or chaining
	ADCx DACx	Conversion triggers
	DMA	Memory to memory transfer trigger
	COMPx	Comparator output blanking
COMPx	TIMx	Timer input: ocrefclear input, input capture
ADCx	TIM/HRTIM1	Timer triggered by analog watchdog
GPIO RTCCLK HSE/32 MC0	TIM16	Clock source used as input channel for HSI and LSI calibration
CSS CPU (hard fault) RAM (parity error) COMPx PVD GPIO	TIM1 TIM15, 16, 17	Timer break
GPIO	TIMx	External trigger, timer break
	ADCx DACx	Conversion external trigger
DACx	COMPx	Comparator inverting input
HRTIM1	DACx/ADCx	Conversion trigger
COMPx	HRTIM1	COMPx output is an input event or a fault input for HRTIM1
OPAMP2	HRTIM1	OPAMP2 output is an input event for HRTIM1
GPIO	HRTIM1	External fault/event/ Synchro inputs for HRTIM1
HRTIM1	GPIO	Synchro output for HRTIM1

Note: For more details about the interconnect actions, refer to the corresponding sections in the RM0364 reference manual.

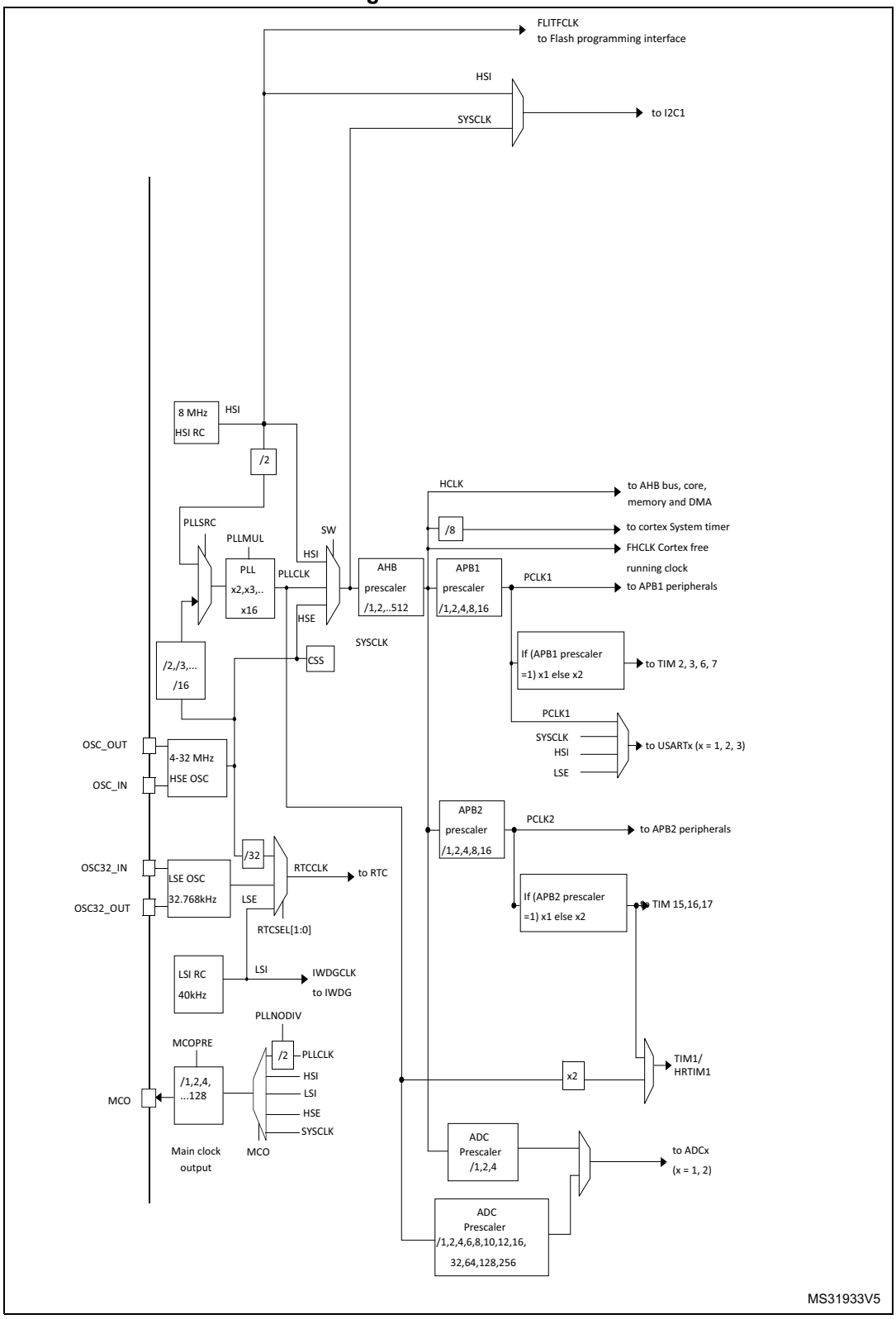
3.6 Clocks and startup

System clock selection is performed on startup, however the internal RC 8 MHz oscillator is selected on reset as default CPU clock. An external 4-32 MHz clock can be selected, in which case it is monitored for failure. If failure is detected, the system automatically switches back to the internal RC oscillator. A software interrupt is generated if enabled. Similarly, full interrupt management of the PLL clock entry is available when necessary (for example with failure of an indirectly used external oscillator).

Several prescalers allow to configure the AHB frequency, the high-speed APB (APB2) and the low-speed APB (APB1) domains. The maximum frequency of the AHB and the high-speed APB domains is 72 MHz, while the maximum allowed frequency of the low-speed APB domain is 36 MHz.

TIM1and HRTIM1 maximum frequency is 144 MHz.

Figure 2. Clock tree



3.7 General-purpose inputs/outputs (GPIOs)

Each of the GPIO pins can be configured by software as output (push-pull or open-drain), as input (with or without pull-up or pull-down) or as peripheral alternate function. Most of the GPIO pins are shared with digital or analog alternate functions. All GPIOs are high current capable except for analog inputs.

The I/Os alternate function configuration can be locked if needed, following a specific sequence to avoid spurious writing to the I/Os registers.

Fast I/O handling allows I/O toggling up to 36 MHz.

3.8 Direct memory access (DMA)

The flexible general-purpose DMA is able to manage memory-to-memory, peripheral-to-memory and memory-to-peripheral transfers. The DMA controller supports circular buffer management, avoiding the generation of interrupts when the controller reaches the end of the buffer.

Each of the 7 DMA channels is connected to dedicated hardware DMA requests, with software trigger support for each channel. Configuration is done by software and transfer sizes between source and destination are independent.

The DMA can be used with the main peripherals: SPI, I^2C, USART, general-purpose timers, high-resolution timer, DAC and ADC.

3.9 Interrupts and events

3.9.1 Nested vectored interrupt controller (NVIC)

The STM32F334x4/6/8 devices embed a nested vectored interrupt controller (NVIC) able to handle up to 60 interrupt channels that can be masked and 16 priority levels.

The NVIC benefits are the following:

- Closely coupled NVIC gives low latency interrupt processing
- Interrupt entry vector table address passed directly to the core
- Closely coupled NVIC core interface
- Allows early processing of interrupts
- Processing of late arriving higher priority interrupts
- Support for tail chaining
- Processor state automatically saved on interrupt entry and restored on interrupt exit with no instruction overhead

The NVIC hardware block provides flexible interrupt management features with minimal interrupt latency.

3.9.2 Extended interrupt/event controller (EXTI)

The external interrupt/event controller consists of 27 edge detector lines used to generate interrupt/event requests and wake-up the system. Each line can be independently configured to select the trigger event (rising edge, falling edge, both) and can be masked

independently. A pending register maintains the status of the interrupt requests. The EXTI can detect an external line with a pulse width shorter than the internal clock period. Up to 51 GPIOs can be connected to the 16 external interrupt lines.

3.10 Fast analog-to-digital converter (ADC)

Two 5 MSPS fast analog-to-digital converters, with selectable resolution between 12 and 6 bit, are embedded in the STM32F334x4/6/8 family devices. The ADCs have up to 21 external channels. Some of the external channels are shared between ADC1 and ADC2, performing conversions in single-shot or scan modes. The channels can be configured to be either single-ended input or differential input. In scan mode, automatic conversion is performed on a selected group of analog inputs.

The ADCs also have internal channels: temperature sensor connected to ADC1 channel 16, $V_{BAT}/2$ connected to ADC1 channel 17, voltage reference V_{REFINT} connected to both ADC1 and ADC2 channel 18 and VOPAMP2 connected to ADC2 channel 17.

Additional logic functions embedded in the ADC interface allow:

- Simultaneous sample and hold
- Interleaved sample and hold
- Single-shunt phase current reading techniques.

Three analog watchdogs are available per ADC. The ADC can be served by the DMA controller.

The analog watchdog feature allows very precise monitoring of the converted voltage of one, some or all selected channels. An interrupt is generated when the converted voltage is outside the programmed thresholds.

The events generated by the general-purpose timers (TIM2, TIM3, TIM6, TIM15), the advanced-control timer (TIM1) and the High-resolution timer (HRTIM1) can be internally connected to the ADC start trigger and injection trigger, respectively, to allow the application to synchronize A/D conversion and timers.

3.10.1 Temperature sensor

The temperature sensor (TS) generates a voltage V_{SENSE} that varies linearly with temperature.

The temperature sensor is internally connected to the ADC1_IN16 input channel that is used to convert the sensor output voltage into a digital value.

The sensor provides good linearity but it has to be calibrated to obtain good overall accuracy of the temperature measurement. As the offset of the temperature sensor varies from chip to chip due to process variation, the uncalibrated internal temperature sensor is suitable for applications that detect temperature changes only.

To improve the accuracy of the temperature sensor measurement, each device is individually factory-calibrated by ST. The temperature sensor factory calibration data are stored by ST in the system memory area, accessible in read-only mode.

3.10.2 Internal voltage reference (VREFINT)

The internal voltage reference (V_{REFINT}) provides a stable (bandgap) voltage output for the ADC and Comparators. V_{REFINT} is internally connected to the ADC1_IN18 and ADC2_IN18

input channels. The precise voltage of V_{REFINT} is individually measured for each part by ST during production test and stored in the system memory area. It is accessible in read-only mode.

3.10.3 V_{BAT} battery voltage monitoring

This embedded hardware feature allows the application to measure the V_{BAT} battery voltage using the internal ADC channel ADC1_IN17. As the V_{BAT} voltage may be higher than V_{DDA}, and thus outside the ADC input range, the V_{BAT} pin is internally connected to a bridge divider by 2. As a consequence, the converted digital value is half the V_{BAT} voltage.

3.10.4 OPAMP2 reference voltage (VOPAMP2)

OPAMP2 reference voltage can be measured using ADC2 internal channel 17.

3.11 Digital-to-analog converter (DAC)

One 12-bit buffered DAC channel (DAC1_OUT1) and two 12-bit unbuffered DAC channels (DAC1_OUT2 and DAC2_OUT1) can be used to convert digital signals into analog voltage signal outputs. The chosen design structure is composed of integrated resistor strings and an amplifier in inverting configuration.

This digital interface supports the following features:

- Three DAC output channels
- 8-bit or 12-bit monotonic output
- Left or right data alignment in 12-bit mode
- Synchronized update capability
- Noise-wave generation (only on DAC1)
- Triangular-wave generation (only on DAC1)
- Dual DAC channel independent or simultaneous conversions
- DMA capability for each channel
- External triggers for conversion

3.12 Operational amplifier (OPAMP)

The STM32F334x4/6/8 embeds an operational amplifier (OPAMP2) with external or internal follower routing and PGA capability (or even amplifier and filter capability with external components). When an operational amplifier is selected, an external ADC channel is used to enable output measurement.

The operational amplifier features:

- 8 MHz GBP
- 0.5 mA output capability
- Rail-to-rail input/output
- In PGA mode, the gain can be programmed to 2, 4, 8 or 16.

3.13 Ultra-fast comparators (COMP)

The STM32F334x4/6/8 devices embed three ultra-fast rail-to-rail comparators (COMP2/4/6) that offer the features below:

- Programmable internal or external reference voltage
- Selectable output polarity.

The reference voltage can be one of the following:

- External I/O
- DAC output
- Internal reference voltage or submultiple (1/4, 1/2, 3/4). Refer to *Table 23: Embedded internal reference voltage* for values and parameters of the internal reference voltage.

All comparators can wake up from STOP mode, generate interrupts and breaks for the timers.

3.14 Timers and watchdogs

The STM32F334x4/6/8 includes advanced control timer, 5 general-purpose timers, basic timer, two watchdog timers and a SysTick timer. The table below compares the features of the advanced control, general purpose and basic timers.

Table 5. Timer feature comparison

Timer type	Timer	Counter resolution	Counter type	Prescaler factor	DMA request generation	Capture/ compare channels	Complementary outputs
High-resolution timer	HRTIM1(1)	16-bit	Up	/1 /2 /4 (x2 x4 x8 x16 x32, with DLL)	Yes	10	Yes
Advanced control	TIM1(1)	16-bit	Up, Down, Up/Down	Any integer between 1 and 65536	Yes	4	Yes
General-purpose	TIM2	32-bit	Up, Down, Up/Down	Any integer between 1 and 65536	Yes	4	No
General-purpose	TIM3	16-bit	Up, Down, Up/Down	Any integer between 1 and 65536	Yes	4	No
General-purpose	TIM15	16-bit	Up	Any integer between 1 and 65536	Yes	2	1
General-purpose	TIM16, TIM17	16-bit	Up	Any integer between 1 and 65536	Yes	1	1
Basic	TIM6, TIM7	16-bit	Up	Any integer between 1 and 65536	Yes	0	No

1. TIM1 can be clocked from the PLL x 2 running at 144 MHz .

3.14.1 217 ps high-resolution timer (HRTIM1)

The high-resolution timer (HRTIM1) allows generating digital signals with high-accuracy timings, such as PWM or phase-shifted pulses.

It consists of 6 timers, 1 master and 5 slaves, totaling 10 high-resolution outputs, which can be coupled by pairs for deadtime insertion. It also features 5 fault inputs for protection purposes and 10 inputs to handle external events such as current limitation, zero voltage or zero current switching.

HRTIM1 timer is made of a digital kernel clocked at 144 MHz followed by delay lines. Delay lines with closed loop control guarantee a 217 ps resolution whatever the voltage, temperature or chip-to-chip manufacturing process deviation. The high-resolution is available on the 10 outputs in all operating modes: variable duty cycle, variable frequency, and constant ON time.

The slave timers can be combined to control multiswitch complex converters or operate independently to manage multiple independent converters.

The waveforms are defined by a combination of user-defined timings and external events such as analog or digital feedbacks signals.

HRTIM1 timer includes options for blanking and filtering out spurious events or faults. It also offers specific modes and features to offload the CPU: DMA requests, burst mode controller, push-pull and resonant mode.

It supports many topologies including LLC, Full bridge phase shifted, buck or boost converters, either in voltage or current mode, as well as lighting application (fluorescent or LED). It can also be used as a general purpose timer, for instance to achieve high-resolution PWM-emulated DAC.

In debug mode, the HRTIM1 counters can be frozen and the PWM outputs enter safe state.

3.14.2 Advanced timer (TIM1)

The advanced-control timer can be seen as a three-phase PWM multiplexed on 6 channels. They have complementary PWM outputs with programmable inserted dead-times. They can also be seen as complete general-purpose timers. The 4 independent channels can be used for:

- Input capture
- Output compare
- PWM generation (edge or center-aligned modes) with full modulation capability (0-100%)
- One-pulse mode output

In debug mode, the advanced-control timer counter can be frozen and the PWM outputs disabled to turn off any power switches driven by these outputs.

Many features are shared with those of the general-purpose TIM timers (described in *Section 3.14.3*) using the same architecture, so the advanced-control timers can work together with the TIM timers via the Timer Link feature for synchronization or event chaining.

3.14.3 General-purpose timers (TIM2, TIM3, TIM15, TIM16 and TIM17)

There are up to three general-purpose timers embedded in the STM32F334x4/6/8 (see *Table 5* for differences) that can be synchronized. Each general-purpose timer can be used to generate PWM outputs, or act as a simple time base.

- TIM2 and TIM3

  They are full-featured general-purpose timers:

  – TIM2 has a 32-bit auto-reload up/down counter and 32-bit prescaler

  – TIM3 has a 16-bit auto-reload up/down counter and 16-bit prescaler

  These timers feature four independent channels for input capture/output compare, PWM or one-pulse mode output. They can work together, or with the other general-purpose timers via the Timer Link feature for synchronization or event chaining.

  The counters can be frozen in debug mode.

  All have independent DMA request generation and support quadrature encoders.

- TIM15, 16 and 17

  They are three general-purpose timers with mid-range features.

  They have 16-bit auto-reload upcounters and 16-bit prescalers.

  – TIM15 has two channels and one complementary channel

  – TIM16 and TIM17 have one channel and one complementary channel

  All channels can be used for input capture/output compare, PWM or one-pulse mode output.

  The timers can work together via the Timer Link feature for synchronization or event chaining. The timers have independent DMA request generation.

  The counters can be frozen in debug mode.

3.14.4 Basic timers (TIM6 and TIM7)

The basic timers are mainly used for DAC trigger generation. They can also be used as generic 16-bit timebases.

3.14.5 Independent watchdog

The independent watchdog is based on a 12-bit downcounter and 8-bit prescaler. It is clocked from an independent 40 kHz internal RC and as it operates independently from the main clock, it can operate in Stop and Standby modes. It can be used either as a watchdog to reset the device when a problem occurs, or as a free running timer for application timeout management. It is hardware or software configurable through the option bytes. The counter can be frozen in debug mode.

3.14.6 Window watchdog

The window watchdog is based on a 7-bit downcounter that can be set as free running. It can be used as a watchdog to reset the device when a problem occurs. It is clocked from the main clock. It has an early warning interrupt capability and the counter can be frozen in debug mode.

3.14.7 SysTick timer

This timer is dedicated to real-time operating systems, but could also be used as a standard down counter. It features:

- A 24-bit down counter
- Auto reload capability
- Maskable system interrupt generation when the counter reaches 0.
- Programmable clock source

3.15 Real-time clock (RTC) and backup registers

The RTC and the 5 backup registers are supplied through a switch that takes power from either the V_{DD} supply when present or the VBAT pin. The backup registers are five 32-bit registers used to store 20 bytes of user application data when V_{DD} power is not present.

They are not reset by a system or power reset, or when the device wakes up from Standby mode.

The RTC is an independent BCD timer/counter. It supports the following features:

- Calendar with subsecond, seconds, minutes, hours (12 or 24 format), week day, date, month, year, in BCD (binary-coded decimal) format.
- Reference clock detection: a more precise second source clock (50 or 60 Hz) can be used to enhance the calendar precision.
- Automatic correction for 28, 29 (leap year), 30, and 31 days of the month.
- Two programmable alarms with wakeup from Stop and Standby mode capability.
- On-the-fly correction from 1 to 32767 RTC clock pulses. This can be used to synchronize it with a master clock.
- Digital calibration circuit with 1 ppm resolution, to compensate for quartz crystal inaccuracy.
- Two anti-tamper detection pins with programmable filter. The MCU can be woken up from Stop and Standby modes on tamper event detection.
- Timestamp feature, which can be used to save the calendar content. This function can be triggered by an event on the timestamp pin, or by a tamper event. The MCU can be woken up from Stop and Standby modes on timestamp event detection.
- 17-bit Auto-reload counter for periodic interrupt with wakeup from STOP/STANDBY capability.

The RTC clock sources can be:

- A 32.768 kHz external crystal
- A resonator or oscillator
- The internal low-power RC oscillator (typical frequency of 40 kHz)
- The high-speed external clock divided by 32.

3.16 Communication interfaces

3.16.1 Inter-integrated circuit interface (I^2C)

The devices feature an I^2C bus interface that can operate in multimaster and slave mode. It can support standard (up to 100 kHz), fast (up to 400 kHz) and fast mode + (up to 1 MHz) modes.

It supports 7-bit and 10-bit addressing modes, multiple 7-bit slave addresses (2 addresses, 1 with configurable mask). It also includes programmable analog and digital noise filters.

Table 6. Comparison of I^2C analog and digital filters

-	Analog filter	Digital filter
Pulse width of suppressed spikes	≥ 50 ns	Programmable length from 1 to 15 I^2C peripheral clocks
Benefits	Available in Stop mode	1. Extra filtering capability vs. standard requirements. 2. Stable length
Drawbacks	Variations depending on temperature, voltage, process	Wakeup from Stop on address match is not available when digital filter is enabled.

In addition, it provides hardware support for SMBUS 2.0 and PMBUS 1.1: ARP capability, Host notify protocol, hardware CRC (PEC) generation/verification, timeouts verifications and ALERT protocol management. It also has a clock domain independent from the CPU clock, allowing the I2C1 to wake up the MCU from Stop mode on address match.

The I^2C interface can be served by the DMA controller.

The features available in I2C1 are showed below in *Table 7*.

Table 7. STM32F334x4/6/8 I2C implementation

I2C features[1]	I2C1
7-bit addressing mode	X
10-bit addressing mode	X
Standard mode (up to 100 kbit/s)	X
Fast mode (up to 400 kbit/s)	X
Fast Mode Plus with 20mA output drive I/Os (up to 1 Mbit/s)	X
Independent clock	X
SMBus	X
Wakeup from STOP	X

1. X = supported.

3.16.2 Universal synchronous / asynchronous receivers / transmitters (USARTs)

The STM32F334x4/6/8 devices have three embedded universal synchronous receivers/transmitters (USART1, USART2 and USART3).

The USART interfaces are able to communicate at speeds of up to 9 Mbits/s.

USART1 provides hardware management of the CTS and RTS signals. It supports IrDA SIR ENDEC, the multiprocessor communication mode, the single-wire half-duplex communication mode and has LIN Master/Slave capability.

All USART interfaces can be served by the DMA controller.

The features available in the USART interfaces are showed below in *Table 8*.

Table 8. USART features

USART modes/features(1)	USART1	USART2 USART3
Hardware flow control for modem	X	X
Continuous communication using DMA	X	X
Multiprocessor communication	X	X
Synchronous mode	X	X
Smartcard mode	X	-
Single-wire half-duplex communication	X	X
IrDA SIR ENDEC block	X	-
LIN mode	X	-
Dual clock domain and wake up from Stop mode	X	-
Receiver timeout interrupt	X	-
Modbus communication	X	-
Auto baud rate detection	X	-
Driver Enable	X	X

1. X = supported.

3.16.3 Serial peripheral interface (SPI)

A SPI interface allows to communicate up to 18 Mbits/s in slave and master modes in full-duplex and simplex communication modes. The 3-bit prescaler gives 8 master mode frequencies and the frame size is configurable from 4 bits to 16 bits.

The features available in SPI1 are showed below in *Table 9*.

Table 9. STM32F334x4/6/8 SPI implementation

SPI features(1)	SPI1
Hardware CRC calculation	X
Rx/Tx FIFO	X

Table 9. STM32F334x4/6/8 SPI implementation (continued)

SPI features[1]	SPI1
NSS pulse mode	X
TI mode	X

1. X = supported.

3.16.4 Controller area network (CAN)

The CAN is compliant with specifications 2.0A and B (active) with a bit rate up to 1 Mbit/s. It can receive and transmit standard frames with 11-bit identifiers as well as extended frames with 29-bit identifiers. It has three transmit mailboxes, two receive FIFOs with 3 stages and 14 scalable filter banks.

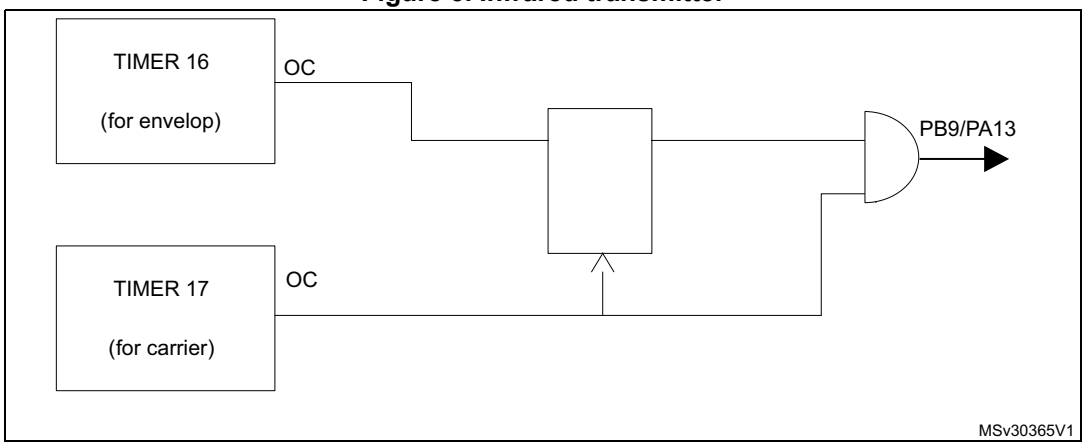
3.17 Infrared transmitter

The STM32F334x4/6/8 devices provide an infrared transmitter solution. The solution is based on internal connections between TIM16 and TIM17 as shown in the figure below.

TIM17 is used to provide the carrier frequency and TIM16 provides the main signal to be sent. The infrared output signal is available on PB9 or PA13.

To generate the infrared remote control signals, TIM16 channel 1 and TIM17 channel 1 must be properly configured to generate correct waveforms. All standard IR pulse modulation modes is obtained by programming the two timers of the output compare channels (see *Figure 3*).

Figure 3. Infrared transmitter



3.18 Touch sensing controller (TSC)

The STM32F334x4/6/8 devices provide a simple solution for adding capacitive sensing functionality to any application. These devices offer up to 18 capacitive sensing channels distributed over 6 analog I/Os group.

Capacitive sensing technology is able to detect the presence of a finger near an electrode that is protected from direct touch by a dielectric (glass, plastic and others). The capacitive

variation introduced by the finger (or any conductive object) is measured using a proven implementation based on a surface charge transfer acquisition principle. It consists of charging the electrode capacitance and then transferring a part of the accumulated charges into a sampling capacitor, until the voltage across this capacitor has reached a specific threshold. To limit the CPU bandwidth usage this acquisition is directly managed by the hardware touch sensing controller and only requires few external components to operate.

The touch sensing controller is fully supported by the STMTouch touch sensing firmware library, which is free to use and allows touch sensing functionality to be implemented reliably in the end application.

Table 10. Capacitive sensing GPIOs available on STM32F334x4/6/8 devices

Group	Capacitive sensing group name	Pin name
1	TSC_G1_IO1	PA0
	TSC_G1_IO2	PA1
	TSC_G1_IO3	PA2
	TSC_G1_IO4	PA3
2	TSC_G2_IO1	PA4
	TSC_G2_IO2	PA5
	TSC_G2_IO3	PA6
	TSC_G2_IO4	PA7
3	TSC_G3_IO1	PC5
	TSC_G3_IO2	PB0
	TSC_G3_IO3	PB1
	TSC_G3_IO4	PB2
4	TSC_G4_IO1	PA9
	TSC_G4_IO2	PA10
	TSC_G4_IO3	PA13
	TSC_G4_IO4	PA14
5	TSC_G5_IO1	PB3
	TSC_G5_IO2	PB4
	TSC_G5_IO3	PB6
	TSC_G5_IO4	PB7
6	TSC_G6_IO1	PB11
	TSC_G6_IO2	PB12
	TSC_G6_IO3	PB13
	TSC_G6_IO4	PB14

Table 11. No. of capacitive sensing channels available on STM32F334x4/6/8 devices

Analog I/O group	Number of capacitive sensing channels		
	STM32F334xRx	STM32F334xCx	STM32F334xKx
G1	3	3	3
G2	3	3	3
G3	3	2	2
G4	3	3	3
G5	3	3	3
G6	3	3	0
Total number of capacitive sensing channels	18	17	14

3.19 Development support

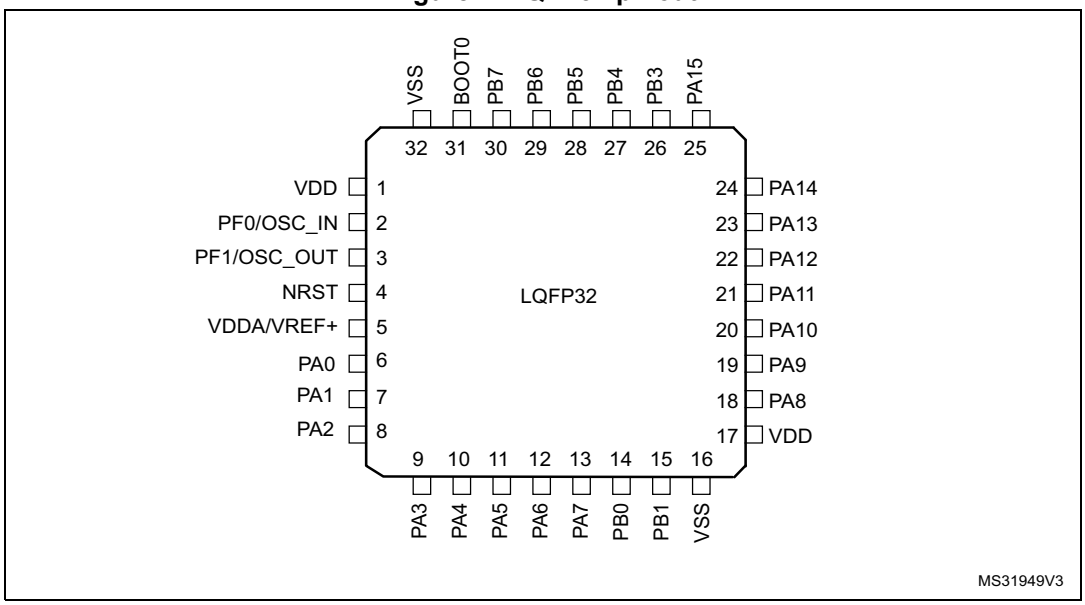
3.19.1 Serial-wire JTAG debug port (SWJ-DP)

The Arm SWJ-DP Interface is embedded, and is a combined JTAG and serial wire debug port that enables either a serial wire debug or a JTAG probe to be connected to the target.

The JTAG TMS and TCK pins are shared respectively with SWDIO and SWCLK and a specific sequence on the TMS pin is used to switch between JTAG-DP and SW-DP.

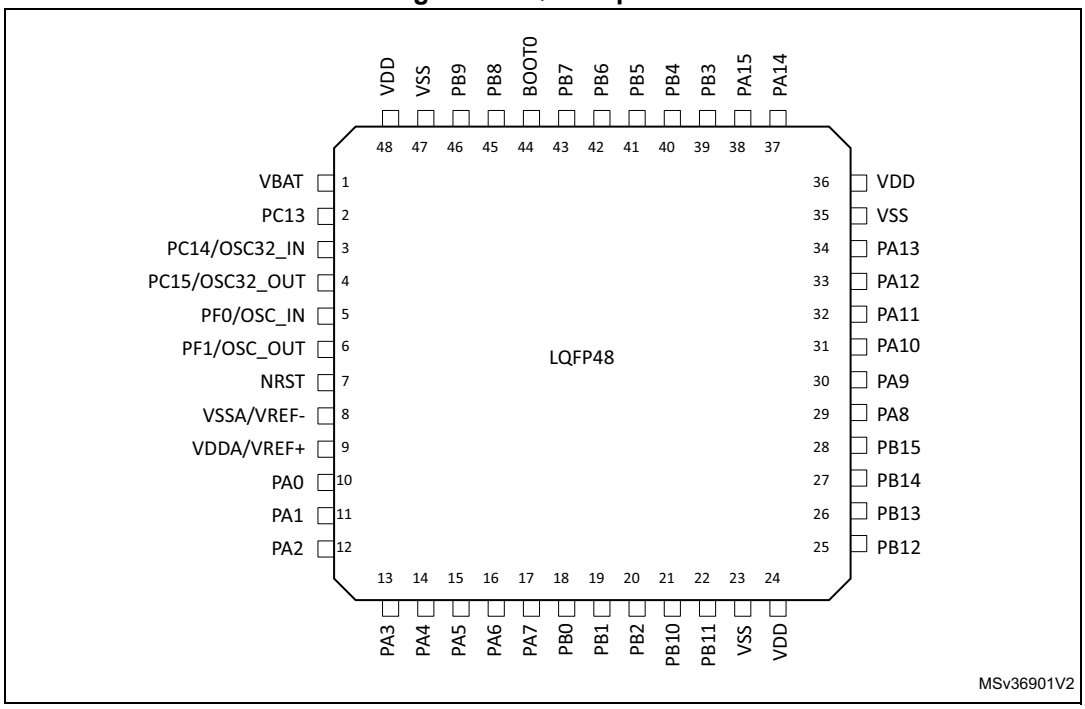
4 Pinout and pin descriptions

Figure 4. LQFP32 pinout



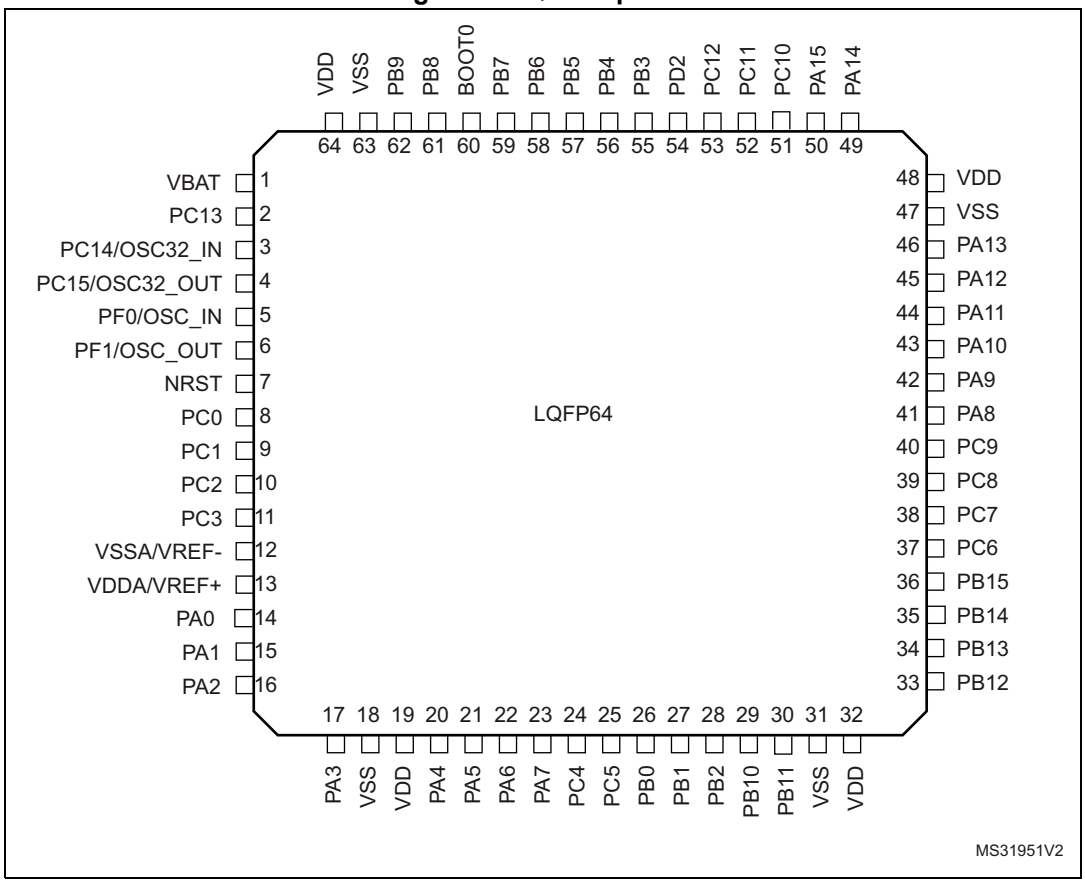
1. The above figure shows the package top view.

Figure 5. LQFP48 pinout



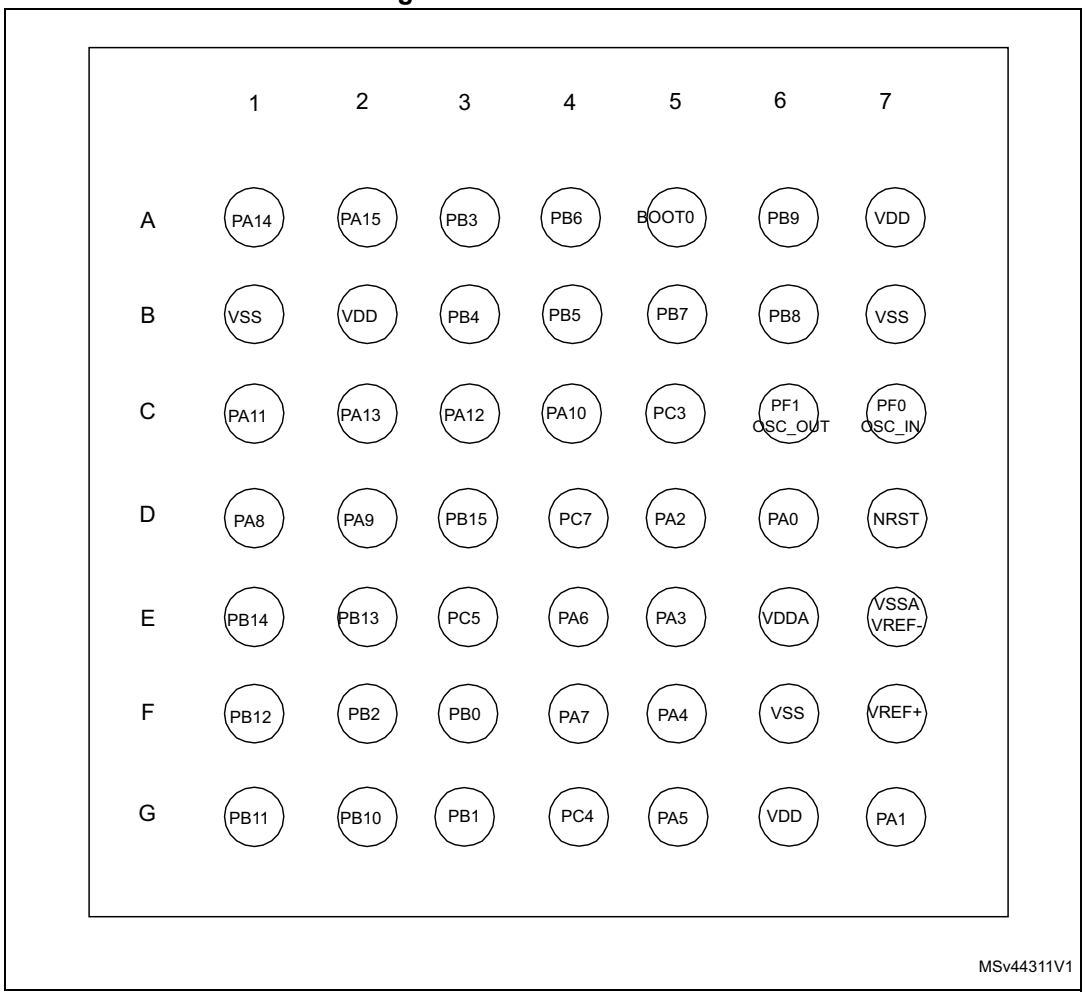
1. The above figure shows the package top view.

Figure 6. LQFP64 pinout



1. The above figure shows the package top view.

Figure 7. WLCSP49 ballout



1. The above figure shows the package top view.

Figure 8. UFQFPN32 pinout

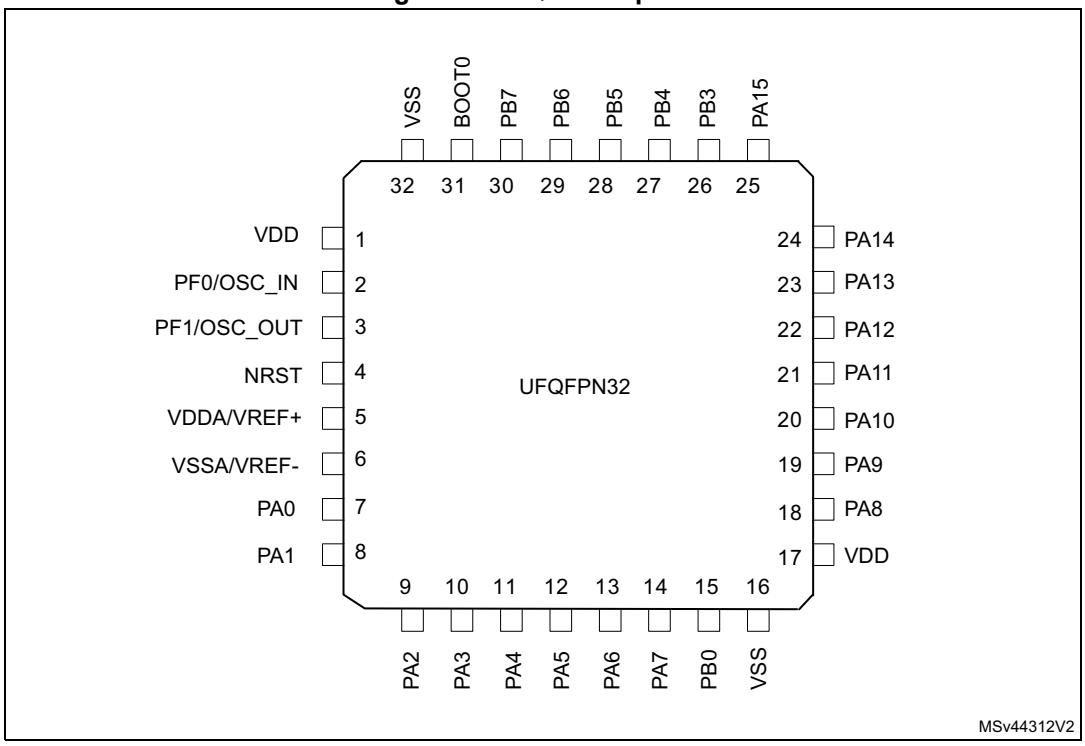


Table 12. Legend/abbreviations used in the pinout table

Name		Abbreviation	Definition
Pin name		Unless otherwise specified in brackets below the pin name, the pin function during and after reset is the same as the actual pin name	
Pin type		S	Supply pin
		I	Input only pin
		I/O	Input / output pin
I/O structure		FT	5 V tolerant I/O
		FTf	5 V tolerant I/O, FM+ capable
		TTa	3.3 V tolerant I/O directly connected to ADC
		TT	3.3 V tolerant I/O
		TC	Standard 3.3 V I/O
		B	Dedicated BOOT0 pin
		RST	Bi-directional reset pin with embedded weak pull-up resistor
Notes		Unless otherwise specified by a note, all I/Os are set as floating inputs during and after reset	
Pin functions	Alternate functions	Functions selected through GPIOx_AFR registers	
	Additional functions	Functions directly selected/enabled through peripheral registers	

Table 13. STM32F334x4/6/8 pin definitions

Pin Number					Pin name (function after reset)	Pin type	I/O structure	Pin functions	
UFQFPN32	LQFP32	LQFP48	LQFP64	WLCSP49				Alternate functions	Additional functions
-	-	1	1	-	VBAT	S	-	Backup power supply	
-	-	2	2	-	PC13(1)	I/O	TC	TIM1_CH1N	RTC_TAMP1/RTC_TS/ RTC_OUT/WKUP2
-	-	3	3	-	PC14 / OSC32_IN(1)	I/O	TC	-	OSC32_IN
-	-	4	4	-	PC15 / OSC32_OUT(1)	I/O	TC	-	OSC32_OUT
2	2	5	5	C7	PF0 / OSC_IN	I/O	FT	TIM1_CH3N	OSC_IN
3	3	6	6	C6	PF1 / OSC_OUT	I/O	FT	-	OSC_OUT
4	4	7	7	D7	NRST	I/O	RST	Device reset input / internal reset output (active low)	
-	-	-	8	-	PC0	I/O	TTa	EVENTOUT, TIM1_CH1	ADC12_IN6

Table 13. STM32F334x4/6/8 pin definitions (continued)

Pin Number					Pin name (function after reset)	Pin type	I/O structure	Pin functions	
UFQFPN32	LQFP32	LQFP48	LQFP64	WLCSP49				Alternate functions	Additional functions
-	-	-	9	-	PC1	I/O	TTa	EVENTOUT, TIM1_CH2	ADC12_IN7
-	-	-	10	-	PC2	I/O	TTa	EVENTOUT, TIM1_CH3	ADC12_IN8
-	-	-	11	C5	PC3	I/O	TTa	EVENTOUT, TIM1_CH4, TIM1_BKIN2	ADC12_IN9
6	-	8	12	E7	VSSA/VREF-	S	-	Analog ground/Negative reference voltage	
-	-	-		F7	VREF+	S	-	-	-
				E6	VDDA	S	-	-	-
5	5	9	13	-	VDDA/VREF+	S	-	Analog power supply/Positive reference voltage	
7	6	10	14	D6	PA0	I/O	TTa	TIM2_CH1/ TIM2_ETR, TSC_G1_IO1, USART2_CTS, EVENTOUT	ADC1_IN1(2), RTC_TAMP2/WKUP1
8	7	11	15	G7	PA1	I/O	TTa	TIM2_CH2, TSC_G1_IO2, USART2_RTS_DE, TIM15_CH1N, EVENTOUT	ADC1_IN2(2), RTC_REFIN
9	8	12	16	D5	PA2	I/O	TTa	TIM2_CH3, TSC_G1_IO3, USART2_TX, COMP2_OUT, TIM15_CH1, EVENTOUT	ADC1_IN3(2), COMP2_INM
10	9	13	17	E5	PA3	I/O	TTa	TIM2_CH4, TSC_G1_IO4, USART2_RX, TIM15_CH2, EVENTOUT	ADC1_IN4(2)
-	-	-	18	F6	VSS	S	-	-	-
-	-	-	19	G6	VDD	S	-	-	-
11	10	14	20	F5	PA4(3)	I/O	TTa	TIM3_CH2, TSC_G2_IO1, SPI1_NSS, USART2_CK, EVENTOUT	ADC2_IN1(2), DAC1_OUT1, COMP2_INM, COMP4_INM, COMP6_INM
12	11	15	21	G5	PA5(3)	I/O	TTa	TIM2_CH1/ TIM2_ETR, TSC_G2_IO2, SPI1_SCK, EVENTOUT	ADC2_IN2(2), DAC1_OUT2, OPAMP2_VINM

Table 13. STM32F334x4/6/8 pin definitions (continued)

Pin Number					Pin name (function after reset)	Pin type	I/O structure	Pin functions	
UFQFPN32	LQFP32	LQFP48	LQFP64	WLCSP49				Alternate functions	Additional functions
13	12	16	22	E4	PA6(3)	I/O	TTa	TIM16_CH1, TIM3_CH1, TSC_G2_IO3, SPI1_MISO, TIM1_BKIN, OPAMP2_DIG, EVENTOUT	ADC2_IN3(2), DAC2_OUT1, OPAMP2_VOUT
14	13	17	23	F4	PA7	I/O	TTa	TIM17_CH1, TIM3_CH2, TSC_G2_IO4, SPI1_MOSI, TIM1_CH1N, EVENTOUT	ADC2_IN4(2), COMP2_INP, OPAMP2_VINP
-	-	-	24	G4	PC4	I/O	TTa	EVENTOUT, TIM1_ETR, USART1_TX	ADC2_IN5(2)
-	-	-	25	E3	PC5	I/O	TTa	EVENTOUT, TIM15_BKIN, TSC_G3_IO1, USART1_RX	ADC2_IN11, OPAMP2_VINM
15	14	18	26	F3	PB0	I/O	TTa	TIM3_CH3, TSC_G3_IO2, TIM1_CH2N, EVENTOUT	ADC1_IN11, COMP4_INP, OPAMP2_VINP
-	15	19	27	G3	PB1	I/O	TTa	TIM3_CH4, TSC_G3_IO3, TIM1_CH3N, COMP4_OUT, HRTIM1_SCOUT, EVENTOUT	ADC1_IN12
-	-	20	28	F2	PB2	I/O	TTa	TSC_G3_IO4, HRTIM_SCIN, EVENTOUT	ADC2_IN12, COMP4_INM
-	-	21	29	G2	PB10	I/O	TT	TIM2_CH3, TSC_SYNC, USART3_TX, HRTIM1_FLT3, EVENTOUT	-
-	-	22	30	G1	PB11	I/O	TTa	TIM2_CH4, TSC_G6_IO1, USART3_RX, HRTIM1_FLT4, EVENTOUT	COMP6_INP
16	16	23	31	-	VSS	S	-	Digital ground	
17	17	24	32	B2	VDD	S	-	Digital power supply	
	-	25	33	F1	PB12	I/O	TTa	TSC_G6_IO2, TIM1_BKIN, USART3_CK, HRTIM1_CHC1, EVENTOUT	ADC2_IN13
-	-	26	34	E2	PB13	I/O	TTa	TSC_G6_IO3, TIM1_CH1N, USART3_CTS, HRTIM1_CHC2, EVENTOUT	ADC1_IN13

Table 13. STM32F334x4/6/8 pin definitions (continued)

Pin Number					Pin name (function after reset)	Pin type	I/O structure	Pin functions	
UFQFPN32	LQFP32	LQFP48	LQFP64	WLCSP49				Alternate functions	Additional functions
-	-	27	35	E1	PB14	I/O	TTa	TIM15_CH1, TSC_G6_IO4, TIM1_CH2N, USART3_RTS_DE, HRTIM1_CHD1, EVENTOUT	ADC2_IN14, OPAMP2_VINP
-	-	28	36	D3	PB15	I/O	TTa	TIM15_CH2, TIM15_CH1N, TIM1_CH3N, HRTIM1_CHD2, EVENTOUT	ADC2_IN15, COMP6_INM, RTC_REFIN
-	-	-	37	-	PC6	I/O	FT	EVENTOUT, TIM3_CH1, HRTIM1_EEV10, COMP6_OUT	-
-	-	-	38	D4	PC7	I/O	FT	EVENTOUT, TIM3_CH2, HRTIM1_FLT5	-
-	-	-	39	-	PC8	I/O	FT	EVENTOUT, TIM3_CH3, HRTIM1_CHE1	-
-	-	-	40	-	PC9	I/O	FT	EVENTOUT, TIM3_CH4, HRTIM1_CHE2	-
18	18	29	41	D1	PA8	I/O	FT	MCO, TIM1_CH1, USART1_CK, HRTIM1_CHA1, EVENTOUT	-
19	19	30	42	D2	PA9	I/O	FT	TSC_G4_IO1, TIM1_CH2, USART1_TX, TIM15_BKIN, TIM2_CH3, HRTIM1_CHA2, EVENTOUT	-
20	20	31	43	C4	PA10	I/O	FT	TIM17_BKIN, TSC_G4_IO2, TIM1_CH3, USART1_RX, COMP6_OUT, TIM2_CH4, HRTIM1_CHB1, EVENTOUT	-
21	21	32	44	C1	PA11	I/O	FT	TIM1_CH1N, USART1_CTS, CAN_RX, TIM1_CH4, TIM1_BKIN2, HRTIM1_CHB2, EVENTOUT	-
22	22	33	45	C3	PA12	I/O	FT	TIM16_CH1, TIM1_CH2N, USART1_RTS_DE, COMP2_OUT, CAN_TX, TIM1_ETR, HRTIM1_FLT1, EVENTOUT	-

Table 13. STM32F334x4/6/8 pin definitions (continued)

Pin Number					Pin name (function after reset)	Pin type	I/O structure	Pin functions	
UFQFPN32	LQFP32	LQFP48	LQFP64	WLCSP49				Alternate functions	Additional functions
23	23	34	46	C2	PA13	I/O	FT	JTMS/SWDAT, TIM16_CH1N, TSC_G4_IO3, IR_OUT, USART3_CTS, EVENTOUT	-
-	-	35	47	B1	VSS	S	-	-	-
-	-	36	48	-	VDD	S	-	-	-
24	24	37	49	A1	PA14	I/O	FTf	JTCK/SWCLK, TSC_G4_IO4, I2C1_SDA, TIM1_BKIN, USART2_TX, EVENTOUT	-
25	25	38	50	A2	PA15	I/O	FTf	JTDI, TIM2_CH1/TIM2_ETR, TSC_SYNC, I2C1_SCL, SPI1_NSS, USART2_RX, TIM1_BKIN, HRTIM1_FLT2, EVENTOUT	-
-	-	-	51	-	PC10	I/O	FT	EVENTOUT, USART3_TX	-
-	-	-	52	-	PC11	I/O	FT	EVENTOUT, HRTIM1_EEV2, USART3_RX	-
-	-	-	53	-	PC12	I/O	FT	EVENTOUT, HRTIM1_EEV1, USART3_CK	-
-	-	-	54	-	PD2	I/O	FT	EVENTOUT, TIM3_ETR	-
26	26	39	55	A3	PB3	I/O	FT	JTDO/TRACE SWO, TIM2_CH2, TSC_G5_IO1, SPI1_SCK, USART2_TX, TIM3_ETR, HRTIM1_SCOUT, HRTIM1_EEV9, EVENTOUT	-
27	27	40	56	B3	PB4	I/O	FT	NJTRST, TIM16_CH1, TIM3_CH1, TSC_G5_IO2, SPI1_MISO, USART2_RX, TIM17_BKIN, HRTIM1_EEV7, EVENTOUT	-

Table 13. STM32F334x4/6/8 pin definitions (continued)

Pin Number					Pin name (function after reset)	Pin type	I/O structure	Pin functions	
UFQFPN32	LQFP32	LQFP48	LQFP64	WLCSP49				Alternate functions	Additional functions
28	28	41	57	B4	PB5	I/O	FT	TIM16_BKIN, TIM3_CH2, I2C1_SMBA, SPI1_MOSI, USART2_CK, TIM17_CH1, HRTIM1_EEV6, EVENTOUT	-
29	29	42	58	A4	PB6	I/O	FTf	TIM16_CH1N, TSC_G5_IO3, I2C1_SCL, USART1_TX, HRTIM1_SCIN, HRTIM1_EEV4, EVENTOUT	-
30	30	43	59	B5	PB7	I/O	FTf	TIM17_CH1N, TSC_G5_IO4, I2C1_SDA, USART1_RX, TIM3_CH4, HRTIM1_EEV3, EVENTOUT	-
31	31	44	60	A5	BOOT0	I	B	-	-
-	-	45	61	B6	PB8	I/O	FTf	TIM16_CH1, TSC_SYNC, I2C1_SCL, USART3_RX, CAN_RX, TIM1_BKIN, HRTIM1_EEV8, EVENTOUT	-
-	-	46	62	A6	PB9	I/O	FTf	TIM17_CH1, I2C1_SDA, IR_OUT, USART3_TX, COMP2_OUT, CAN_TX, HRTIM1_EEV5, EVENTOUT	-
32	32	47	63	B7	VSS	S	-	-	-
1	1	48	64	A7	VDD	S	-	-	-

1. PC13, PC14 and PC15 are supplied through the power switch. Since the switch sinks only a limited amount of current (3 mA), the use of GPIO PC13 to PC15 in output mode is limited:
   - The speed should not exceed 2 MHz with a maximum load of 30 pF
   - These GPIOs must not be used as current sources (e.g. to drive an LED).
   After the first backup domain power-up, PC13, PC14 and PC15 operate as GPIOs. Their function then depends on the content of the Backup registers which is not reset by the main reset. For details on how to manage these GPIOs, refer to the Battery backup domain and BKP register description sections in the reference manual.
2. Fast ADC channel.
3. These GPIOs offer a reduced touch sensing sensitivity. It is thus recommended to use them as sampling capacitor I/O.

Table 14. Alternate functions

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS_AF	TIM2/TIM15/ TIM16/TIM17/ EVENT	TIM1/TIM3/ TIM15/ TIM16	HRTIM1/TSC	I2C1/TIM1	SPI1/ Infrared	TIM1/ Infrared	USART1/USA RT2/USART3/ GPCOMP6	GPCOMP2/ GPCOMP4/ GPCOMP6	CAN/TIM1/ TIM15	TIM2/TIM3/TI M17	TIM1	HRTIM1/ TIM1	HRTIM1/ OPAMP2	-	EVENT
Port A	PA0	-	TIM2_CH1/TI M2_ETR	-	TSC_G1_IO1	-	-	-	USART2_CTS	-	-	-	-	-	-	-	EVENTOUT
	PA1	-	TIM2_CH2	-	TSC_G1_IO2	-	-	-	USART2_RTS _DE	-	TIM15_CH1N	-	-	-	-	-	EVENTOUT
	PA2	-	TIM2_CH3	-	TSC_G1_IO3	-	-	-	USART2_TX	COMP2_OUT	TIM15_CH1	-	-	-	-	-	EVENTOUT
	PA3	-	TIM2_CH4	-	TSC_G1_IO4	-	-	-	USART2_RX	-	TIM15_CH2	-	-	-	-	-	EVENTOUT
	PA4	-	-	TIM3_CH2	TSC_G2_IO1	-	SPI1_NSS	-	USART2_CK	-	-	-	-	-	-	-	EVENTOUT
	PA5	-	TIM2_CH1/TI M2_ETR	-	TSC_G2_IO2	-	SPI1_SCK	-	-	-	-	-	-	-	-	-	EVENTOUT
	PA6	-	TIM16_CH1	TIM3_CH1	TSC_G2_IO3	-	SPI1_MISO	TIM1_BKIN	-	-	-	-	-	-	OPAMP2_DIG	-	EVENTOUT
	PA7	-	TIM17_CH1	TIM3_CH2	TSC_G2_IO4	-	SPI1_MOSI	TIM1_CH1N	-	-	-	-	-	-	-	-	EVENTOUT
	PA8	MCO	-	-	-	-	-	TIM1_CH1	USART1_CK	-	-	-	-	-	HRTIM1_CHA1	-	EVENTOUT
	PA9	-	-	-	TSC_G4_IO1	-	-	TIM1_CH2	USART1_TX	-	TIM15_BKIN	TIM2_CH3	-	-	HRTIM1_CHA2	-	EVENTOUT
	PA10	-	TIM17_BKIN	-	TSC_G4_IO2	-	-	TIM1_CH3	USART1_RX	COMP6_OUT	-	TIM2_CH4	-	-	HRTIM1_CHB1	-	EVENTOUT
	PA11	-	-	-	-	-	-	TIM1_CH1N	USART1_CTS	-	CAN_RX	-	TIM1_CH4	TIM1_BKIN2	HRTIM1_CHB2	-	EVENTOUT
	PA12	-	TIM16_CH1	-	-	-	-	TIM1_CH2N	USART1_RTS _DE	COMP2_OUT	CAN_TX	-	TIM1_ETR	-	HRTIM1_FLT1	-	EVENTOUT
	PA13	JTMS/SWDAT	TIM16_CH1N	-	TSC_G4_IO3	-	IR_OUT	-	USART3_CTS	-	-	-	-	-	-	-	EVENTOUT
	PA14	JTCK/SWCLK	-	-	TSC_G4_IO4	I2C1_SDA	-	TIM1_BKIN	USART2_TX	-	-	-	-	-	-	-	EVENTOUT
	PA15	JTDI	TIM2_CH1/ TIM2_ETR	-	TSC_SYNC	I2C1_SCL	SPI1_NSS	-	USART2_RX	-	TIM1_BKIN	-	-	-	HRTIM1_FLT2	-	EVENTOUT
Port B	PB0	-	-	TIM3_CH3	TSC_G3_IO2	-	-	TIM1_CH2N	-	-	-	-	-	-	-	-	EVENTOUT
	PB1	-	-	TIM3_CH4	TSC_G3_IO3	-	-	TIM1_CH3N	-	COMP4_OUT	-	-	-	-	HRTIM1_SCOUT	-	EVENTOUT
	PB2	-	-	-	TSC_G3_IO4	-	-	-	-	-	-	-	-	-	HRTIM1_SCIN	-	EVENTOUT
	PB3	JTDO/TRACE SWO	TIM2_CH2	-	TSC_G5_IO1	-	SPI1_SCK	-	USART2_TX	-	-	TIM3_ETR	-	HRTIM1_ SCOUT	HRTIM1_EEV9	-	EVENTOUT
	PB4	NJTRST	TIM16_CH1	TIM3_CH1	TSC_G5_IO2	-	SPI1_MISO	-	USART2_RX	-	-	TIM17_BKIN	-	-	HRTIM1_EEV7	-	EVENTOUT
	PB5	-	TIM16_BKIN	TIM3_CH2	-	I2C1_SMBA	SPI1_MOSI	-	USART2_CK	-	-	TIM17_CH1	-	-	HRTIM1_EEV6	-	EVENTOUT
	PB6	-	TIM16_CH1N	-	TSC_G5_IO3	I2C1_SCL	-	-	USART1_TX	-	-	-	-	HRTIM1_ SCIN	HRTIM1_EEV4	-	EVENTOUT
	PB7	-	TIM17_CH1N	-	TSC_G5_IO4	I2C1_SDA	-	-	USART1_RX	-	-	TIM3_CH4	-	-	HRTIM1_EEV3	-	EVENTOUT
	PB8	-	TIM16_CH1	-	TSC_SYNC	I2C1_SCL	-	-	USART3_RX	-	CAN_RX	-	-	TIM1_BKIN	HRTIM1_EEV8	-	EVENTOUT
	PB9	-	TIM17_CH1	-	-	I2C1_SDA	-	IR_OUT	USART3_TX	COMP2_OUT	CAN_TX	-	-	-	HRTIM1_EEV5	-	EVENTOUT

Table 14. Alternate functions (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS_AF	TIM2/TIM15/ TIM16/TIM17/ EVENT	TIM1/TIM3/ TIM15/ TIM16	HRTIM1/TSC	I2C1/TIM1	SPI1/ Infrared	TIM1/ Infrared	USART1/USA RT2/USART3/ GPCOMP6	GPCOMP2/ GPCOMP4/ GPCOMP6	CAN/TIM1/ TIM15	TIM2/TIM3/TI M17	TIM1	HRTIM1/ TIM1	HRTIM1/ OPAMP2	-	EVENT
Port B	PB10	-	TIM2_CH3	-	TSC_SYNC	-	-	-	USART3_TX	-	-	-	-	-	HRTIM1_FLT3	-	EVENTOUT
	PB11	-	TIM2_CH4	-	TSC_G6_IO1	-	-	-	USART3_RX	-	-	-	-	-	HRTIM1_FLT4	-	EVENTOUT
	PB12	-	-	-	TSC_G6_IO2	-	-	TIM1_BKIN	USART3_CK	-	-	-	-	-	HRTIM1_CHC1	-	EVENTOUT
	PB13	-	-	-	TSC_G6_IO3	-	-	TIM1_CH1N	USART3_CTS	-	-	-	-	-	HRTIM1_CHC2	-	EVENTOUT
	PB14	-	TIM15_CH1	-	TSC_G6_IO4	-	-	TIM1_CH2N	USART3_RTS _DE	-	-	-	-	-	HRTIM1_CHD1	-	EVENTOUT
	PB15	-	TIM15_CH2	TIM15_CH1N	-	TIM1_CH3N	-	-	-	-	-	-	-	-	HRTIM1_CHD2	-	EVENTOUT
Port C	PC0	-	EVENTOUT	TIM1_CH1	-	-	-	-	-	-	-	-	-	-	-	-	-
	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
	PC2	-	EVENTOUT	TIM1_CH3	-	-	-	-	-	-	-	-	-	-	-	-	-
	PC3	-	EVENTOUT	TIM1_CH4	-	-	-	TIM1_BKIN2	-	-	-	-	-	-	-	-	-
	PC4	-	EVENTOUT	TIM1_ETR	-	-	-	-	USART1_TX	-	-	-	-	-	-	-	-
	PC5	-	EVENTOUT	TIM15_BKIN	TSC_G3_IO1	-	-	-	USART1_RX	-	-	-	-	-	-	-	-
	PC6	-	EVENTOUT	TIM3_CH1	HRTIM1_ EEV10	-	-	-	COMP6_OUT	-	-	-	-	-	-	-	-
	PC7	-	EVENTOUT	TIM3_CH2	HRTIM1_FLT5	-	-	-	-	-	-	-	-	-	-	-	-
	PC8	-	EVENTOUT	TIM3_CH3	HRTIM1_CHE1	-	-	-	-	-	-	-	-	-	-	-	-
	PC9	-	EVENTOUT	TIM3_CH4	HRTIM1_CHE2	-	-	-	-	-	-	-	-	-	-	-	-
	PC10	-	EVENTOUT	-	-	-	-	-	USART3_TX	-	-	-	-	-	-	-	-
	PC11	-	EVENTOUT	-	HRTIM1_EEV2	-	-	-	USART3_RX	-	-	-	-	-	-	-	-
	PC12	-	EVENTOUT	-	HRTIM1_EEV1	-	-	-	USART3_CK	-	-	-	-	-	-	-	-
	PC13	-	-	-	-	TIM1_CH1N	-	-	-	-	-	-	-	-	-	-	-
	PC14	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
	PC15	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
Port D	PD2	-	EVENTOUT	TIM3_ETR	-	-	-	-	-	-	-	-	-	-	-	-	-
Port F	PF0	-	-	-	-	-	-	TIM1_CH3N	-	-	-	-	-	-	-	-	-
	PF1	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-

5 Memory mapping

Figure 9. STM32F334x4/6/8 memory map

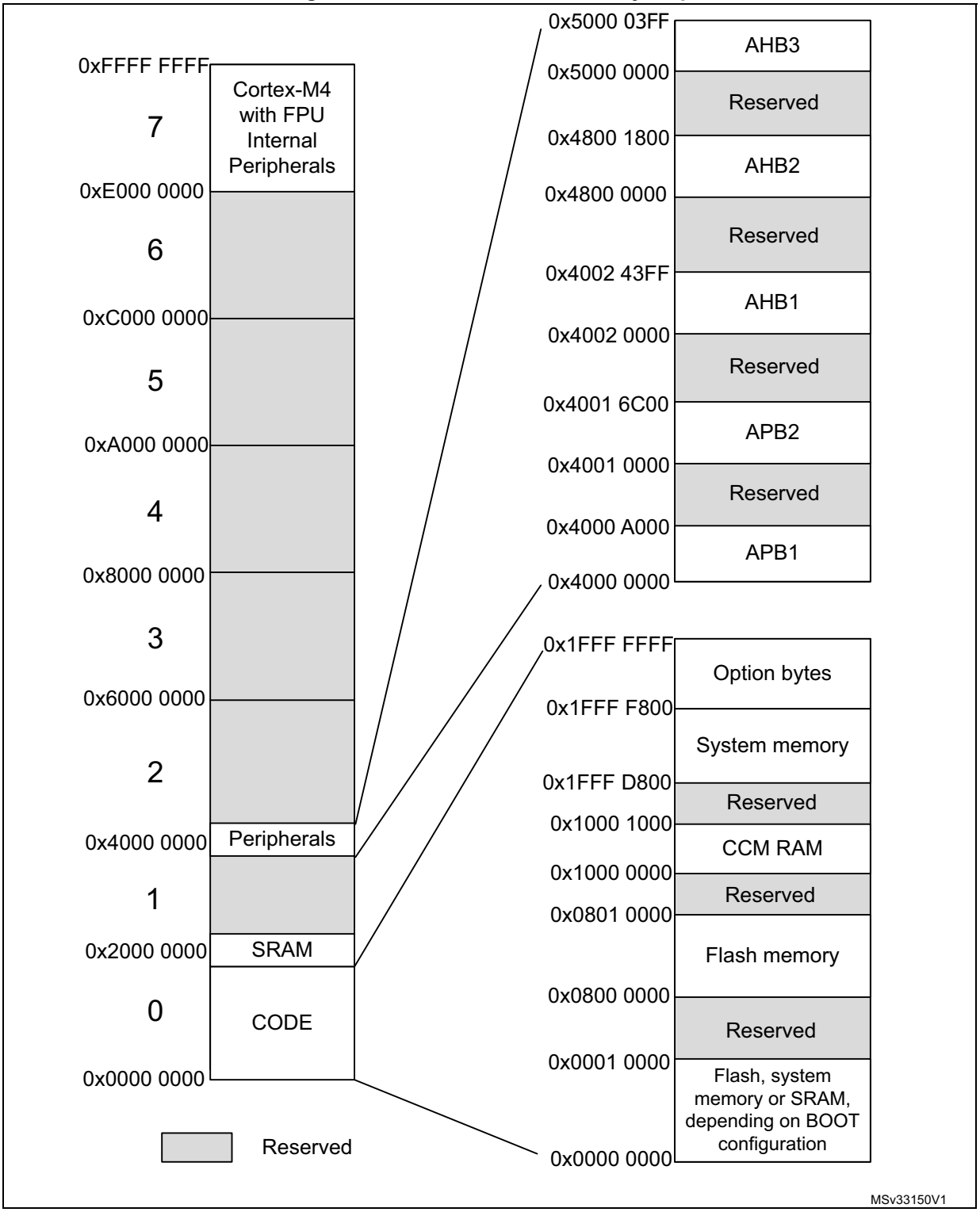


Table 15. STM32F334x4/6/8 peripheral register boundary addresses

Bus	Boundary address	Size (bytes)	Peripheral
AHB3	0x5000 0000 - 0x5000 03FF	1 K	ADC1 - ADC2
-	0x4800 1800 - 0x4FFF FFFF	~132 M	Reserved
AHB2	0x4800 1400 - 0x4800 17FF	1 K	GPIOF
-	0x4800 1000 - 0x4800 13FF	1 K	Reserved
AHB2	0x4800 0C00 - 0x4800 0FFF	1 K	GPIOD
	0x4800 0800 - 0x4800 0BFF	1 K	GPIOC
	0x4800 0400 - 0x4800 07FF	1 K	GPIOB
	0x4800 0000 - 0x4800 03FF	1 K	GPIOA
-	0x4002 4400 - 0x47FF FFFF	~128 M	Reserved
AHB1	0x4002 4000 - 0x4002 43FF	1 K	TSC
	0x4002 3400 - 0x4002 3FFF	3 K	Reserved
	0x4002 3000 - 0x4002 33FF	1 K	CRC
	0x4002 2400 - 0x4002 2FFF	3 K	Reserved
	0x4002 2000 - 0x4002 23FF	1 K	Flash interface
	0x4002 1400 - 0x4002 1FFF	3 K	Reserved
	0x4002 1000 - 0x4002 13FF	1 K	RCC
	0x4002 0400 - 0x4002 0FFF	3 K	Reserved
	0x4002 0000 - 0x4002 03FF	1 K	DMA1
-	0x4001 8000 - 0x4001 FFFF	32 K	Reserved
APB2	0x4001 7400 - 0x4001 77FF	1 K	HRTIM1
APB2	0x4001 4C00 - 0x4001 73FF	12 K	Reserved
	0x4001 4800 - 0x4001 4BFF	1 K	TIM17
	0x4001 4400 - 0x4001 47FF	1 K	TIM16
	0x4001 4000 - 0x4001 43FF	1 K	TIM15
	0x4001 3C00 - 0x4001 3FFF	1 K	Reserved
	0x4001 3800 - 0x4001 3BFF	1 K	USART1
	0x4001 3400 - 0x4001 37FF	1 K	Reserved
	0x4001 3000 - 0x4001 33FF	1 K	SPI1
	0x4001 2C00 - 0x4001 2FFF	1 K	TIM1
	0x4001 0800 - 0x4001 2BFF	9 K	Reserved
	0x4001 0400 - 0x4001 07FF	1 K	EXTI
	0x4001 0000 - 0x4001 03FF	1 K	SYSCFG + COMP + OPAMP
-	0x4000 9C00 - 0x4000 FFFF	25 K	Reserved

Table 15. STM32F334x4/6/8 peripheral register boundary addresses (continued)

Bus	Boundary address	Size (bytes)	Peripheral
APB1	0x4000 9800 - 0x4000 9BFF	1 K	DAC2
	0x4000 7800 - 0x4000 97FF	8 K	Reserved
	0x4000 7400 - 0x4000 77FF	1 K	DAC1
	0x4000 7000 - 0x4000 73FF	1 K	PWR
	0x4000 6800 - 0x4000 6FFF	2 K	Reserved
	0x4000 6400 - 0x4000 67FF	1 K	bxCAN
	0x4000 5800 - 0x4000 63FF	3 K	Reserved
	0x4000 5400 - 0x4000 57FF	1 K	I2C1
	0x4000 4C00 - 0x4000 53FF	2 K	Reserved
	0x4000 4800 - 0x4000 4BFF	1 K	USART3
	0x4000 4400 - 0x4000 47FF	1 K	USART2
	0x4000 3400 - 0x4000 43FF	2 K	Reserved
	0x4000 3000 - 0x4000 33FF	1 K	IWDG
	0x4000 2C00 - 0x4000 2FFF	1 K	WWDG
	0x4000 2800 - 0x4000 2BFF	1 K	RTC
	0x4000 1800 - 0x4000 27FF	4 K	Reserved
	0x4000 1400 - 0x4000 17FF	1 K	TIM7
	0x4000 1000 - 0x4000 13FF	1 K	TIM6
	0x4000 0800 - 0x4000 0FFF	2 K	Reserved
	0x4000 0400 - 0x4000 07FF	1 K	TIM3
	0x4000 0000 - 0x4000 03FF	1 K	TIM2
-	0x2000 3000 - 3FFF FFFF	~512 M	Reserved
-	0x2000 0000 - 0x2000 2FFF	12 K	SRAM
-	0x1FFF F800 - 0x1FFF FFFF	2 K	Option bytes
-	0x1FFF D800 - 0x1FFF F7FF	8 K	System memory
-	0x1000 2000 - 0x1FFF D7FF	~256 M	Reserved
-	0x1000 0000 - 0x1000 0FFF	4 K	CCM RAM
-	0x0804 0000 - 0x0FFF FFFF	~128 M	Reserved
-	0x0800 0000 - 0x0800 FFFF	64 K	Main Flash memory
-	0x0004 0000 - 0x07FF FFFF	~128 M	Reserved
-	0x0000 000 - 0x0000 FFFF	64 K	Main Flash memory, system memory or SRAM depending on BOOT configuration

6 Electrical characteristics

6.1 Parameter conditions

Unless otherwise specified, all voltages are referenced to V_{SS}.

6.1.1 Minimum and maximum values

Unless otherwise specified, the minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage and frequencies by tests in production on 100% of the devices with an ambient temperature at T_A = 25 °C and T_A = $T_A$max (given by the selected temperature range).

Data based on characterization results, design simulation and/or technology characteristics are indicated in the table footnotes and are not tested in production. Based on characterization, the minimum and maximum values refer to sample tests and represent the mean value plus or minus three times the standard deviation (mean ±3 σ).

6.1.2 Typical values

Unless otherwise specified, typical data are based on T_A = 25 °C, V_{DD} = 3.3 V, V_{DDA} = 3.3 V. They are given only as design guidelines and are not tested.

Typical ADC accuracy values are determined by characterization of a batch of samples from a standard diffusion lot over the full temperature range, where 95% of the devices have an error less than or equal to the value indicated (mean±2σ).

6.1.3 Typical curves

Unless otherwise specified, all typical curves are given only as design guidelines and are not tested.

6.1.4 Loading capacitor

The loading conditions used for pin parameter measurement are shown in *Figure 10*.

6.1.5 Input voltage on a pin

The input voltage measurement on a pin of the device is described in *Figure 11*.

Figure 10. Pin loading conditions

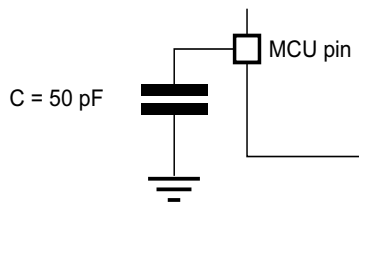
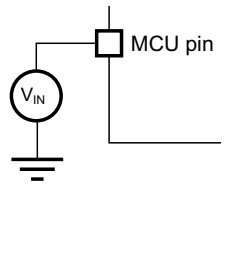
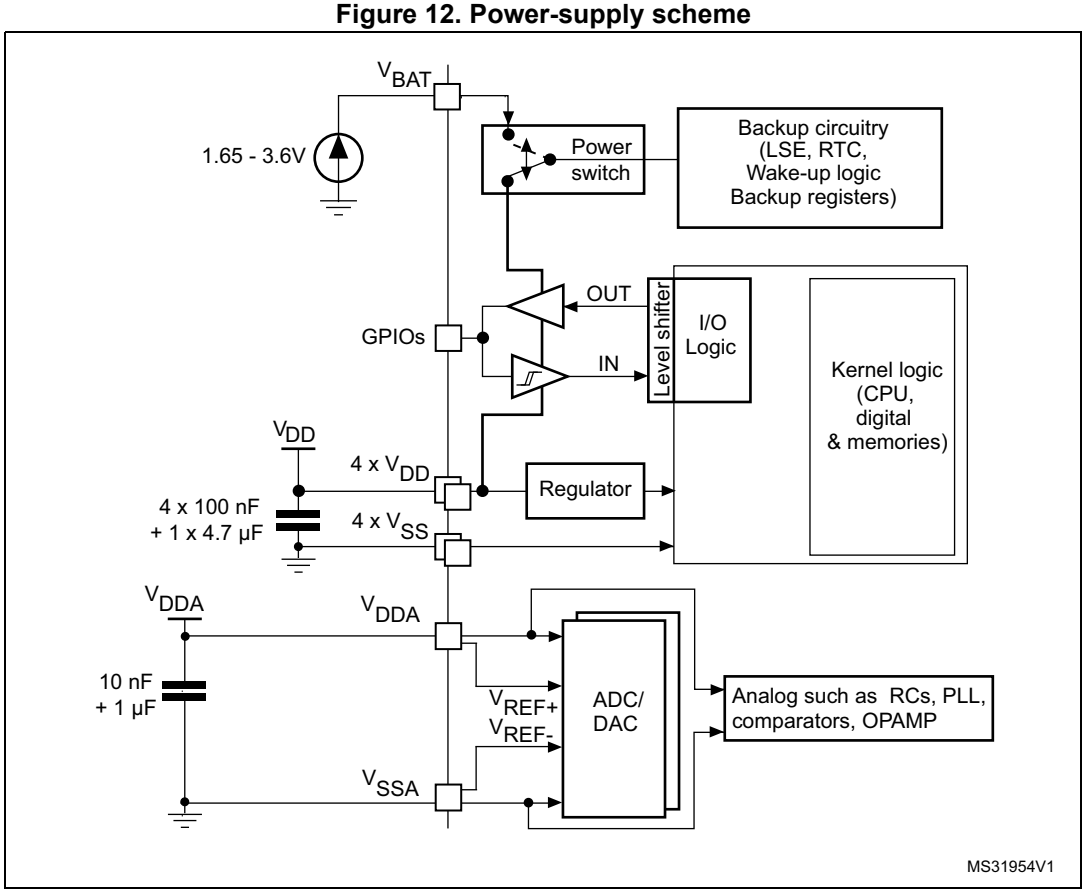


Figure 11. Pin input voltage



6.1.6 Power-supply scheme

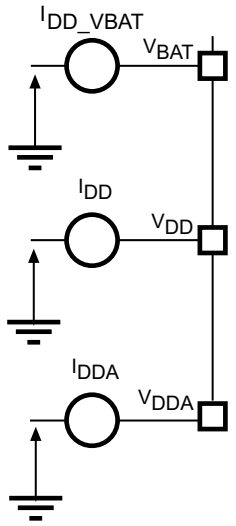
Figure 12. Power-supply scheme



Caution: Each power-supply pair (V_{DD}/V_{SS}, V_{DDA}/V_{SSA} etc..) must be decoupled with filtering ceramic capacitors as shown above. These capacitors must be placed as close as possible to or below the appropriate pins on the underside of the PCB, to ensure the good functionality of the device.

6.1.7 Measurement of the current consumption

Figure 13. Scheme of the current-consumption measurement



6.2 Absolute maximum ratings

Stresses above the absolute maximum ratings listed in *Table 16: Voltage characteristics*, *Table 17: Current characteristics*, and *Table 18: Thermal characteristics* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect the device reliability.

Table 16. Voltage characteristics(1)

Symbol	Ratings	Min.	Max.	Unit
$V_{DD}–V_{SS}$	External main supply voltage (including V_{DDA}, V_{BAT} and V_{DD})	-0.3	4.0	V
$V_{DD}–V_{DDA}$	Allowed voltage difference for $V_{DD} > V_{DDA}$	-	0.4	
V_{IN}(2)	Input voltage on FT and FTf pins	V_{SS} –0.3	V_{DD} + 4.0	
	Input voltage on TTa and TT pins	V_{SS} –0.3	4.0	
	Input voltage on any other pin	V_{SS} –0.3	4.0	
	Input voltage on Boot0 pin	0	9	
$\|\Delta V_{DDx}\|$	Variations between different V_{DD} power pins	-	50	mV
$\|V_{SSX} – V_{SS}\|$	Variations between all the different ground pins(3)	-	50	
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	see *Section 6.3.12: Electrical sensitivity characteristics*		-

1. All main power (V_{DD}, V_{DDA}) and ground (V_{SS}, V_{SSA}) pins must always be connected to the external power supply, in the permitted range. The following relationship must be respected between V_{DDA} and V_{DD}:
V_{DDA} must power on before or at the same time as V_{DD} in the power up sequence.
V_{DDA} must be greater than or equal to V_{DD}.
2. V_{IN} maximum must always be respected. Refer to *Table 17: Current characteristics* for the maximum allowed injected current values.
3. Include V_{REF-} pin.

Table 17. Current characteristics

Symbol	Ratings	Max.	Unit
ΣI_{VDD}	Total current into sum of all VDD power lines (source)(1)	140	mA
ΣI_{VSS}	Total current out of sum of all VSS ground lines (sink)(1)	-140	
I_{VDD}	Maximum current into each VDD power line (source)(1)	100	
I_{VSS}	Maximum current out of each V_{SS_x} ground line (sink)(1)	100	
$I_{IO(PIN)}$	Output current sunk by any I/O and control pin	25	
	Output current source by any I/O and control pin	-25	
$\Sigma I_{IO(PIN)}$	Total output current sunk by sum of all I/Os and control pins(2)	80	
	Total output current sourced by sum of all I/Os and control pins(2)	-80	
$I_{INJ(PIN)}$	Injected current on TT, FT, FTf and B pins(3)	-5 /+0	
	Injected current on TC and RST pin(4)	±5	
	Injected current on TTa pins(5)	±5	
$\Sigma I_{INJ(PIN)}$	Total injected current (sum of all I/O and control pins)(6)	±25	

1. All main power (V_{DD}, V_{DDA}) and ground (V_{SS} and V_{SSA}) pins must always be connected to the external power supply, in the permitted range.
2. This current consumption must be correctly distributed over all I/Os and control pins. The total output current must not be sunk/sourced between two consecutive power supply pins referring to high pin count LQFP packages.
3. Positive injection is not possible on these I/Os and does not occur for input voltages lower than the specified maximum value.
4. A positive injection is induced by $V_{IN} > V_{DD}$ while a negative injection is induced by $V_{IN} < V_{SS}$. $I_{INJ(PIN)}$ must never be exceeded. Refer to *Table 16: Voltage characteristics* for the maximum allowed input voltage values.
5. A positive injection is induced by $V_{IN} > V_{DDA}$ while a negative injection is induced by $V_{IN} < V_{SS}$. $I_{INJ(PIN)}$ must never be exceeded. Refer also to *Table 16: Voltage characteristics* for the maximum allowed input voltage values. Negative injection disturbs the analog performance of the device. See note 2.
6. When several inputs are submitted to a current injection, the maximum $\Sigma I_{INJ(PIN)}$ is the absolute sum of the positive and negative injected currents (instantaneous values).

Table 18. Thermal characteristics

Symbol	Ratings	Value	Unit
T_{STG}	Storage temperature range	–65 to +150	°C
T_J	Maximum junction temperature	150	°C

6.3 Operating conditions

6.3.1 General operating conditions

Table 19. General operating conditions

Symbol	Parameter	Conditions	Min.	Max.	Unit
f_{HCLK}	Internal AHB clock frequency	-	0	72	MHz
f_{PCLK1}	Internal APB1 clock frequency	-	0	36	MHz
f_{PCLK2}	Internal APB2 clock frequency	-	0	72	MHz
V_{DD}	Standard operating voltage	-	2	3.6	V
V_{DD18}	Core, SRAM and Flash memory power supply	-	1.65	1.95	V
V_{DDA}	Analog operating voltage (OPAMP and DAC not used)	Must have a potential equal to or higher than V_{DD}	2	3.6	V
	Analog operating voltage (OPAMP and DAC used)		2.4	3.6	
V_{BAT}	Backup operating voltage	-	1.65	3.6	V
V_{IN}	I/O input voltage	TC I/O	–0.3	V_{DD}+0.3	V
		TT I/O	-0.3	3.6	
		TTa I/O	–0.3	V_{DDA}+0.3	
		FT and FTf I/O(1)	–0.3	5.5	
		BOOT0	0	5.5	
PD	Power dissipation at T_A = 85 °C for suffix 6 or T_A = 105 °C for suffix 7(2)	LQFP64	-	444	mW
		LQFP48	-	364	mW
		LQFP32	-	333	mW
		UFQFPN32	-	540	mW
		WLCSP49	-	414	mW
T_A	Ambient temperature for 6 suffix version	Maximum power dissipation	–40	85	°C
		Low power dissipation(3)	–40	105	
	Ambient temperature for 7 suffix version	Maximum power dissipation	–40	105	°C
		Low power dissipation(3)	–40	125	
T_J	Junction temperature range	6 suffix version	–40	105	°C
		7 suffix version	–40	125	

1. To sustain a voltage higher than V_{DD}+0.3 V, the internal pull-up/pull-down resistors must be disabled.
2. If T_A is lower, higher P_D values are allowed as long as T_J does not exceed T_{Jmax} (see *Table 81: Package thermal characteristics*).
3. In low power dissipation state, T_A can be extended to this range as long as T_J does not exceed T_{Jmax} (see *Section 7.7: Thermal characteristics*).

6.3.2 Operating conditions at power-up / power-down

The parameters given in *Table 20* are derived from tests performed under the ambient temperature condition summarized in *Table 19*.

Table 20. Operating conditions at power-up / power-down

Symbol	Parameter	Conditions	Min.	Max.	Unit
t_{VDD}	V_{DD} rise time rate	-	0	∞	µs/V
	V_{DD} fall time rate		20	∞	
t_{VDDA}	V_{DDA} rise time rate	-	0	∞	
	V_{DDA} fall time rate		20	∞	

6.3.3 Characteristics of the embedded reset and power-control block

The parameters given in *Table 21* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 19*.

Table 21. Embedded reset and power control block characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
$V_{POR/PDR}$(1)	Power on/power down reset threshold	Falling edge	1.8(2)	1.88	1.96	V
		Rising edge	1.84	1.92	2.0	V
$V_{PDRhyst}$(1)	PDR hysteresis	-	-	40	-	mV
$t_{RSTTEMPO}$(3)	POR reset temporization	-	1.5	2.5	4.5	ms

1. The PDR detector monitors V_{DD} and also V_{DDA} (if kept enabled in the option bytes). The POR detector monitors only V_{DD}.
2. The product behavior is guaranteed by design down to the minimum $V_{POR/PDR}$ value.
3. Guaranteed by design, not tested in production.

Table 22. Programmable voltage detector characteristics

Symbol	Parameter	Conditions	Min.(1)	Typ.	Max.(1)	Unit
V_{PVD0}	PVD threshold 0	Rising edge	2.1	2.18	2.26	V
		Falling edge	2	2.08	2.16	
V_{PVD1}	PVD threshold 1	Rising edge	2.19	2.28	2.37	
		Falling edge	2.09	2.18	2.27	
V_{PVD2}	PVD threshold 2	Rising edge	2.28	2.38	2.48	
		Falling edge	2.18	2.28	2.38	
V_{PVD3}	PVD threshold 3	Rising edge	2.38	2.48	2.58	
		Falling edge	2.28	2.38	2.48	
V_{PVD4}	PVD threshold 4	Rising edge	2.47	2.58	2.69	
		Falling edge	2.37	2.48	2.59	
V_{PVD5}	PVD threshold 5	Rising edge	2.57	2.68	2.79	
		Falling edge	2.47	2.58	2.69	
V_{PVD6}	PVD threshold 6	Rising edge	2.66	2.78	2.9	
		Falling edge	2.56	2.68	2.8	
V_{PVD7}	PVD threshold 7	Rising edge	2.76	2.88	3	
		Falling edge	2.66	2.78	2.9	
$V_{PVDhyst}$(2)	PVD hysteresis	-	-	100	-	mV
IDD(PVD)	PVD current consumption	-	-	0.15	0.26	µA

1. Data based on characterization results only, not tested in production.
2. Guaranteed by design, not tested in production.

6.3.4 Embedded reference voltage

The parameters given in *Table 23* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 19*.

Table 23. Embedded internal reference voltage

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{REFINT}	Internal reference voltage	–40 °C < T_A < +105 °C	1.20	1.23	1.25	V
$T_{S_vrefint}$	ADC sampling time when reading the internal reference voltage	-	2.2	-	-	µs
V_{RERINT}	Internal reference voltage spread over the temperature range	V_{DD} = 31.8 V ±10 mV	-	-	10(1)	mV
T_{Coeff}	Temperature coefficient	-	-	-	100(1)	ppm/°C

1. Guaranteed by design, not tested in production.

Table 24. Internal reference voltage calibration values

Calibration value name	Description	Memory address
V_{REFINT_CAL}	Raw data acquired at temperature of 30 °C V_{DDA}= 3.3 V	0x1FFF F7BA - 0x1FFF F7BB

6.3.5 Supply current characteristics

The current consumption is a function of several parameters and factors such as the operating voltage, ambient temperature, I/O pin loading, device software configuration, operating frequencies, I/O pin switching rate, program location in memory and executed binary code.
The current consumption is measured as described in *Figure 13: Scheme of the current-consumption measurement*.
All Run-mode current consumption measurements given in this section are performed with a reduced code that gives a consumption equivalent to CoreMark code.

Note: The total current consumption is the sum of the IDD and IDDA values.

Typical and maximum current consumption

The MCU is placed under the following conditions:

- All I/O pins are in input mode with a static value at V_{DD} or V_{SS} (no load)
- All peripherals are disabled except when explicitly mentioned
- The Flash memory access time is adjusted to the f_{HCLK} frequency (0 wait state from 0 to 24 MHz,1 wait state from 24 to 48 MHz and 2 wait states from 48 to 72 MHz)
- Prefetch in ON (reminder: this bit must be set before clock setting and bus prescaling)
- When the peripherals are enabled $f_{PCLK2} = f_{HCLK}$ and $f_{PCLK1} = f_{HCLK/2}$
- When f_{HCLK} > 8 MHz, the PLL is ON and the PLL input is equal to HSI/2 (4 MHz) or HSE (8 MHz) in bypass mode.

The parameters given in *Table 25* to *Table 29* are derived from tests performed under ambient temperature and supply voltage conditions summarized in *Table 19*.

Table 25. Typical and maximum current consumption from V_{DD} supply at V_{DD} = 3.6V

Symbol	Parameter	Conditions	f_{HCLK}	All peripherals enabled				All peripherals disabled				Unit
				Typ.	Max. @ T_A(1)			Typ.	Max. @ T_A(1)			
					25 °C	85 °C	105 °C		25 °C	85 °C	105 °C	
I_{DD}	Supply current in Run mode, executing from Flash	External clock (HSE bypass)	72 MHz	71.4	77.9	79.1	80.0	27.1	32.2	32.4	32.4	mA
			64 MHz	63.9	70.6	71.3	71.5	24.2	27.0	27.5	27.7	
			48 MHz	49.5	56.6	57.1	57.7	18.7	21.4	21.6	21.9	
			32 MHz	34.0	38.6	38.9	39.2	12.9	14.6	14.9	15.9	
			24 MHz	25.9	30.2	30.4	30.6	10.0	11.1	11.2	12.3	
			8 MHz	9.3	14.1	14.3	14.4	3.3	4.0	4.4	5.1	
			1 MHz	3.5	8.9	9.1	9.5	0.7	0.9	1.0	1.2	
		Internal clock (HSI)	64 MHz	61.6	68.1	68.8	70.1	24.1	27.0	27.1	27.2	
			48 MHz	48.1	54.6	54.8	55.1	18.6	21.6	21.7	21.9	
			32 MHz	33.3	37.8	37.9	38.0	12.7	14.4	14.9	16.0	
			24 MHz	25.7	29.8	29.8	30.0	10.0	11.1	11.2	12.3	
			8 MHz	9.7	12.2	12.3	12.8	3.4	3.8	4.2	5.0	
	Supply current in Run mode, executing from RAM	External clock (HSE bypass)	72 MHz	71.3	77.8	78.7	78.9	27.6	32.1	32.2	32.3	
			64 MHz	63.8	70.5	70.7	70.9	24.5	27.2	27.6	27.7	
			48 MHz	49.3	56.5	56.9	57.4	18.1	21.6	21.8	21.8	
			32 MHz	33.9	37.7	37.9	38.0	12.9	14.9	14.9	15.9	
			24 MHz	25.8	28.8	29.0	29.2	9.8	11.1	11.3	11.5	
			8 MHz	9.0	13.2	13.3	13.8	3.2	3.6	4.0	4.6	
			1 MHz	3.2	7.6	7.8	8.0	0.3	0.4	0.8	1.2	
		Internal clock (HSI)	64 MHz	61.3	66.9	67.3	67.8	24.1	26.9	27.0	27.1	
			48 MHz	48.0	52.4	52.6	53.1	19.1	21.6	21.6	22.1	
			32 MHz	33.1	35.6	35.8	36.6	12.6	14.8	14.9	15.9	
			24 MHz	25.6	28.5	28.7	28.8	9.8	11.1	11.3	11.5	
			8 MHz	9.7	11.6	11.6	11.7	3.0	3.1	4.1	4.7	
I_{DD}	Supply current in Sleep mode, executing from Flash or RAM	External clock (HSE bypass)	72 MHz	55.5	58.7	61.1	61.9	7.0	7.3	8.4	8.5	mA
			64 MHz	49.8	52.7	54.5	54.8	6.3	6.7	7.0	7.8	
			48 MHz	38.5	40.6	41.7	41.8	4.6	5.1	5.6	5.9	
			32 MHz	26.9	28.8	29.2	29.5	3.0	3.3	4.0	4.5	
			24 MHz	19.1	23.2	23.7	23.9	2.4	2.5	3.2	3.8	
			8 MHz	7.1	11.5	11.7	11.9	0.6	0.9	1.2	2.1	
			1 MHz	3.0	7.4	7.7	7.9	0.3	0.3	0.4	1.2	
		Internal clock (HSI)	64 MHz	47.7	52.4	52.6	52.8	5.4	6.5	6.8	7.5	
			48 MHz	35.0	40.4	40.6	40.8	4.3	4.7	5.2	5.7	
			32 MHz	23.7	27.7	28.3	28.8	2.9	3.1	3.2	4.4	
			24 MHz	18.5	23.8	24.0	24.2	1.3	1.7	2.2	2.7	
			8 MHz	7.5	9.6	9.7	9.7	0.5	0.7	1.1	2.0	

1. Data based on characterization results, not tested in production unless otherwise specified.

Table 26. Typical and maximum current consumption from the V_{DDA} supply

Symbol	Parameter	Conditions (1)	f_{HCLK}	V_{DDA} = 2.4 V				V_{DDA} = 3.6 V				Unit
				Typ.	Max. @ T_A(2)			Typ.	Max. @ T_A(2)			
					25 °C	85 °C	105 °C		25 °C	85 °C	105 °C	
I_{DDA}	Supply current in Run/Sleep mode, code executing from Flash or RAM	HSE bypass	72 MHz	224	252	265	269	245	272	288	295	µA
			64 MHz	196	225	237	241	214	243	257	263	
			48 MHz	147	174	183	186	159	186	196	201	
			32 MHz	100	126	133	135	109	133	142	145	
			24 MHz	79	102	107	108	85	108	113	116	
			8 MHz	3	5	5	6	4	6	6	7	
			1 MHz	3	5	5	6	3	5	6	6	
		HSI clock	64 MHz	259	288	304	309	285	315	332	338	
			48 MHz	208	239	251	254	230	258	271	277	
			32 MHz	162	190	198	202	179	206	216	219	
			24 MHz	140	168	175	178	155	181	188	191	
			8 MHz	62	85	88	89	71	94	96	98	

1. Current consumption from the V_{DDA} supply is independent of whether the peripherals are on or off. Furthermore when the PLL is off, I_{DDA} is independent from the frequency.
2. Data based on characterization results, not tested in production.

Table 27. Typical and maximum V_{DD} consumption in Stop and Standby modes

Symbol	Parameter	Conditions	Typ. @V_{DD} (V_{DD}=V_{DDA})						Max.(1)			Unit
			2.0 V	2.4 V	2.7 V	3.0 V	3.3 V	3.6 V	T_A = 25 °C	T_A = 85 °C	T_A = 105 °C	
I_{DD}	Supply current in Stop mode	Regulator in run mode, all oscillators OFF	17.51	17.68	17.84	18.17	18.57	19.39	30.6	232.5	612.2	µA
		Regulator in low-power mode, all oscillators OFF	6.44	6.51	6.60	6.73	6.96	7.20	20.0	246.4	585.0	
	Supply current in Standby mode	LSI ON and IWDG ON	0.73	0.89	1.02	1.14	1.28	1.44	-	-	-	
		LSI OFF and IWDG OFF	0.55	0.66	0.75	0.85	0.93	1.01	4.9	7.0	7.9	

1. Data based on characterization results, not tested in production unless otherwise specified.

Table 28. Typical and maximum V_{DDA} consumption in Stop and Standby modes

Symbol	Parameter	Conditions		Typ. @V_{DD} (V_{DD} = V_{DDA})						Max.(1)			Unit
				2.0 V	2.4 V	2.7 V	3.0 V	3.3 V	3.6 V	T_A = 25 °C	T_A = 85 °C	T_A = 105 °C	
I_{DDA}	Supply current in Stop mode	V_{DDA} supervisor ON	Regulator in run/low-power mode, all oscillators OFF	1.67	1.79	1.91	2.04	2.19	2.35	2.5	5.9	6.2	µA
	Supply current in Standby mode		LSI ON and IWDG ON	2.06	2.24	2.41	2.60	2.80	3.04	-	-	-	
			LSI OFF and IWDG OFF	1.54	1.68	1.78	1.92	2.06	2.22	2.6	3.0	3.8	
	Supply current in Stop mode	V_{DDA} supervisor OFF	Regulator in run/low-power mode, all oscillators OFF	0.97	0.99	1.03	1.07	1.14	1.22	-	-	-	
	Supply current in Standby mode		LSI ON and IWDG ON	1.36	1.44	1.52	1.62	1.76	1.91	-	-	-	
			LSI OFF and IWDG OFF	0.86	0.88	0.91	0.95	1.03	1.09	-	-	-	

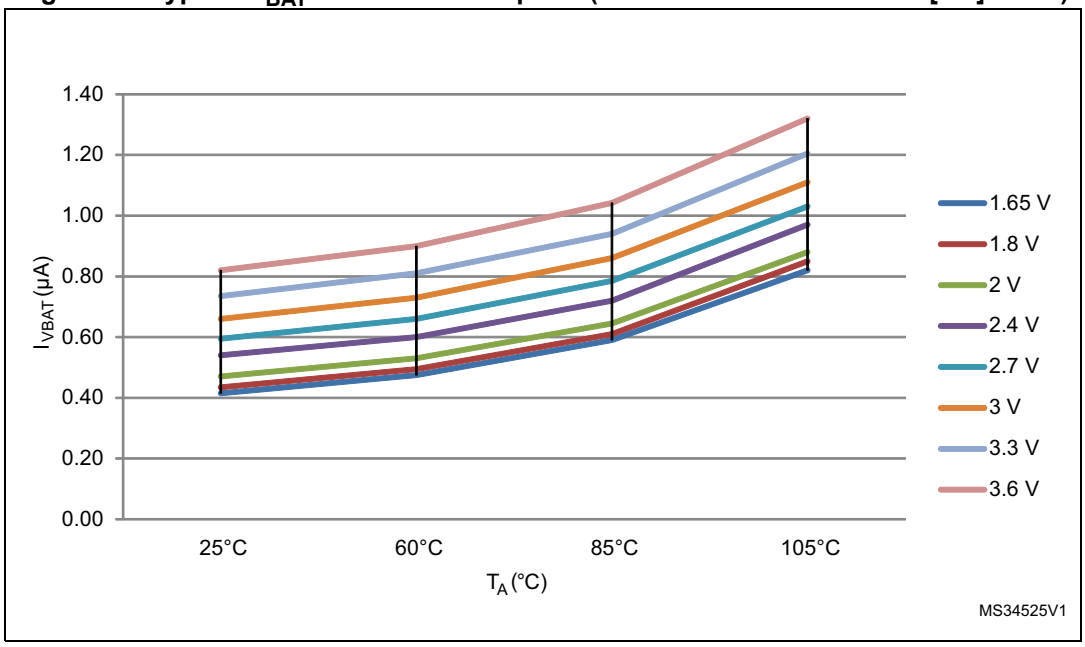
1. Data based on characterization results, not tested in production.

Table 29. Typical and maximum current consumption from V_{BAT} supply

Symbol	Parameter	Conditions (1)	Typ.@V_{BAT}								Max. @V_{BAT}= 3.6V(2)			Unit
			1.65V	1.8V	2V	2.4V	2.7V	3V	3.3V	3.6V	T_A= 25°C	T_A= 85°C	T_A= 105°C	
I_{DD_VBAT}	Backup domain supply current	LSE & RTC ON; “Xtal mode” lower driving capability; LSEDRV[1:0] = '00'	0.42	0.44	0.47	0.54	0.60	0.66	0.74	0.82	-	-	-	µA
		LSE & RTC ON; “Xtal mode” higher driving capability; LSEDRV[1:0] = '11'	0.71	0.74	0.77	0.85	0.91	0.98	1.06	1.16	-	-	-	

1. Crystal used: Abracon ABS07-120-32.768 kHz-T with a CL of 6 pF for typical values.
2. Data based on characterization results, not tested in production.

Figure 14. Typical V_{BAT} current consumption (LSE and RTC ON/LSEDRV[1:0] = '00')



Typical current consumption

The MCU is placed under the following conditions:

- $V_{DD} = V_{DDA} = 3.3$ V
- All I/O pins available on each package are in analog input configuration
- The Flash access time is adjusted to f_{HCLK} frequency (0 wait states from 0 to 24 MHz, 1 wait state from 24 to 48 MHz and 2 wait states from 48 MHz to 72 MHz), and Flash prefetch is ON
- When the peripherals are enabled, $f_{APB1} = f_{AHB/2}$, $f_{APB2} = f_{AHB}$
- PLL is used for frequencies greater than 8 MHz
- AHB prescaler of 2, 4, 8, 16 and 64 is used for the frequencies 4 MHz, 2 MHz, 1 MHz, 500 kHz and 125 kHz respectively.
- Typical current consumption in Run mode, code with data processing running from Flash

Table 30. Typical current consumption in Run mode, code with data processing running from Flash memory

Symbol	Parameter	Conditions	f_{HCLK}	Typ.		Unit
				Peripherals enabled	Peripherals disabled	
I_{DD}	Supply current in Run mode from V_{DD} supply	Running from HSE crystal clock 8 MHz, code executing from Flash memory	72 MHz	70.6	25.2	mA
			64 MHz	60.3	22.6	
			48 MHz	46.0	17.3	
			32 MHz	31.3	12.0	
			24 MHz	25.0	9.3	
			16 MHz	16.2	6.5	
			8 MHz	8.4	3.55	
			4 MHz	4.75	2.21	
			2 MHz	2.81	1.52	
			1 MHz	1.82	1.17	
			500 kHz	1.34	0.94	
			125 kHz	0.93	0.82	
I_{DDA}(1) (2)	Supply current in Run mode from V_{DDA} supply		72 MHz	240.0	234.0	µA
			64 MHz	209.9	208.6	
			48 MHz	154.5	153.5	
			32 MHz	104.1	103.6	
			24 MHz	80.2	80.0	
			16 MHz	56.8	56.6	
			8 MHz	1.14	1.14	
			4 MHz	1.14	1.14	
			2 MHz	1.14	1.14	
			1 MHz	1.14	1.14	
			500 kHz	1.14	1.14	
			125 kHz	1.14	1.14	

1. V_{DDA} supervisor is OFF.
2. When peripherals are enabled, the power consumption of the analog part of peripherals such as ADC, DAC, Comparators, OpAmp and others, is not included. Refer to the tables of characteristics in the subsequent sections.

Table 31. Typical current consumption in Sleep mode, code running from Flash or RAM

Symbol	Parameter	Conditions	f_{HCLK}	Typ.		Unit
				Peripherals enabled	Peripherals disabled	
I_{DD}	Supply current in Sleep mode from V_{DD} supply	Running from HSE crystal clock 8 MHz, code executing from Flash or RAM	72 MHz	51.8	6.3	mA
			64 MHz	46.4	5.7	
			48 MHz	35.0	4.40	
			32 MHz	23.7	3.13	
			24 MHz	18.0	2.49	
			16 MHz	12.2	1.85	
			8 MHz	6.2	0.99	
			4 MHz	3.68	0.88	
			2 MHz	2.26	0.80	
			1 MHz	1.55	0.76	
			500 kHz	1.20	0.74	
			125 kHz	0.89	0.72	
I_{DDA}(1) (2)	Supply current in Sleep mode from V_{DDA} supply		72 MHz	239.0	236.7	µA
			64 MHz	209.4	207.8	
			48 MHz	154.0	152.9	
			32 MHz	103.7	103.2	
			24 MHz	80.1	79.8	
			16 MHz	56.7	56.6	
			8 MHz	1.14	1.14	
			4 MHz	1.14	1.14	
			2 MHz	1.14	1.14	
			1 MHz	1.14	1.14	
			500 kHz	1.14	1.14	
			125 kHz	1.14	1.14	

1. V_{DDA} supervisor is OFF.
2. When peripherals are enabled, the power consumption of the analog part of peripherals such as ADC, DAC, Comparators, OpAmp and others, is not included. Refer to the tables of characteristics in the subsequent sections.

I/O system current consumption

The current consumption of the I/O system has two components: static and dynamic.

I/O static current consumption

All the I/Os used as inputs with pull-up generate current consumption when the pin is externally held low. The value of this current consumption can be simply computed by using the pull-up/pull-down resistors values given in *Table 50: I/O static characteristics*.

For the output pins, any external pull-down or external load must also be considered to estimate the current consumption.

Additional I/O current consumption is due to I/Os configured as inputs if an intermediate voltage level is externally applied. This current consumption is caused by the input Schmitt trigger circuits used to discriminate the input value. Unless this specific configuration is required by the application, this supply current consumption can be avoided by configuring these I/Os in analog mode. This is notably the case of ADC input pins that must be configured as analog inputs.

Caution: Any floating input pin can also settle to an intermediate voltage level or switch inadvertently, as a result of external electromagnetic noise. To avoid current consumption related to floating pins, they must either be configured in analog mode, or forced internally to a definite digital value. This can be done either by using pull-up/down resistors or by configuring the pins in output mode.

I/O dynamic current consumption

In addition to the internal peripheral current consumption (see *Table 33: Peripheral current consumption*), the I/Os used by an application also contribute to the current consumption. When an I/O pin switches, it uses the current from the MCU supply voltage to supply the I/O pin circuitry and to charge/discharge the capacitive load (internal or external) connected to the pin:

$$I_{SW} = V_{DD} \times f_{SW} \times C$$

where:

I_{SW} is the current sunk by a switching I/O to charge/discharge the capacitive load

V_{DD} is the MCU supply voltage

f_{SW} is the I/O switching frequency

C is the total capacitance seen by the I/O pin: $C = C_{INT} + C_{EXT+CS}$

The test pin is configured in push-pull output mode and is toggled by software at a fixed frequency.

Table 32. Switching output I/O current consumption

Symbol	Parameter	Conditions[1]	I/O toggling frequency (f_{SW})	Typ.	Unit
I_{SW}	I/O current consumption	V_{DD} = 3.3 V C_{ext} = 0 pF $C = C_{INT} + C_{EXT} + C_S$	2 MHz	0.90	mA
			4 MHz	0.93	
			8 MHz	1.16	
			18 MHz	1.60	
			36 MHz	2.51	
		V_{DD} = 3.3 V C_{ext} = 10 pF $C = C_{INT} + C_{EXT} + C_S$	2 MHz	0.93	
			4 MHz	1.06	
			8 MHz	1.47	
			18 MHz	2.26	
			36 MHz	3.39	
		V_{DD} = 3.3 V C_{ext} = 22 pF $C = C_{INT} + C_{EXT} + C_S$	2 MHz	1.03	
			4 MHz	1.30	
			8 MHz	1.79	
			18 MHz	3.01	
			36 MHz	5.99	
		V_{DD} = 3.3 V C_{ext} = 33 pF $C = C_{INT} + C_{EXT} + C_S$	2 MHz	1.10	
			4 MHz	1.31	
			8 MHz	2.06	
			18 MHz	3.47	
			36 MHz	8.35	
		V_{DD} = 3.3 V C_{ext} = 47 pF $C = C_{INT} + C_{EXT} + C_S$	2 MHz	1.20	
			4 MHz	1.54	
			8 MHz	2.46	
			18 MHz	4.51	
			36 MHz	9.98	

1. CS = 5 pF (estimated value).

On-chip peripheral current consumption

The MCU is placed under the following conditions:

- All I/O pins are in analog input configuration
- All peripherals are disabled unless otherwise mentioned
- The given value is calculated by measuring the current consumption:
  - With all peripherals clocked off
  - With only one peripheral clocked on
- Ambient operating temperature at 25°C and $V_{DD} = V_{DDA} = 3.3$ V

Table 33. Peripheral current consumption

Peripheral	Typical consumption(1)	Unit
	I_{DD}	
BusMatrix (2)	11.1	µA/MHz
DMA1	8.0	
CRC	2.1	
GPIOA	8.7	
GPIOB	8.4	
GPIOC	8.4	
GPIOD	2.6	
GPIOF	1.7	
TSC	4.7	
ADC1&2	17.4	
APB2-Bridge (3)	3.3	
SYSCFG	4.2	
TIM1	32.3	
USART1	20.3	
TIM15	13.8	
TIM16	9.7	
TIM17	10.3	
HRTIM	324.2	
APB1-Bridge (3)	5.3	
TIM2	43.4	
TIM3	34.0	
TIM6	9.7	
TIM7	10.3	
WWDG	6.9	
USART2	18.8	
USART3	19.1	

Table 33. Peripheral current consumption (continued)

Peripheral	Typical consumption(1)	Unit
	I_{DD}	
I2C1	13.3	µA/MHz
CAN	31.3	
PWR	4.7	
DAC	15.4	
DAC2	8.6	
SPI1	8.2	

1. The power consumption of the analog part (I_{DDA}) of peripherals such as ADC, DAC, Comparators, OpAmp and others, is not included. Refer to the tables of characteristics in the subsequent sections.
2. BusMatrix is automatically active when at least one master is ON (CPU or DMA1).
3. The APBx bridge is automatically active when at least one peripheral is ON on the same bus.

6.3.6 Wakeup time from low-power mode

The wakeup times given in *Table 34* are measured starting from the wakeup event trigger up to the first instruction executed by the CPU:

- For Stop or Sleep mode: the wakeup event is WFE.
- WKUP1 (PA0) pin is used to wake up from Standby, Stop and Sleep modes.

All timings are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 19*.

Table 34. Low-power mode wakeup timings

Symbol	Parameter	Conditions	Typ. @V_{DD}, $V_{DD} = V_{DDA}$						Max.	Unit
			2.0 V	2.4 V	2.7 V	3 V	3.3 V	3.6 V		
t_{WUSTOP}	Wakeup from Stop mode	Regulator in run mode	4.3	4.1	4.0	3.9	3.8	3.7	4.5	µs
		Regulator in low-power mode	7.8	6.7	6.1	5.9	5.5	5.3	9	
$t_{WUSTANDBY}$(1)	Wakeup from Standby mode	LSI and IWDG OFF	74.4	64.3	60.0	56.9	54.3	51.1	103	
$t_{WUSLEEP}$	Wakeup from Sleep mode	-	6						-	CPU clock cycles

1. Data based on characterization results, not tested in production.

Table 35. Wakeup time using USART(1)

Symbol	Parameter	Conditions	Typ	Max	Unit
$t_{WUUSART}$	Wakeup time needed to calculate the maximum USART baudrate allowing to wake up from stop mode when USART clock source is HSI	Stop mode with main regulator in low power mode	-	13.125	µs
		Stop mode with main regulator in run mode	-	3.125	

1. Guaranteed by design.

6.3.7 External clock source characteristics

High-speed external user clock generated from an external source

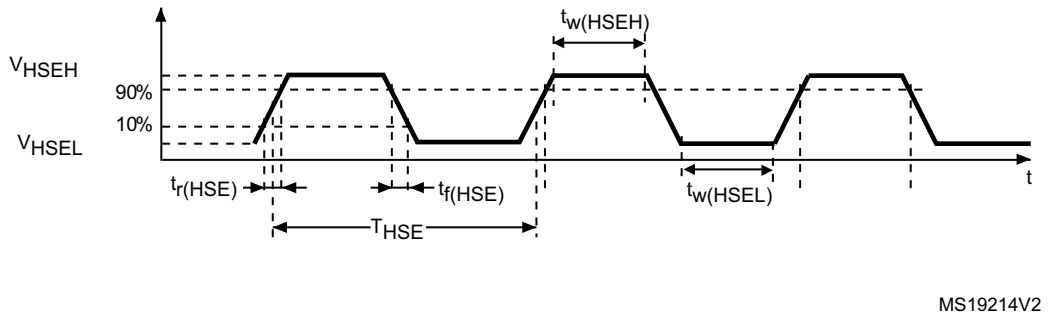
In bypass mode the HSE oscillator is switched off and the input pin is a standard GPIO. The external clock signal has to respect the I/O characteristics in *Section 6.3.14*. However, the recommended clock input waveform is shown in *Figure 15*.

Table 36. High-speed external user clock characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
f_{HSE_ext}	User external clock source frequency(1)	-	1	8	32	MHz
V_{HSEH}	OSC_IN input pin high-level voltage		$0.7V_{DD}$	-	V_{DD}	V
V_{HSEL}	OSC_IN input pin low-level voltage		V_{SS}	-	$0.3V_{DD}$	
$t_{w(HSEH)}$ $t_{w(HSEL)}$	OSC_IN high or low time(1)		15	-	-	ns
$t_{r(HSE)}$ $t_{f(HSE)}$	OSC_IN rise or fall time(1)		-	-	20	

1. Guaranteed by design, not tested in production.

Figure 15. High-speed external clock source AC timing diagram



Low-speed external user clock generated from an external source

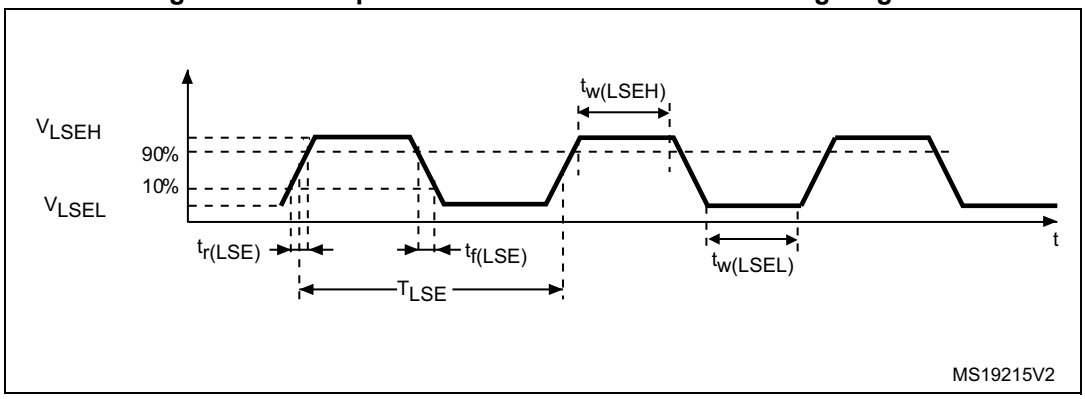
In bypass mode the LSE oscillator is switched off and the input pin is a standard GPIO. The external clock signal has to respect the I/O characteristics in *Section 6.3.14*. However, the recommended clock input waveform is shown in *Figure 16*.

Table 37. Low-speed external user clock characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
f_{LSE_ext}	User External clock source frequency(1)	-	-	32.768	1000	kHz
V_{LSEH}	OSC32_IN input pin high-level voltage		$0.7V_{DD}$	-	V_{DD}	V
V_{LSEL}	OSC32_IN input pin low-level voltage		V_{SS}	-	$0.3V_{DD}$	
$t_{w(LSEH)}$ $t_{w(LSEL)}$	OSC32_IN high or low time(1)		450	-	-	ns
$t_{r(LSE)}$ $t_{f(LSE)}$	OSC32_IN rise or fall time(1)		-	-	50	

1. Guaranteed by design, not tested in production.

Figure 16. Low-speed external clock source AC timing diagram



High-speed external clock generated from a crystal/ceramic resonator

The high-speed external (HSE) clock can be supplied with a 4 to 32 MHz crystal/ceramic resonator oscillator. All the information given in this paragraph are based on design simulation results obtained with typical external components specified in *Table 38*. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

Table 38. HSE oscillator characteristics

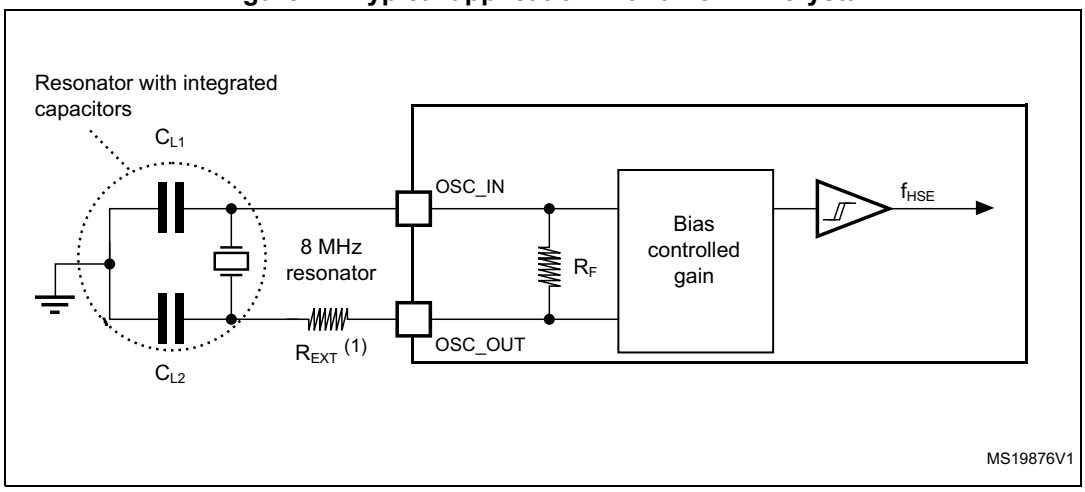
Symbol	Parameter	Conditions[1]	Min.[2]	Typ.	Max.[2]	Unit
f_{OSC_IN}	Oscillator frequency	-	4	8	32	MHz
R_F	Feedback resistor	-	-	200	-	kΩ
I_{DD}	HSE current consumption	During startup[3]	-	-	8.5	mA
		V_{DD}= 3.3 V, Rm= 30Ω, CL=10 pF@8 MHz	-	0.4	-	
		V_{DD}= 3.3 V, Rm= 45Ω, CL=10 pF@8 MHz	-	0.5	-	
		V_{DD}= 3.3 V, Rm= 30Ω, CL=5 pF@32 MHz	-	0.8	-	
		V_{DD}= 3.3 V, Rm= 30Ω, CL=10 pF@32 MHz	-	1	-	
		V_{DD}= 3.3 V, Rm= 30Ω, CL=20 pF@32 MHz	-	1.5	-	
g_m	Oscillator transconductance	Startup	10	-	-	mA/V
$t_{SU(HSE)}$[4]	Startup time	V_{DD} is stabilized	-	2	-	ms

1. Resonator characteristics given by the crystal/ceramic resonator manufacturer.
2. Guaranteed by design, not tested in production.
3. This consumption level occurs during the first 2/3 of the $t_{SU(HSE)}$ startup time.
4. $t_{SU(HSE)}$ is the startup time measured from the moment it is enabled (by software) to a stabilized 8 MHz oscillation is reached. This value is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer.

For C_{L1} and C_{L2}, it is recommended to use high-quality external ceramic capacitors in the 5 pF to 25 pF range (typ.), designed for high-frequency applications, and selected to match the requirements of the crystal or resonator (see *Figure 17*). C_{L1} and C_{L2} are usually the same size. The crystal manufacturer typically specifies a load capacitance which is the series combination of C_{L1} and C_{L2}. PCB and MCU pin capacitance must be included (10 pF can be used as a rough estimate of the combined pin and board capacitance) when sizing C_{L1} and C_{L2}.

Note: For information on selecting the crystal, refer to the application note AN2867 "Oscillator design guide for ST microcontrollers" available from the ST website www.st.com.

Figure 17. Typical application with an 8 MHz crystal



1. R_{EXT} value depends on the crystal characteristics.

Low-speed external clock generated from a crystal/ceramic resonator

The low-speed external (LSE) clock can be supplied with a 32.768 kHz crystal/ceramic resonator oscillator. All the information given in this paragraph are based on design simulation results obtained with typical external components specified in *Table 39*. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

Table 39. LSE oscillator characteristics (f_{LSE} = 32.768 kHz)

Symbol	Parameter	Conditions[1]	Min.[2]	Typ.	Max.[2]	Unit
I_{DD}	LSE current consumption	LSEDRV[1:0]=00 lower driving capability	-	0.5	0.9	µA
		LSEDRV[1:0]=10 medium low driving capability	-	-	1	
		LSEDRV[1:0]=01 medium high-driving capability	-	-	1.3	
		LSEDRV[1:0]=11 higher-driving capability	-	-	1.6	

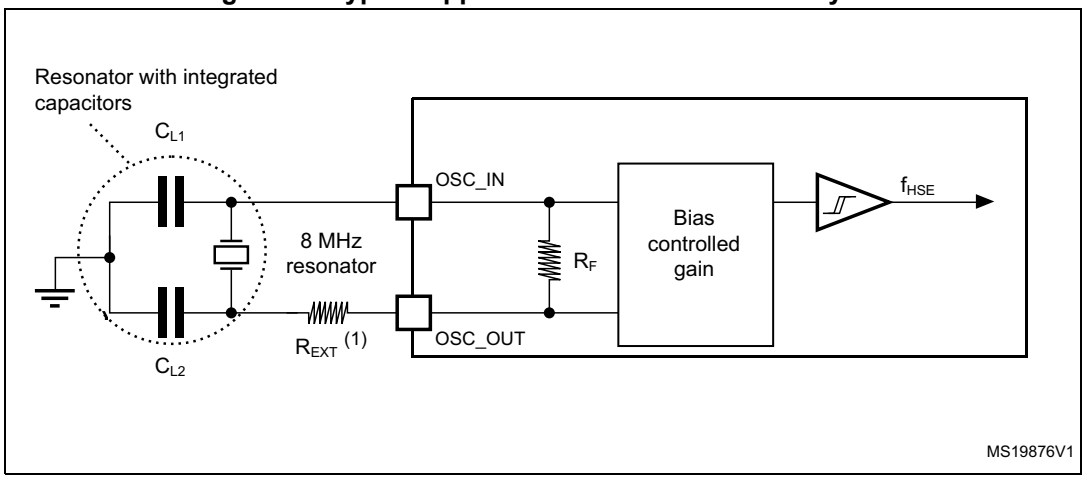
Table 39. LSE oscillator characteristics (f_{LSE} = 32.768 kHz) (continued)

Symbol	Parameter	Conditions[1]	Min.[2]	Typ.	Max.[2]	Unit
g_m	Oscillator transconductance	LSEDRV[1:0]=00 lower-driving capability	5	-	-	µA/V
		LSEDRV[1:0]=10 medium low-driving capability	8	-	-	
		LSEDRV[1:0]=01 medium high-driving capability	15	-	-	
		LSEDRV[1:0]=11 higher-driving capability	25	-	-	
$t_{SU(LSE)}$[3]	Startup time	V_{DD} is stabilized	-	2	-	s

1. Refer to the note and caution paragraphs below the table, and to the application note AN2867 “Oscillator design guide for ST microcontrollers”.
2. Guaranteed by design, not tested in production.
3. $t_{SU(LSE)}$ is the startup time measured from the moment it is enabled (by software) to a stabilized 32.768 kHz oscillation is reached. This value is measured for a standard crystal and it can vary significantly with the crystal manufacturer.

Note: For information on selecting the crystal, refer to the application note AN2867 “Oscillator design guide for ST microcontrollers” available at the ST website www.st.com.

Figure 18. Typical application with a 32.768 kHz crystal



Note: An external resistor is not required between OSC32_IN and OSC32_OUT and it is forbidden to add one.

6.3.8 Internal clock source characteristics

The parameters given in *Table 40* are derived from tests performed under ambient temperature and supply voltage conditions summarized in *Table 19*.

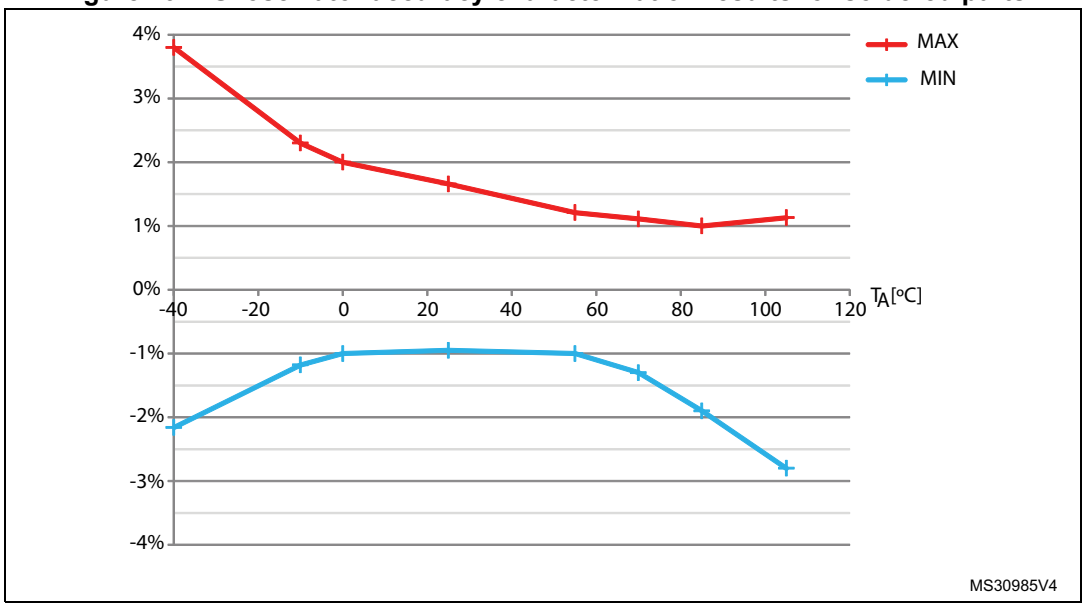
High-speed internal (HSI) RC oscillator

Table 40. HSI oscillator characteristics(1)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
f_{HSI}	Frequency	-	-	8	-	MHz
TRIM	HSI user trimming step	-	-	-	1(2)	%
$DuCy_{(HSI)}$	Duty cycle	-	45(2)	-	55(2)	%
ACC_{HSI}	Accuracy of the HSI oscillator (factory calibrated)	T_A = –40 to 105 °C	–2.8(3)	-	3.8(3)	%
		T_A = –10 to 85 °C	–1.9(3)	-	2.3(3)	
		T_A = 0 to 85 °C	-1.9(3)	-	2(3)	
		T_A = 0 to 70 °C	-1.3(3)	-	2(3)	
		T_A = 0 to 55 °C	–1(3)	-	2(3)	
		T_A = 25 °C(4)	–1	-	1	
$t_{su(HSI)}$	HSI oscillator startup time	-	1(2)	-	2(2)	µs
$I_{DDA(HSI)}$	HSI oscillator power consumption	-	-	80	100(2)	µA

1. V_{DDA} = 3.3 V, T_A = –40 to 105 °C unless otherwise specified.
2. Guaranteed by design, not tested in production.
3. Data based on characterization results, not tested in production.
4. Factory calibrated, parts not soldered

Figure 19. HSI oscillator accuracy characterization results for soldered parts



Low-speed internal (LSI) RC oscillator

Table 41. LSI oscillator characteristics(1)

Symbol	Parameter	Min.	Typ.	Max.	Unit
f_{LSI}	Frequency	30	40	50	kHz
$t_{su(LSI)}$(2)	LSI oscillator startup time	-	-	85	µs
$I_{DD(LSI)}$(2)	LSI oscillator power consumption	-	0.75	1.2	µA

1. V_{DDA} = 3.3 V, T_A = –40 to 105 °C unless otherwise specified.
2. Guaranteed by design, not tested in production.

6.3.9 PLL characteristics

The parameters given in *Table 42* are derived from tests performed under ambient temperature and supply voltage conditions summarized in *Table 19*.

Table 42. PLL characteristics

Symbol	Parameter	Value			Unit
		Min.	Typ.	Max.	
f_{PLL_IN}	PLL input clock(1)	1(2)	-	24(2)	MHz
	PLL input clock duty cycle	40(2)	-	60(2)	%
f_{PLL_OUT}	PLL multiplier output clock	16(2)	-	72	MHz
t_{LOCK}	PLL lock time	-	-	200(2)	µs
Jitter	Cycle-to-cycle jitter	-	-	300(2)	ps

1. Take care of using the appropriate multiplier factors so as to have PLL input clock values compatible with the range defined by f_{PLL_OUT}.
2. Guaranteed by design, not tested in production.

6.3.10 Memory characteristics

Flash memory

The characteristics are given at T_A = –40 to 105 °C unless otherwise specified.

Table 43. Flash memory characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.(1)	Unit
t_{prog}	16-bit programming time	T_A = –40 to +105 °C	40	53.5	60	µs
t_{ERASE}	Page (2 KB) erase time	T_A = –40 to +105 °C	20	-	40	ms
t_{ME}	Mass erase time	T_A = –40 to +105 °C	20	-	40	ms
I_{DD}	Supply current	Write mode	-	-	10	mA
		Erase mode	-	-	12	mA

1. Guaranteed by design, not tested in production.

Table 44. Flash memory endurance and data retention

Symbol	Parameter	Conditions	Value	Unit
			Min.(1)	
N_{END}	Endurance	TA = –40 to +85 °C (6 suffix versions) TA = –40 to +105 °C (7 suffix versions)	10	kcycles
t_{RET}	Data retention	1 kcycle(2) at T_A = 85 °C	30	Years
		1 kcycle(2) at T_A = 105 °C	10	
		10 kcycles(2) at T_A = 55 °C	20	

1. Data based on characterization results, not tested in production.
2. Cycling performed over the whole temperature range.

6.3.11 EMC characteristics

Susceptibility tests are performed on a sample basis during device characterization.

Functional EMS (electromagnetic susceptibility)

While a simple application is executed on the device (toggling 2 LEDs through I/O ports). The device is stressed by two electromagnetic events until a failure occurs. The failure is indicated by the LEDs:

- **Electrostatic discharge (ESD)** (positive and negative) is applied to all device pins until a functional disturbance occurs. This test is compliant with the IEC 61000-4-2 standard.
- **FTB**: A Burst of Fast Transient voltage (positive and negative) is applied to V_{DD} and V_{SS} through a 100 pF capacitor, until a functional disturbance occurs. This test is compliant with the IEC 61000-4-4 standard.

A device reset allows normal operations to be resumed.

The test results are given in *Table 45*. They are based on the EMS levels and classes defined in "*EMC design guide for ST microcontrollers*" application note (AN1709).

Table 45. EMS characteristics

Symbol	Parameter	Conditions	Level/ Class
V_{FESD}	Voltage limits to be applied on any I/O pin to induce a functional disturbance	V_{DD} = 3.3 V, LQFP64, T_A = +25°C, f_{HCLK} = 72 MHz conforms to IEC 61000-4-2	2B
V_{EFTB}	Fast transient voltage burst limits to be applied through 100 pF on V_{DD} and V_{SS} pins to induce a functional disturbance	V_{DD} = 3.3 V, LQFP64, T_A = +25°C, f_{HCLK} = 72 MHz conforms to IEC 61000-4-4	4A

Designing hardened software to avoid noise problems

EMC characterization and optimization are performed at component level with a typical application environment and simplified MCU software. It must be noted that good EMC performance is highly dependent on the user application and the software in particular.

Therefore it is recommended that the user applies EMC software optimization and prequalification tests in relation with the EMC level requested for his application.

Software recommendations

The software flowchart must include the management of runaway conditions such as:

- Corrupted program counter
- Unexpected reset
- Critical Data corruption (for example control registers)

Prequalification trials

Most of the common failures (unexpected reset and program counter corruption) can be reproduced by manually forcing a low state on the NRST pin or the Oscillator pins for 1 second.

To complete these trials, ESD stress can be applied directly on the device, over the range of specification values. When unexpected behavior is detected, the software can be hardened to prevent unrecoverable errors occurring (see the *"Software techniques for improving microcontrollers EMC performance"* application note (AN1015)).

Electromagnetic interference (EMI)

The electromagnetic field emitted by the device are monitored, while a simple application is executed (toggling 2 LEDs through the I/O ports). This emission test is compliant with the IEC 61967-2 standard that specifies the test board and the pin loading.

Table 46. EMI characteristics

Symbol	Parameter	Conditions	Monitored frequency band	Max vs. [f_{HSE}/f_{HCLK}]	Unit
				8/72 MHz	
S_{EMI}	Peak level	V_{DD} = 3.6 V, T_A =25 °C, LQFP64 package compliant with IEC 61967-2	0.1 to 30 MHz	5	dBµV
			30 to 130 MHz	9	
			130 MHz to 1GHz	31	
			SAE EMI Level	4	-

6.3.12 Electrical sensitivity characteristics

Based on three different tests (ESD, LU) using specific measurement methods, the device is stressed to determine its performance in terms of electrical sensitivity.

Electrostatic discharge (ESD)

Electrostatic discharges (a positive then a negative pulse separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts × (n+1) supply pins). This test conforms to the JESD22-A114/C101 standard.

Table 47. ESD absolute maximum ratings

Symbol	Ratings	Conditions	Class	Maximum value(1)	Unit
V_{ESD} (HBM)	Electrostatic discharge voltage (human body model)	T_A = +25 °C, conforming to JESD22-A114	2	2000	V
V_{ESD} (CDM)	Electrostatic discharge voltage (charge device model)	T_A = +25 °C, conforming to JESD22-C101	II	250	

1. Data based on characterization results, not tested in production.

Static latch-up

Two complementary static tests are required on six parts to assess the latch-up performance:

- A supply overvoltage is applied to each power supply pin
- A current injection is applied to each input, output and configurable I/O pin

These tests are compliant with EIA/JESD 78A IC latch-up standard.

Table 48. Electrical sensitivities

Symbol	Parameter	Conditions	Class
LU	Static latch-up class	T_A = +105 °C conforming to JESD78A	II level A

6.3.13 I/O current injection characteristics

As a general rule, current injection to the I/O pins, due to external voltage below V_{SS} or above V_{DD} (for standard, 3 V-capable I/O pins) must be avoided during normal product operation. However, to give an indication of the robustness of the microcontroller in cases when abnormal injection accidentally happens, susceptibility tests are performed on a sample basis during device characterization.

Functional susceptibility to I/O current injection

While a simple application is executed on the device, the device is stressed by injecting current into the I/O pins programmed in floating input mode. While current is injected into the I/O pin, one at a time, the device is checked for functional failures.

The failure is indicated by an out of range parameter: ADC error above a certain limit (higher than 5 LSB TUE), out of conventional limits of induced leakage current on adjacent pins (out of –5 µA/+0 µA range), or other functional failure (for example reset occurrence or oscillator frequency deviation). The test results are given in the table below.

Table 49. I/O current injection susceptibility

Symbol	Description	Functional susceptibility		Unit
		Negative injection	Positive injection	
I_{INJ}	Injected current on BOOT0	– 0	NA (Injection is not possible)	mA
	Injected current on PC0, PC1, PC2, PC3 (TTa pins) and PF1 pin (FT pin)	-0	+5	
	Injected current on PA0, PA1, PA2, PA3, PA4, PA5, PA6, PA7, PC4, PC5, PB0, PB1, PB2, PB12, PB13, PB14, PB15 with induced leakage current on other pins from this group less than -100 µA or more than +900 µA	-5	+5	
	Injected current on PB11, other TT, FT, and FTf pins	– 5	Injection is not possible	
	Injected current on all other TC, TTa and RESET pins	– 5	+5	

Note: It is recommended to add a Schottky diode (pin to ground) to the analog pins that may potentially inject negative currents.

6.3.14 I/O port characteristics

General input/output characteristics

Unless otherwise specified, the parameters given in *Table 50* are derived from tests performed under the conditions summarized in *Table 19*. All I/Os are CMOS and TTL compliant.

Table 50. I/O static characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{IL}	Low-level input voltage	TT, TC and TTa I/O	-	-	0.3 V_{DD}+0.07 (1)	V
		FT and FTf I/O	-	-	0.475 V_{DD}-0.2 (1)	
		BOOT0	-	-	0.3 V_{DD}–0.3 (1)	
		All I/Os except BOOT0	-	-	0.3 V_{DD} (2)	
V_{IH}	High-level input voltage	TTa and TT I/O	0.445 V_{DD}+0.398 (1)	-	-	
		FT and FTf I/O	0.5 $V_{DD+0.2}$ (1)	-	-	
		BOOT0	0.2 V_{DD}+0.95 (1)	-	-	
		All I/Os except BOOT0	0.7 V_{DD} (2)	-	-	

Table 50. I/O static characteristics (continued)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{hys}	Schmitt trigger hysteresis	TT, TC and TTa I/O	-	200 (1)	-	mV
		FT and FTf I/O	-	100 (1)	-	
		BOOT0	-	300 (1)	-	
I_{lkg}	Input leakage current (3)	TC, FT, TT, FTf and TTa I/O in digital mode $V_{SS} \leq V_{IN} \leq V_{DD}$	-	-	±0.1	µA
		TTa I/O in digital mode $V_{DD} \leq V_{IN} \leq V_{DDA}$	-	-	1	
		TTa I/O in analog mode $V_{SS} \leq V_{IN} \leq V_{DDA}$	-	-	±0.2	
		FT and FTf I/O(4) $V_{DD} \leq V_{IN} \leq 5$ V	-	-	10	
R_{PU}	Weak pull-up equivalent resistor(5)	$V_{IN} = V_{SS}$	25	40	55	kΩ
R_{PD}	Weak pull-down equivalent resistor(5)	$V_{IN} = V_{DD}$	25	40	55	kΩ
C_{IO}	I/O pin capacitance	-	-	5	-	pF

1. Data based on design simulation.
2. Tested in production.
3. Leakage could be higher than the maximum value. If negative current is injected on adjacent pins. Refer to *Table 49: I/O current injection susceptibility*.
4. To sustain a voltage higher than V_{DD} +0.3 V, the internal pull-up/pull-down resistors must be disabled.
5. Pull-up and pull-down resistors are designed with a true resistance in series with a switchable PMOS/NMOS. This PMOS/NMOS contribution to the series resistance is minimum (~10% order).

All I/Os are CMOS and TTL compliant (no software configuration required). Their characteristics cover more than the strict CMOS-technology or TTL parameters. The coverage of these requirements is shown in *Figure 20* and *Figure 21* for standard I/Os.

Figure 20. TC and TTa I/O input characteristics - CMOS port

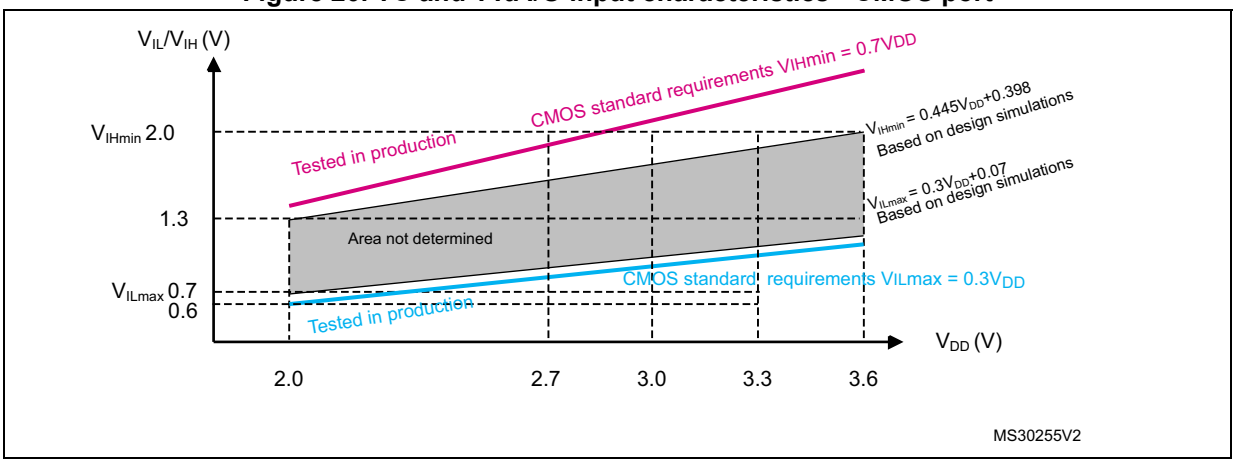


Figure 21. TC and TTa I/O input characteristics - TTL port

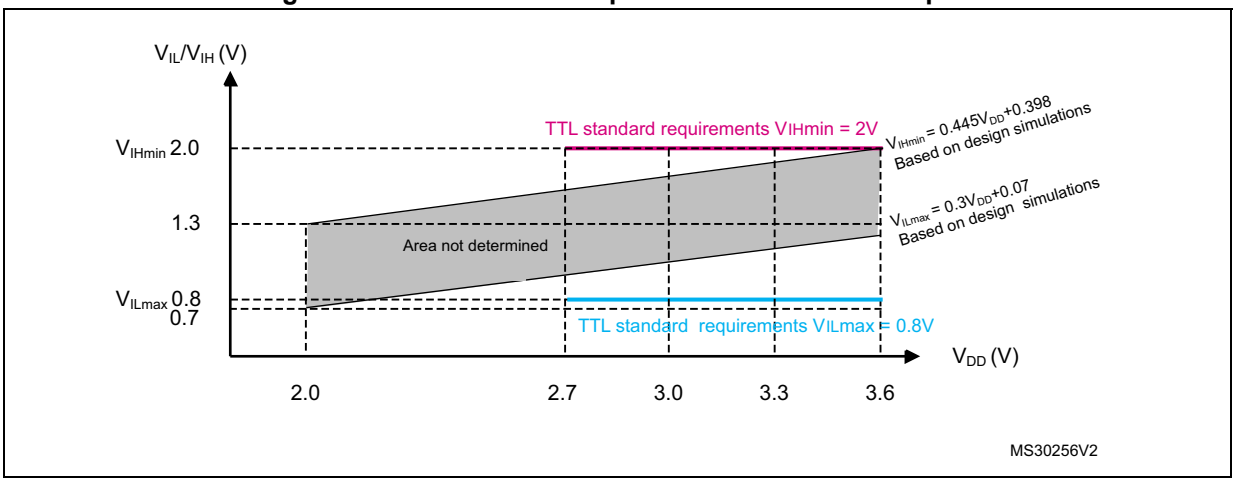


Figure 22. 5V- tolerant (FT and FTf) I/O input characteristics - CMOS port

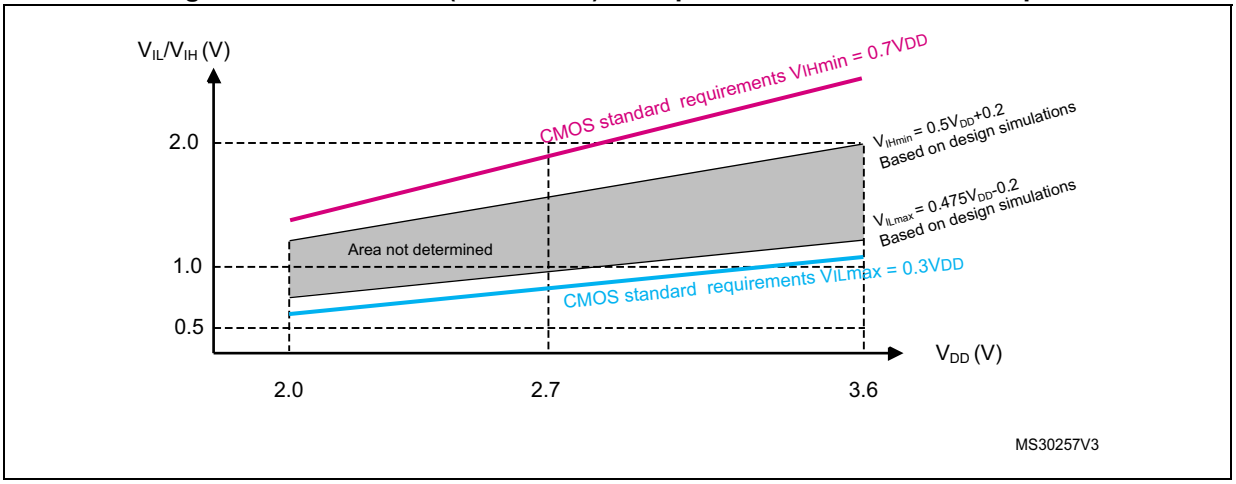
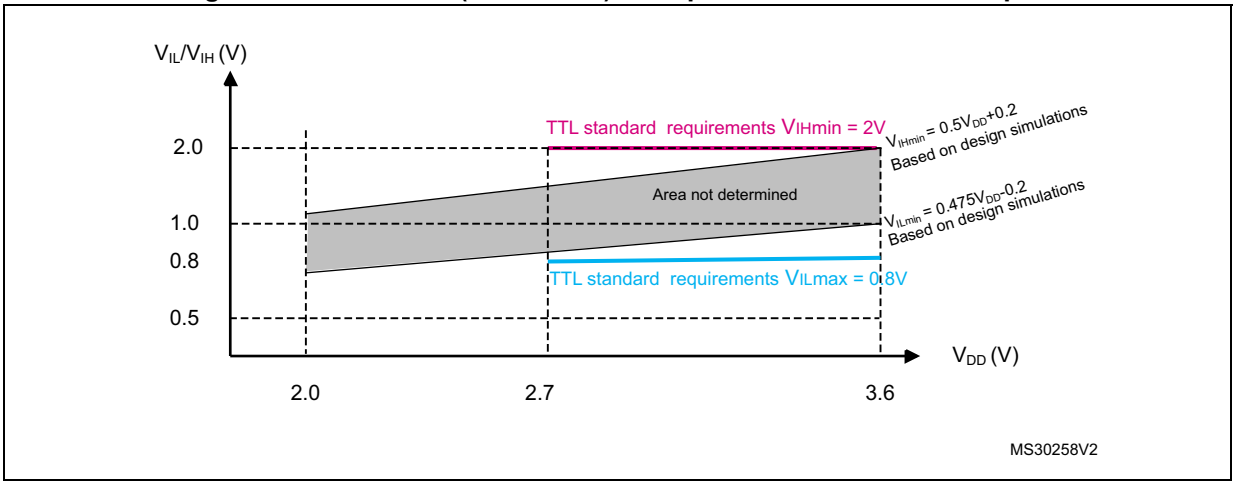


Figure 23. 5V-tolerant (FT and FTf) I/O input characteristics - TTL port



Output driving current

The GPIOs (general-purpose input/output) can sink or source up to +/-8 mA, and sink or source up to +/- 20 mA (with a relaxed V_{OL}/V_{OH}).

In the user application, the number of I/O pins which can drive current must be limited to respect the absolute maximum rating specified in *Section 6.2*:

- The sum of the currents sourced by all the I/Os on $V_{DD,}$ plus the maximum Run consumption of the MCU sourced on $V_{DD,}$ cannot exceed the absolute maximum rating ΣI_{VDD} (see *Table 17*).
- The sum of the currents sunk by all the I/Os on V_{SS} plus the maximum Run consumption of the MCU sunk on V_{SS} cannot exceed the absolute maximum rating ΣI_{VSS} (see *Table 17*).

Output voltage levels

Unless otherwise specified, the parameters given in *Table 47: ESD absolute maximum ratings* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 19*. All I/Os (FT, TTa and TC unless otherwise specified) are CMOS and TTL compliant.

Table 51. Output voltage characteristics

Symbol	Parameter	Conditions	Min.	Max.	Unit
V_{OL}(1)	Low-level output voltage for an I/O pin	CMOS port(2) I_{IO} = +8 mA 2.7 V < V_{DD} < 3.6 V	-	0.4	V
V_{OH}(3)	High- level output voltage for an I/O pin		V_{DD}–0.4	-	
V_{OL} (1)	Low-level output voltage for an I/O pin	TTL port(2) I_{IO} = +8 mA 2.7 V < V_{DD} < 3.6 V	-	0.4	
V_{OH} (3)	High-level output voltage for an I/O pin		2.4	-	
V_{OL}(1)(4)	Low-level output voltage for an I/O pin	I_{IO} = +20 mA 2.7 V < V_{DD} < 3.6 V	-	1.3	
V_{OH}(3)(4)	High-level output voltage for an I/O pin		V_{DD}–1.3	-	
V_{OL}(1)(4)	Low-level output voltage for an I/O pin	I_{IO} = +6 mA 2 V < V_{DD} < 2.7 V	-	0.4	
V_{OH}(3)(4)	High-level output voltage for an I/O pin		V_{DD}–0.4	-	
V_{OLFM+}(1)(4)	Low-level output voltage for an FTf I/O pin in FM+ mode	I_{IO} = +20 mA 2.7 V < V_{DD} < 3.6 V	-	0.4	

1. The I_{IO} current sunk by the device must always respect the absolute maximum rating specified in *Table 17* and the sum of I_{IO} (I/O ports and control pins) must not exceed $\Sigma I_{IO(PIN)}$.
2. TTL and CMOS outputs are compatible with JEDEC standards JESD36 and JESD52.
3. The I_{IO} current sourced by the device must always respect the absolute maximum rating specified in *Table 17* and the sum of I_{IO} (I/O ports and control pins) must not exceed $\Sigma I_{IO(PIN)}$.
4. Data based on design simulation.

Input/output AC characteristics

The definition and values of input/output AC characteristics are given in *Figure 24* and

Table 66, respectively.

Unless otherwise specified, the parameters given are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 19*.

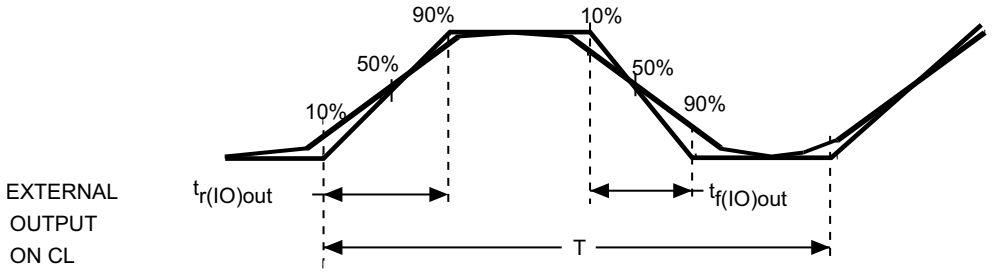
Table 52. I/O AC characteristics(1)

OSPEEDRy [1:0] value(1)	Symbol	Parameter	Conditions	Min.	Max.	Unit
x0	$f_{max(IO)out}$	Maximum frequency(2)	C_L = 50 pF, V_{DD} = 2 V to 3.6 V	-	2(3)	MHz
	$t_{f(IO)out}$	Output high to low level fall time	C_L = 50 pF, V_{DD} = 2 V to 3.6 V	-	125(3)	ns
	$t_{r(IO)out}$	Output low to high level rise time		-	125(3)	
01	$f_{max(IO)out}$	Maximum frequency(2)	C_L = 50 pF, V_{DD} = 2 V to 3.6 V	-	10(3)	MHz
	$t_{f(IO)out}$	Output high to low level fall time	C_L = 50 pF, V_{DD} = 2 V to 3.6 V	-	25 (3)	ns
	$t_{r(IO)out}$	Output low to high level rise time		-	25 (3)	
11	$f_{max(IO)out}$	Maximum frequency(2)	C_L = 30 pF, V_{DD} = 2.7 V to 3.6 V	-	50(3)	MHz
			C_L = 50 pF, V_{DD} = 2.7 V to 3.6 V	-	30(3)	MHz
			C_L = 50 pF, V_{DD} = 2 V to 2.7 V	-	20(3)	MHz
	$t_{f(IO)out}$	Output high to low level fall time	C_L = 30 pF, V_{DD} = 2.7 V to 3.6 V	-	5(3)	ns
			C_L = 50 pF, V_{DD} = 2.7 V to 3.6 V	-	8(3)	
			C_L = 50 pF, V_{DD} = 2 V to 2.7 V	-	12(3)	
	$t_{r(IO)out}$	Output low to high level rise time	C_L = 30 pF, V_{DD} = 2.7 V to 3.6 V	-	5(3)	
			C_L = 50 pF, V_{DD} = 2.7 V to 3.6 V	-	8(3)	
			C_L = 50 pF, V_{DD} = 2 V to 2.7 V	-	12(3)	
FM+ configuration(4)	$f_{max(IO)out}$	Maximum frequency(2)	C_L = 50 pF, V_{DD} = 2 V to 3.6 V	-	2(4)	MHz
	$t_{f(IO)out}$	Output high to low level fall time		-	12(4)	ns
	$t_{r(IO)out}$	Output low to high level rise time		-	34(4)	
-	t_{EXTIpw}	Pulse width of external signals detected by the EXTI controller	-	10	-	ns

1. The I/O speed is configured using the OSPEEDRx[1:0] bits. Refer to the RM0364 reference manual for a description of GPIO Port configuration register.
2. The maximum frequency is defined in *Figure 24*.
3. Guaranteed by design, not tested in production.

4. The I/O speed configuration is bypassed in FM+ I/O mode. Refer to the RM0364 reference manual for a description of FM+ I/O mode configuration.

Figure 24. I/O AC characteristics definition



Maximum frequency is achieved if ($t_r + t_f$) ≤ (2/3)T and if the duty cycle is (45-55%) when loaded by CL specified in the table " *I/O AC characteristics*".

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6.3.15 NRST pin characteristics

The NRST pin input driver uses CMOS technology. It is connected to a permanent pull-up resistor, R_{PU} (see *Table 50*).

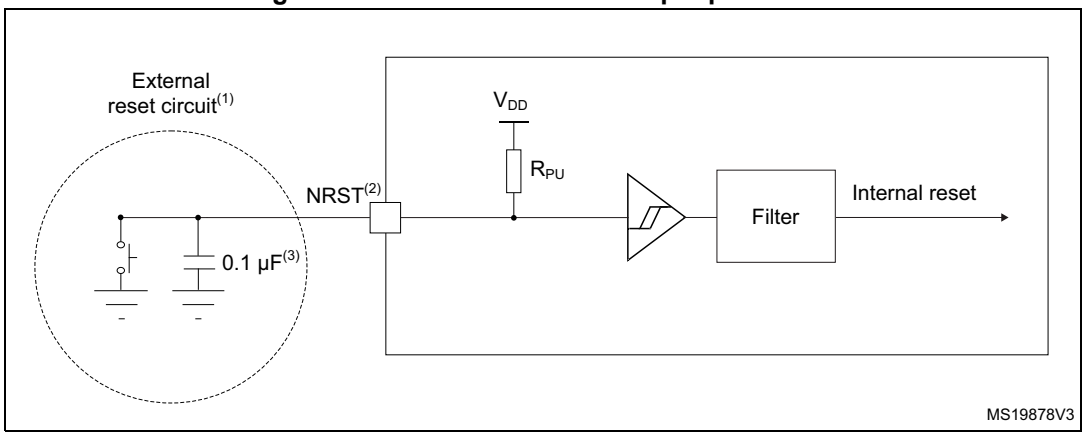
Unless otherwise specified, the parameters given in *Table 53* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 19*.

Table 53. NRST pin characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
$V_{IL(NRST)}$(1)	NRST Input low level voltage	-	-	-	$0.3V_{DD}$ + 0.07(1)	V
$V_{IH(NRST)}$(1)	NRST Input high-level voltage	-	$0.445V_{DD}$ + 0.398(1)	-	-	
$V_{hys(NRST)}$	NRST Schmitt trigger voltage hysteresis	-	-	200	-	mV
R_{PU}	Weak pull-up equivalent resistor(2)	$V_{IN} = V_{SS}$	25	40	55	kΩ
$V_{F(NRST)}$(1)	NRST Input filtered pulse	-	-	-	100(1)	ns
$V_{NF(NRST)}$(1)	NRST Input not filtered pulse	-	500(1)	-	-	ns

1. Guaranteed by design, not tested in production.
2. The pull-up is designed with a true resistance in series with a switchable PMOS. This PMOS contribution to the series resistance must be minimum (~10% order).

Figure 25. Recommended NRST pin protection



1. The reset network protects the device against parasitic resets.
2. The user must ensure that the level on the NRST pin can go below the $V_{IL(NRST)}$ max level specified in *Table 53*. Otherwise the reset is not be taken into account by the device.
3. The external capacitor on NRST must be placed as close as possible to the device.
4. Place the external capacitor 0.1u F on NRST as close as possible to the chip.

6.3.16 High-resolution timer (HRTIM)

The parameters given in *Table 54* are derived from tests performed under ambient temperature and supply voltage conditions summarized in *Table 19*.

Table 54. HRTIM1 characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
T_A	Timer ambient temperature range	f_{HRTIM}=144MHz (1)	-40	-	105	°C
		f_{HRTIM}=128MHz (2)	-10	-	105	°C
f_{HRTIM}	HRTIM input clock for DLL calibration	As per T_A conditions	128	-	144	MHz
t_{HRTIM}			6.9	-	7.8	ns
$t_{RES(HRTIM)}$	Timer resolution time	f_{HRTIM}=144MHz (1), TA from -40 to 105°C	-	217	-	ps
		f_{HRTIM}=128MHz (2),TA from -10 to 105°C	-	244	-	ps
Res_{HRTIM}	Timer resolution	-	-	-	16	bit
t_{DTG}	Dead time generator clock period	-	0.125	-	16	t_{HRTIM}
		f_{HRTIM}=144MHz (1)	0.868	-	111.10	ns
$\lvert t_{DTR}\rvert$ / $\lvert t_{DTF}\rvert$ max	Dead time range (absolute value)	-	-	-	511	t_{DTG}
		f_{HRTIM}=144MHz (1)	-	-	56.77	µs
f_{CHPFRQ}	Chopper stage clock frequency	-	1/256	-	1/16	f_{HRTIM}
		f_{HRTIM}=144MHz (1)	0.562	-	9	MHz
t_{1STPW}	Chopper first pulse length	-	16	-	256	t_{HRTIM}
		f_{HRTIM}=144MHz (1)	0.111	-	1.77	µs

1. Using HSE with 8MHz XTAL as clock source, configuring PLL to get PLLCLK=144MHz, and selecting PLLCLKx2 as HRTIM clock source. (Refer to Reset and clock control section in RM0364.)
2. Using HSI (internal 8MHz RC oscillator), configuring PLL to get PLLCLK=128MHz, and selecting PLLCLKx2 as HRTIM clock source. (Refer to Reset and clock control section in RM0364.

Table 55. HRTIM output response to fault protection(1)

Symbol	Parameter	Conditions	Min.	Typ.	Max.(2)	Unit
$t_{LAT(DF)}$	Digital fault response latency	Propagation delay from HRTIM1_FLTx digital input to HRTIM_CHxy output pin	-	12	25	ns
$t_{W(FLT)}$	Minimum Fault pulse width	-	12.5	-	-	
$t_{LAT(AF)}$	Analog fault response latency	Propagation delay from comparator COMPx_INP input pin to HRTIM_CHxy output pin	-	25	43	

1. Refer to Fault paragraph in HRTIM section of RM0364.
2. Data based on characterization results, not tested in production.

Table 56. HRTIM output response to external events 1 to 5 (Low-Latency mode(1))

Symbol	Parameter	Conditions	Min.	Typ.	Max.(2)	Unit
$t_{LAT(DEEV)}$	Digital external event response latency	Propagation delay from HRTIM1_EEVx digital input to HRTIM_CHxy output pin (30pF load)	-	12	25	ns
$t_{W(FLT)}$	Minimum external event pulse width	-	12.5	-	-	ns
$t_{LAT(AEEV)}$	Analog external event response latency	Propagation delay from comparator COMPx_INP input pin to HRTIM_CHxy output pin (30pF load)	-	25	43	ns
$T_{JIT(EEV)}$	External event response jitter	Jitter of the delay from HRTIM1_EEVx digital input or COMPx_INP input pin to HRTIM_CHxy output pin	-	-	0	t_{HRTIM}(3)
$T_{JIT(PW)}$	Jitter on output pulse width in response to an external event	-	-	-	1	t_{HRTIM}(3)

1. EExFAST bit in HRTIM_EECR1 register is set (Low Latency mode). This functionality is available on external events channels 1 to 5. Refer to Latency to external events paragraph in HRTIM section of RM0364.
2. Data based on characterization results, not tested in production.
3. T_{HRTIM} = 1 / f_{HRTIM} with f_{HRTIM}= 144 MHz or f_{HRTIM} = 128 MHZ depending on the clock controller configuration. (Refer to Reset and clock control section in RM0364.)

Table 57. HRTIM output response to external events 1 to 10 (Synchronous mode (1))

Symbol	Parameter	Conditions	Min.	Typ.	Max.(2)	Unit
$T_{PROP(HRTIM)}$	External event response latency in HRTIM	HRTIM internal propagation delay (3)	6	-	7	t_{HRTIM}
$t_{LAT(DEEV)}$	Digital external event response latency	Propagation delay from HRTIM1_EEVx digital input to HRTIM_CHxy output pin (30pF load) (4)	-	61	72	ns

Table 57. HRTIM output response to external events 1 to 10 (Synchronous mode [1]) (continued)

Symbol	Parameter	Conditions	Min.	Typ.	Max.[2]	Unit
$t_{LAT(AEEV)}$	Analog external event response latency	Propagation delay from COMPx_INP input pin to HRTIM_CHxy output pin (30pF load) [4]	-	81	94	ns
$t_{W(FLT)}$	Minimum external event pulse width	-	12.5	-	-	ns
$T_{JIT(EEV)}$	External event response jitter	Jitter of the delay from HRTIM1_EEVx digital input or COMPx_INP to HRTIM_CHxy output pin	-	-	1	t_{HRTIM} [5]
$T_{JIT(PW)}$	Jitter on output pulse width in response to an external event	-	-	-	0	t_{HRTIM} [5]

1. EExFAST bit in HRTIM_EECR1 or HRTIM_EECR2 register is cleared (synchronous mode). External event filtering is disabled, i.e. EExF[3:0]=0000 in HRTIM_EECR2 register. Refer to Latency to external events paragraph in HRTIM section of RM0364.
2. Data based on characterization results, not tested in production.
3. This parameter does not take into account latency introduced by GPIO or comparator. Refer to DEERL or SACRL parameter for complete latency.
4. This parameter is given for f_{HRTIM} = 144 MHz.
5. T_{HRTIM} = 1 / f_{HRTIM} with f_{HRTIM}= 144 MHz or f_{HRTIM} = 128 MHZ depending on the clock controller configuration. (Refer to Reset and clock control section in RM0364.)

Table 58. HRTIM synchronization input / output[1]

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
$t_{W(SYNCIN)}$	Minimum pulse width on SYNCIN inputs, including HRTIM1_SCIN	-	2	-	-	t_{HRTIM}
$t_{LAT(DF)}$	Response time to external synchronization request	-	-	-	1	t_{HRTIM}
$t_{LAT(AF)}$	Pulse width on HRTIM1_SCOUT output	-	-	16	-	t_{HRTIM}
		f_{HRTIM}=144 MHz	-	111.1	-	ns

1. Guaranteed by design, not tested in production.

6.3.17 Timer characteristics

The parameters given in *Table 59* are guaranteed by design.

Refer to *Section 6.3.14: I/O port characteristics* for details on the input/output alternate function characteristics (output compare, input capture, external clock, PWM output).

Table 59. TIMx(1)(2) characteristics

Symbol	Parameter	Conditions	Min.	Max.	Unit
$t_{res(TIM)}$	Timer resolution time	-	1	-	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 72 MHz	13.9	-	ns
		$f_{TIM1CLK}$ = 144 MHz	6.95	-	ns
f_{EXT}	Timer external clock frequency on CH1 to CH4	-	0	$f_{TIMxCLK}/2$	MHz
		$f_{TIMxCLK}$ = 72 MHz	0	36	MHz
Res_{TIM}	Timer resolution	TIMx (except TIM2)	-	16	bit
		TIM2	-	32	
$t_{COUNTER}$	16-bit counter clock period	-	1	65536	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 72 MHz	0.0139	910	µs
		$f_{TIM1CLK}$ = 144 MHz	0.0069	455	µs
t_{MAX_COUNT}	Maximum possible count with 32-bit counter	-	-	65536 × 65536	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 72 MHz	-	59.65	s
		$f_{TIM1CLK}$ = 144 MHz	-	29.825	s

1. TIMx is used as a general term to refer to the TIM1, TIM2, TIM3, TIM15, TIM16 and TIM17 timers.
2. Guaranteed by design, not tested in production.

Table 60. IWDG min./max. timeout period at 40 kHz (LSI) (1)

Prescaler divider	PR[2:0] bits	Min. timeout (ms) RL[11:0] = 0x000	Max. timeout (ms) RL[11:0] = 0xFFF
/4	0	0.1	409.6
/8	1	0.2	819.2
/16	2	0.4	1638.4
/32	3	0.8	3276.8
/64	4	1.6	6553.6
/128	5	3.2	13107.2
/256	7	6.4	26214.4

1. These timings are given for a 40 kHz clock but the microcontroller's internal RC frequency can vary from 30 to 60 kHz. Moreover, given an exact RC oscillator frequency, the exact timings still depend on the phasing of the APB interface clock versus the LSI clock so that there is always a full RC period of uncertainty.

Table 61. WWDG min./max. timeout value at 72 MHz (PCLK)(1)

Prescaler	WDGTB	Min. timeout value	Max. timeout value
1	0	0.05687	3.6409
2	1	0.1137	7.2817
4	2	0.2275	14.564
8	3	0.4551	29.127

1. Guaranteed by design, not tested in production.

6.3.18 Communication interfaces

I²C interface characteristics

The I²C interface meets the timings requirements of the I²C-bus specification and user manual rev. 03 for:

- Standard-mode (Sm): with a bit rate up to 100 Kbit/s
- Fast-mode (Fm): with a bit rate up to 400 Kbit/s
- Fast-mode Plus (Fm+): with a bit rate up to 1 Mbit/s.

The I²C timings requirements are guaranteed by design when the I²C peripheral is properly configured (refer to Reference manual).

The SDA and SCL I/O requirements are met with the following restrictions: the SDA and SCL I/O pins are not "true" open-drain. When configured as open-drain, the PMOS connected between the I/O pin and VDD is disabled, but is still present. Only FTf I/O pins support Fm+ low-level output current maximum requirement. Refer to *Section 6.3.14: I/O port characteristics* for the I²C I/O characteristics.

All I²C SDA and SCL I/Os embed an analog filter. Refer to the table below for the analog filter characteristics:

Table 62. I²C analog filter characteristics(1)

Symbol	Parameter	Min.	Max.	Unit
t_{AF}	Maximum pulse width of spikes that are suppressed by the analog filter.	50(2)	260(3)	ns

1. Guaranteed by design, not tested in production.
2. Spikes with width below t_{AF}(min.) are filtered.
3. Spikes with width above t_{AF}(max.) are not filtered.

SPI characteristics

Unless otherwise specified, the parameters given in *Table 53* for SPI are derived from tests performed under ambient temperature, f_{PCLKx} frequency and V_{DD} supply voltage conditions summarized in *Table 19: General operating conditions*.

Refer to *Section 6.3.14: I/O port characteristics* for more details on the input/output alternate function characteristics (NSS, SCK, MOSI, MISO for SPI).

Table 63. SPI characteristics(1)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
f_{SCK} $1/t_{c(SCK)}$	SPI clock frequency	Master mode 2.7 < V_{DD} < 3.6 V	-	-	24	MHz
		Master mode 2 < V_{DD} < 3.6 V			18	
		Slave mode 2 < V_{DD} < 3.6 V			24	
		Slave mode transmitter/full duplex 2 < V_{DD} < 3.6 V			18(2)	
DuCy(SCK)	Duty cycle of SPI clock frequency	Slave mode	30	50	70	%
$t_{su(NSS)}$	NSS setup time	Slave mode, SPI presc = 2	4*Tpclk	-	-	ns
$t_{h(NSS)}$	NSS hold time	Slave mode, SPI presc = 2	2*Tpclk	-	-	
$t_{w(SCKH)}$ $t_{w(SCKL)}$	SCK high and low time	Master mode	Tpclk-2	Tpclk	Tpclk+2	
$t_{su(MI)}$	Data input setup time	Master mode	0	-	-	
$t_{su(SI)}$		Slave mode	3	-	-	
$t_{h(MI)}$	Data input hold time	Master mode	5	-	-	
$t_{h(SI)}$		Slave mode	1	-	-	
$t_{a(SO)}$	Data output access time	Slave mode	10	-	40	
$t_{dis(SO)}$	Data output disable time	Slave mode	10	-	17	
$t_{v(SO)}$	Data output valid time	Slave mode 2.7 < V_{DD} < 3.6 V	-	12	20	
		Slave mode 2 < V_{DD} < 3.6 V	-	12	27.5	
$t_{v(MO)}$		Master mode	-	1.5	5	
$t_{h(SO)}$	Data output hold time	Slave mode	7.5	-	-	
$t_{h(MO)}$		Master mode	0	-	-	

1. Data based on characterization results, not tested in production.
2. Maximum frequency in Slave transmitter mode is determined by the sum of tv(SO) and tsu(MI) which has to fit into SCK low or high phase preceding the SCK sampling edge. This value can be achieved when the SPI communicates with a master having tsu(MI) = 0 while Duty(SCK) = 50%.

Figure 26. SPI timing diagram - slave mode and CPHA = 0

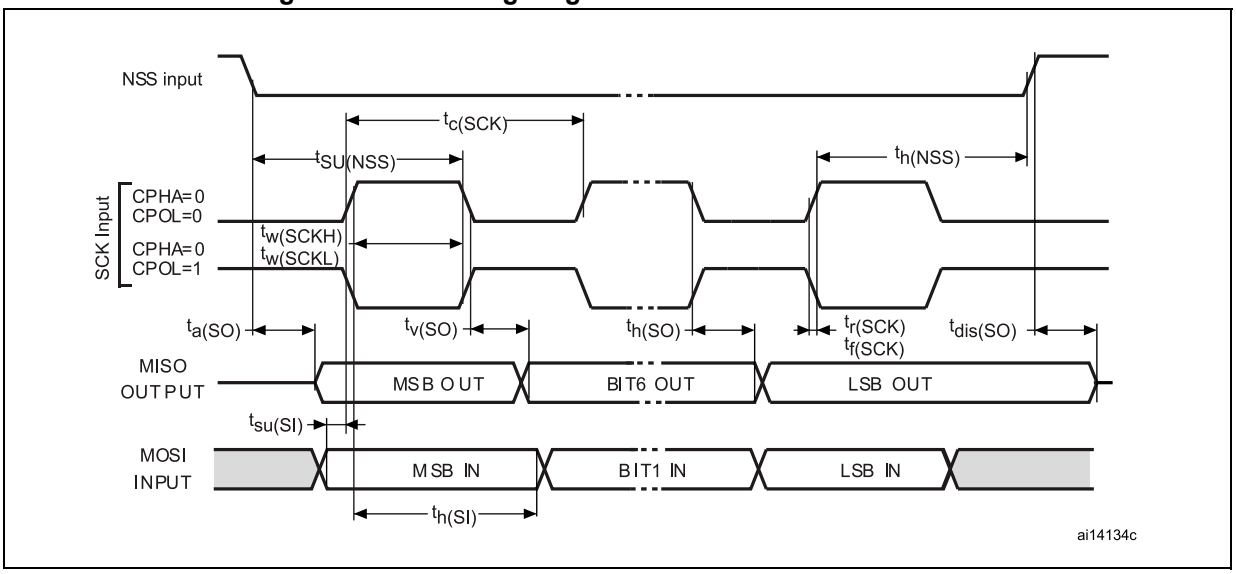
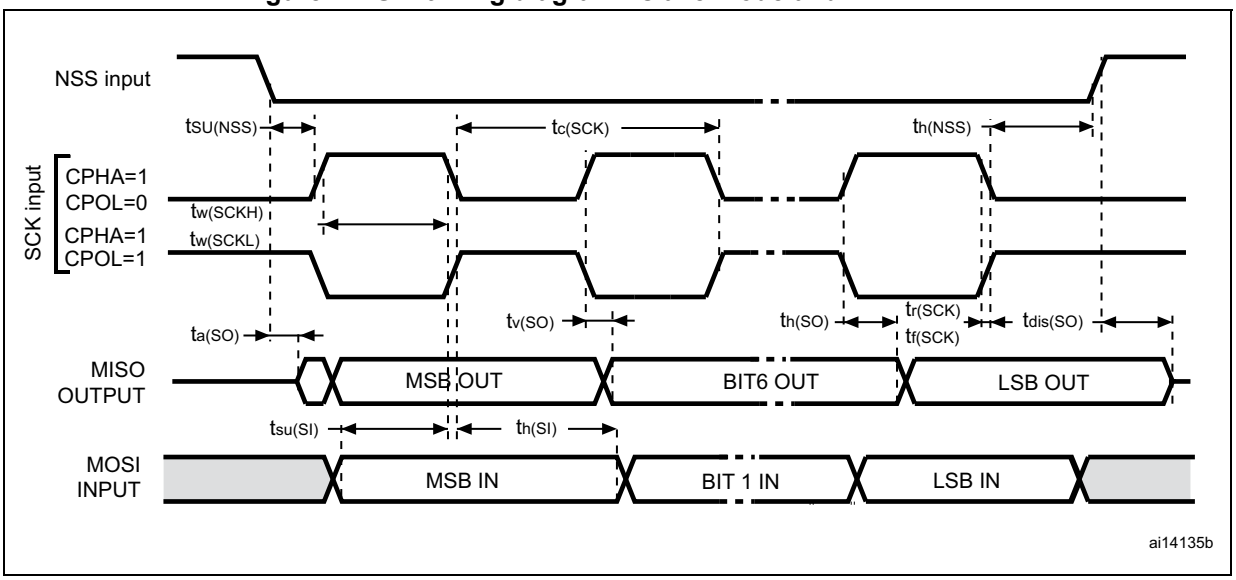
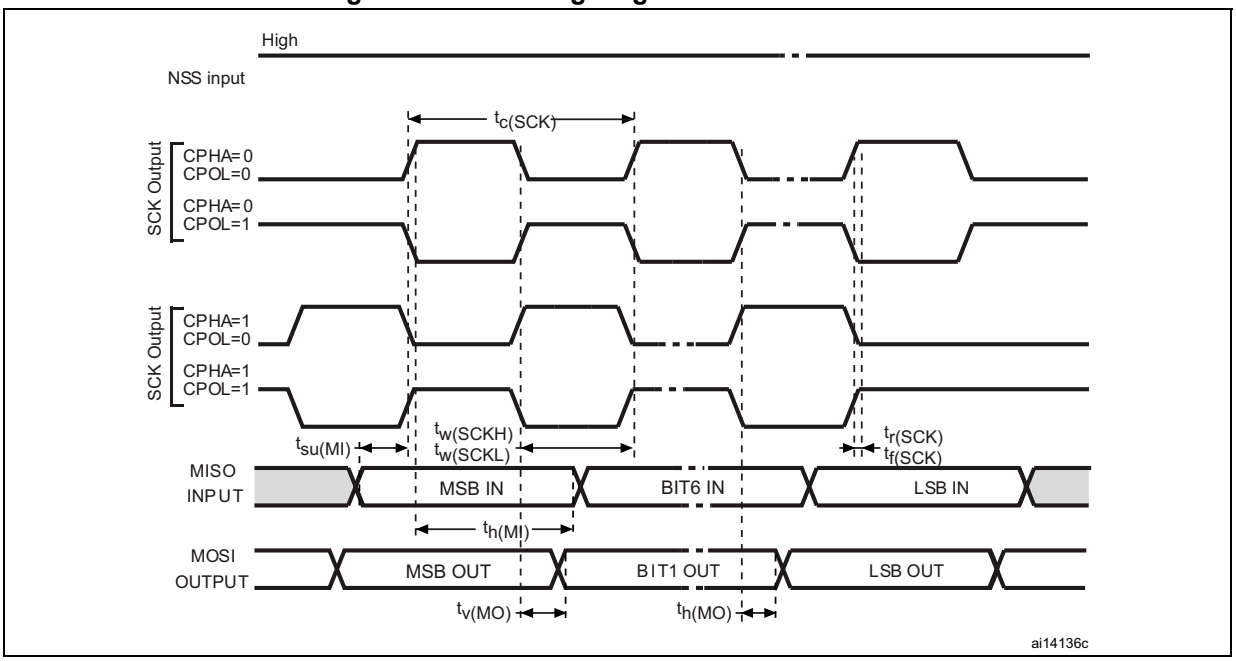


Figure 27. SPI timing diagram - slave mode and CPHA = 1(1)



1. Measurement points are done at $0.5V_{DD}$ and with external C_L = 30 pF.

Figure 28. SPI timing diagram - master mode(1)



1. Measurement points are done at $0.5V_{DD}$ and with external C_L = 30 pF.

CAN (controller area network) interface

Refer to *Section 6.3.14: I/O port characteristics* for more details on the input/output alternate function characteristics (CAN_TX and CAN_RX).

6.3.19 ADC characteristics

Unless otherwise specified, the parameters showed from *Table 64* to *Table 67* are guaranteed by design, with the conditions summarized in *Table 19*.

Table 64. ADC characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{DDA}	Analog supply voltage for ADC	-	2	-	3.6	V
I_{DDA}	ADC current consumption (*Figure 29*)	Single ended mode, 5 MSPS	-	1011.3	1172.0	µA
		Single ended mode, 1 MSPS	-	214.7	322.3	
		Single ended mode, 200 KSPS	-	54.7	81.1	
		Differential mode, 5 MSPS	-	1061.5	1243.6	
		Differential mode, 1 MSPS	-	246.6	337.6	
		Differential mode, 200 KSPS	-	56.4	83.0	
V_{REF-}	Negative reference voltage	-	-	0	-	V

Table 64. ADC characteristics (continued)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
f_{ADC}	ADC clock frequency	-	0.14	-	72	MHz
f_S(1)	Sampling rate	Resolution = 12 bits, Fast Channel	0.01	-	5.14	Msps
		Resolution = 10 bits, Fast Channel	0.012	-	6	
		Resolution = 8 bits, Fast Channel	0.014	-	7.2	
		Resolution = 6 bits, Fast Channel	0.0175	-	9	
f_{TRIG}(1)	External trigger frequency	f_{ADC} = 72 MHz Resolution = 12 bits	-	-	5.14	MHz
		Resolution = 12 bits	-	-	14	$1/f_{ADC}$
V_{AIN}	Conversion voltage range	-	0	-	V_{DDA}	V
R_{AIN}(1)	External input impedance	-	-	-	100	κΩ
C_{ADC}(1)	Internal sample and hold capacitor	-	-	5	-	pF
t_{CAL}(1)	Calibration time	f_{ADC} = 72 MHz	1.56			µs
		-	112			$1/f_{ADC}$
t_{latr}(1)	Trigger conversion latency Regular and injected channels without conversion abort	CKMODE = 00	1.5	2	2.5	$1/f_{ADC}$
		CKMODE = 01	-	-	2	$1/f_{ADC}$
		CKMODE = 10	-	-	2.25	$1/f_{ADC}$
		CKMODE = 11	-	-	2.125	$1/f_{ADC}$
$t_{latrinj}$(1)	Trigger conversion latency Injected channels aborting a regular conversion	CKMODE = 00	2.5	3	3.5	$1/f_{ADC}$
		CKMODE = 01	-	-	3	$1/f_{ADC}$
		CKMODE = 10	-	-	3.25	$1/f_{ADC}$
		CKMODE = 11	-	-	3.125	$1/f_{ADC}$
t_S(1)	Sampling time	f_{ADC} = 72 MHz	0.021	-	8.35	µs
		-	1.5	-	601.5	$1/f_{ADC}$
$t_{ADCVREG_STUP}$(1)	ADC Voltage Regulator Start-up time	-	-	-	10	µs
t_{STAB}	Power-up time	-	1			conversion cycle

Table 64. ADC characteristics (continued)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
t_{CONV}(1)	Total conversion time (including sampling time)	f_{ADC} = 72 MHz Resolution = 12 bits	0.19	-	8.52	µs
		Resolution = 12 bits	14 to 614 (t_S for sampling + 12.5 for successive approximation)			$1/f_{ADC}$
CMIR	Common Mode Input signal	ADC differential mode	(V_{SSA}+V_{REF}+)/2-0.18	(V_{SSA} + V_{REF}+)/2	(V_{SSA} + V_{REF}+)/2 + 0.18	V

1. Data guaranteed by design, not tested in production.

Figure 29. ADC typical current consumption in single-ended and differential modes

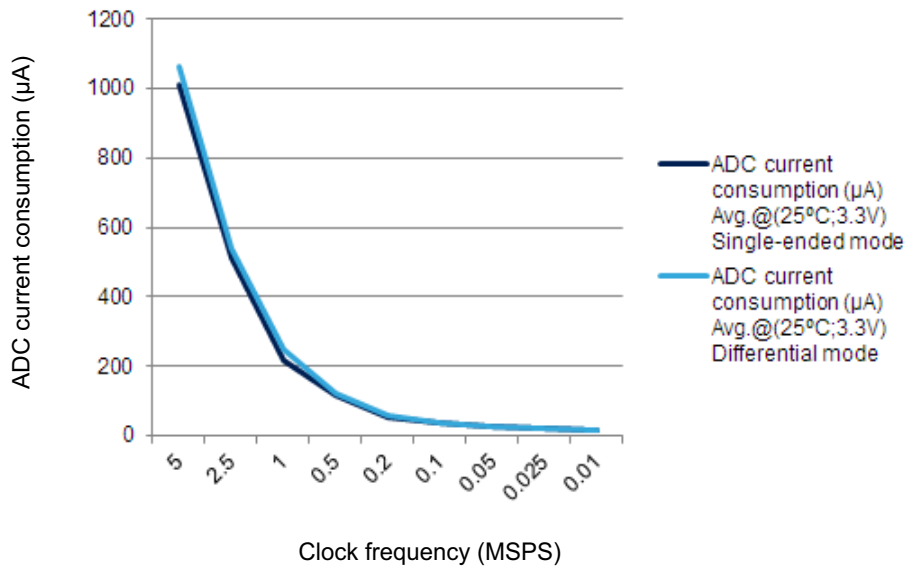


Table 65. Maximum ADC R_{AIN}(1)

Resolution	Sampling cycle @ 72 MHz	Sampling time [ns] @ 72 MHz	R_{AIN} max. (kΩ)		
			Fast channels(2)	Slow channels	Other channels(3)
12 bits	1.5	20.83	0.018	NA	NA
	2.5	34.72	0.150	NA	0.022
	4.5	62.50	0.470	0.220	0.180
	7.5	104.17	0.820	0.560	0.470
	19.5	270.83	2.70	1.80	1.50
	61.5	854.17	8.20	6.80	4.70
	181.5	2520.83	22.0	18.0	15.0
	601.5	8354.17	82.0	68.0	47.0

Table 65. Maximum ADC R_{AIN}(1) (continued)

Resolution	Sampling cycle @ 72 MHz	Sampling time [ns] @ 72 MHz	R_{AIN} max. (kΩ)		
			Fast channels(2)	Slow channels	Other channels(3)
10 bits	1.5	20.83	0.082	NA	NA
	2.5	34.72	0.270	0.082	0.100
	4.5	62.50	0.560	0.390	0.330
	7.5	104.17	1.20	0.82	0.68
	19.5	270.83	3.30	2.70	2.20
	61.5	854.17	10.0	8.2	6.8
	181.5	2520.83	33.0	27.0	22.0
	601.5	8354.17	100.0	82.0	68.0
8 bits	1.5	20.83	0.150	NA	0.039
	2.5	34.72	0.390	0.180	0.180
	4.5	62.50	0.820	0.560	0.470
	7.5	104.17	1.50	1.20	1.00
	19.5	270.83	3.90	3.30	2.70
	61.5	854.17	12.00	12.00	8.20
	181.5	2520.83	39.00	33.00	27.00
	601.5	8354.17	100.00	100.00	82.00
6 bits	1.5	20.83	0.270	0.100	0.150
	2.5	34.72	0.560	0.390	0.330
	4.5	62.50	1.200	0.820	0.820
	7.5	104.17	2.20	1.80	1.50
	19.5	270.83	5.60	4.7	3.90
	61.5	854.17	18.0	15.0	12.0
	181.5	2520.83	56.0	47.0	39.0
	601.5	8354.17	100.00	100.0	100.0

1. Data based on characterization results, not tested in production.
2. All fast channels, expect channel on PA6.
3. Channels available on PA6.

Table 66. ADC accuracy - limited test conditions(1)(2)

Symbol	Parameter	Conditions			Min. (3)	Typ.	Max.(3)	Unit
ET	Total unadjusted error	ADC clock freq. ≤72 MHz Sampling freq. ≤5 Msps V_{DDA} = 3.3 V 25°C	Single ended	Fast channel 5.1 Ms	-	±4	±4.5	LSB
				Slow channel 4.8 Ms	-	±5.5	±6	
			Differential	Fast channel 5.1 Ms	-	±3.5	±4	
				Slow channel 4.8 Ms	-	±3.5	±4	
EO	Offset error		Single ended	Fast channel 5.1 Ms	-	±2	±2	
				Slow channel 4.8 Ms	-	±1.5	±2	
			Differential	Fast channel 5.1 Ms	-	±1.5	±2	
				Slow channel 4.8 Ms	-	±1.5	±2	
EG	Gain error		Single ended	Fast channel 5.1 Ms	-	±3	±4	
				Slow channel 4.8 Ms	-	±5	±5.5	
			Differential	Fast channel 5.1 Ms	-	±3	±3	
				Slow channel 4.8 Ms	-	±3	±3.5	
ED	Differential linearity error		Single ended	Fast channel 5.1 Ms	-	±1	±1	
				Slow channel 4.8 Ms	-	±1	±1	
			Differential	Fast channel 5.1 Ms	-	±1	±1	
				Slow channel 4.8 Ms	-	±1	±1	
EL	Integral linearity error		Single ended	Fast channel 5.1 Ms	-	±1.5	±2	
				Slow channel 4.8 Ms	-	±2	±3	
			Differential	Fast channel 5.1 Ms	-	±1.5	±1.5	
				Slow channel 4.8 Ms	-	±1.5	±2	
ENOB(4)	Effective number of bits		Single ended	Fast channel 5.1 Ms	10.8	10.8	-	bit
				Slow channel 4.8 Ms	10.8	10.8	-	
			Differential	Fast channel 5.1 Ms	11.2	11.3	-	
				Slow channel 4.8 Ms	11.2	11.3	-	
SINAD (4)	Signal-to-noise and distortion ratio		Single ended	Fast channel 5.1 Ms	66	67	-	dB
				Slow channel 4.8 Ms	66	67	-	
			Differential	Fast channel 5.1 Ms	69	70	-	
				Slow channel 4.8 Ms	69	70	-	

Table 66. ADC accuracy - limited test conditions(1)(2) (continued)

Symbol	Parameter	Conditions			Min. (3)	Typ.	Max.(3)	Unit
SNR(4)	Signal-to-noise ratio	ADC clock freq. ≤ 72 MHz Sampling freq. ≤ 5 Msps V_{DDA} = 3.3 V 25°C	Single ended	Fast channel 5.1 Ms	66	67	-	dB
				Slow channel 4.8 Ms	66	67	-	
			Differential	Fast channel 5.1 Ms	69	70	-	
				Slow channel 4.8 Ms	69	70	-	
THD(4)	Total harmonic distortion		Single ended	Fast channel 5.1 Ms	-	-80	-80	
				Slow channel 4.8 Ms	-	-78	-77	
			Differential	Fast channel 5.1 Ms	-	-83	-82	
				Slow channel 4.8 Ms	-	-81	-80	

1. ADC DC accuracy values are measured after internal calibration.
2. ADC accuracy vs. negative Injection Current: Injecting negative current on any analog input pins must be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to analog pins which may potentially inject negative current.
Any positive injection current within the limits specified for $I_{INJ(PIN)}$ and $\Sigma I_{INJ(PIN)}$ in *Section 6.3.14* does not affect the ADC accuracy.
3. Data based on characterization results, not tested in production.
4. Value measured with a -0.5 dB full scale 50 kHz sine wave input signal.

Table 67. ADC accuracy (1)(2)(3)

Symbol	Parameter	Conditions			Min.(4)	Max.(4)	Unit
ET	Total unadjusted error	ADC clock freq. ≤ 72 MHz, Sampling freq. ≤ 5 Msps 2.0 V ≤ V_{DDA} ≤ 3.6 V	Single ended	Fast channel 5.1 Ms	-	±6.5	LSB
				Slow channel 4.8 Ms	-	±6.5	
			Differential	Fast channel 5.1 Ms	-	±4	
				Slow channel 4.8 Ms	-	±4.5	
EO	Offset error		Single ended	Fast channel 5.1 Ms	-	±3	
				Slow channel 4.8 Ms	-	±3	
			Differential	Fast channel 5.1 Ms	-	±2.5	
				Slow channel 4.8 Ms	-	±2.5	
EG	Gain error		Single ended	Fast channel 5.1 Ms	-	±6	
				Slow channel 4.8 Ms	-	±6	
			Differential	Fast channel 5.1 Ms	-	±3.5	
				Slow channel 4.8 Ms	-	±4	
ED	Differential linearity error		Single ended	Fast channel 5.1 Ms	-	±1.5	
				Slow channel 4.8 Ms	-	±1.5	
			Differential	Fast channel 5.1 Ms	-	±1.5	
				Slow channel 4.8 Ms	-	±1.5	

Table 67. ADC accuracy (1)(2)(3) (continued)

Symbol	Parameter	Conditions			Min.(4)	Max.(4)	Unit
EL	Integral linearity error	ADC clock freq. ≤ 72 MHz, Sampling freq. ≤ 5 Msps 2.0 V ≤ V_{DDA} ≤ 3.6 V	Single ended	Fast channel 5.1 Ms	-	±3	LSB
				Slow channel 4.8 Ms	-	±3.5	
			Differential	Fast channel 5.1 Ms	-	±2	
				Slow channel 4.8 Ms	-	±2.5	
ENOB (5)	Effective number of bits		Single ended	Fast channel 5.1 Ms	10.4	-	bits
				Slow channel 4.8 Ms	10.4	-	
			Differential	Fast channel 5.1 Ms	10.8	-	
				Slow channel 4.8 Ms	10.8	-	
SINAD (5)	Signal-to-noise and distortion ratio		Single ended	Fast channel 5.1 Ms	64	-	dB
				Slow channel 4.8 Ms	63	-	
			Differential	Fast channel 5.1 Ms	67	-	
				Slow channel 4.8 Ms	67	-	
SNR(5)	Signal-to-noise ratio	ADC clock freq. ≤ 72 MHz, Sampling freq ≤ 5 Msps, 2.0 V ≤ V_{DDA} ≤ 3.6 V	Single ended	Fast channel 5.1 Ms	64	-	
				Slow channel 4.8 Ms	64	-	
			Differential	Fast channel 5.1 Ms	67	-	
				Slow channel 4.8 Ms	67	-	
THD(5)	Total harmonic distortion		Single ended	Fast channel 5.1 Ms	-	-75	
				Slow channel 4.8 Ms	-	-75	
			Differential	Fast channel 5.1 Ms	-	-79	
				Slow channel 4.8 Ms	-	-78	

1. ADC DC accuracy values are measured after internal calibration.
2. ADC accuracy vs. negative Injection Current: Injecting negative current on any analog input pins must be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to analog pins which may potentially inject negative current.
   Any positive injection current within the limits specified for $I_{INJ(PIN)}$ and $\Sigma I_{INJ(PIN)}$ in *Section 6.3.14* does not affect the ADC accuracy.
3. Better performance may be achieved in restricted V_{DDA}, frequency and temperature ranges.
4. Data based on characterization results, not tested in production.
5. Value measured with a -0.5 dB full scale 50 kHz sine wave input signal.

Table 68. ADC accuracy(1)(2) at 1MSPS

Symbol	Parameter	Test conditions		Typ.	Max(3)	Unit
ET	Total unadjusted error	ADC Freq. ≤ 72 MHz Sampling Freq. ≤ 1MSPS 2.4 V ≤ V_{DDA} = V_{REF+} ≤ 3.6 V Single-ended mode	Fast channel	±2.5	±5	LSB
			Slow channel	±3.5	±5	
EO	Offset error		Fast channel	±1	±2.5	
			Slow channel	±1.5	±2.5	
EG	Gain error		Fast channel	±2	±3	
			Slow channel	±3	±4	
ED	Differential linearity error		Fast channel	±0.7	± 2	
			Slow channel	±0.7	±2	
EL	Integral linearity error		Fast channel	±1	±3	
			Slow channel	±1.2	±3	

1. ADC DC accuracy values are measured after internal calibration.
2. ADC accuracy vs. negative Injection Current: Injecting negative current on any analog input pins must be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to analog pins which may potentially inject negative current. Any positive injection current within the limits specified for IINJ(PIN) and ∑IINJ(PIN) in *Section 6.3.14: I/O port characteristics* does not affect the ADC accuracy.
3. Data based on characterization results, not tested in production.

Figure 30. ADC accuracy characteristics

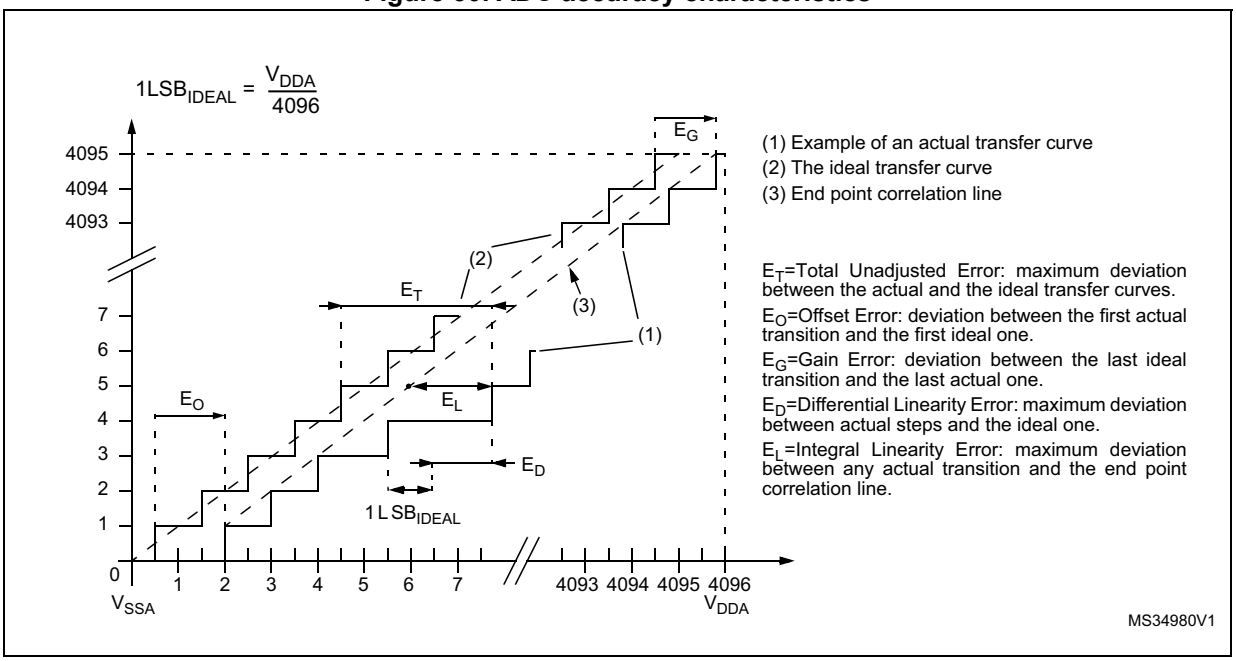
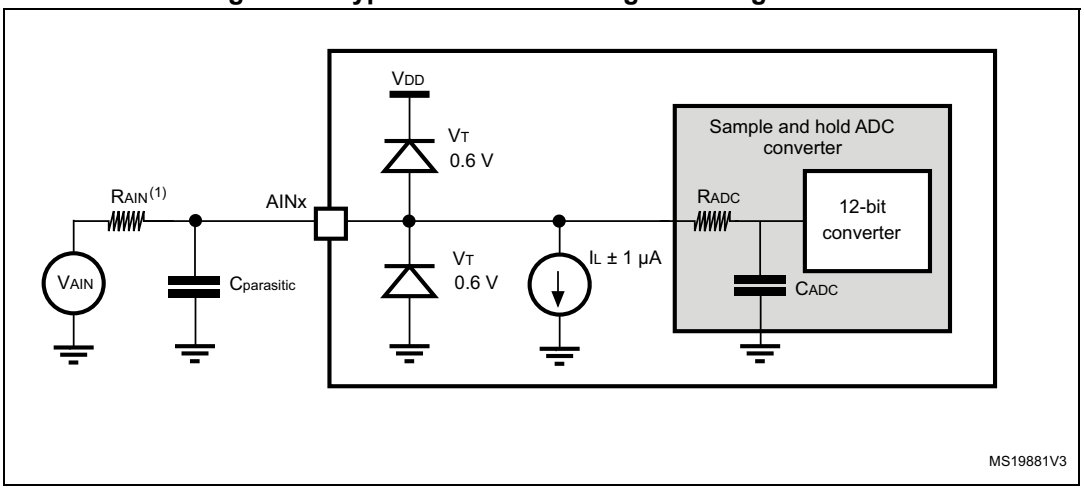


Figure 31. Typical connection diagram using the ADC



1. Refer to *Table 64* for the values of R_{AIN}.
2. $C_{parasitic}$ represents the capacitance of the PCB (dependent on soldering and PCB layout quality) plus the pad capacitance (roughly 7 pF). A high $C_{parasitic}$ value downgrades conversion accuracy. To remedy this, f_{ADC} must be reduced.

General PCB design guidelines

Power supply decoupling must be performed as shown in *Figure 12: Power-supply scheme*. The 10 nF capacitor must be ceramic (good quality) and it must be placed as close as possible to the chip.

6.3.20 DAC electrical specifications

Table 69. DAC characteristics

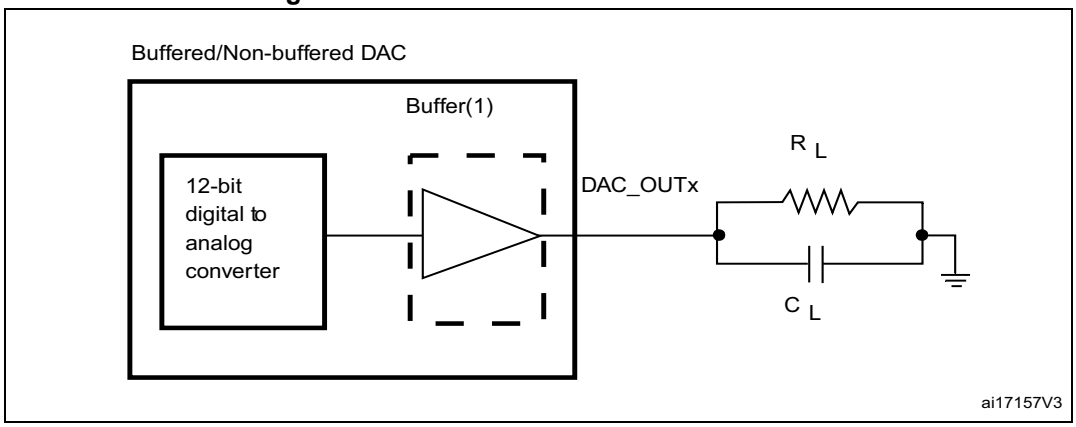
Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{DDA}	Analog supply voltage	-	2.4	-	3.6	V
R_{LOAD}(1)	Resistive load	DAC output buffer ON (to V_{SSA})	5	-		kΩ
		DAC output buffer ON (to V_{DDA})	25			
R_O(1)	Output impedance	DAC output buffer OFF	-	-	15	kΩ
C_{LOAD}(1)	Capacitive load	DAC output buffer ON	-	-	50	pF
V_{DAC_OUT}(1)	Voltage on DAC_OUT output	Corresponds to 12-bit input code (0x0E0) to (0xF1C) at V_{DDA} = 3.6 V and (0x155) and (0xEAB) at V_{DDA} = 2.4 V	0.2	-	V_{DDA} – 0.2	V
		DAC output buffer OFF	-	0.5	-	mV
			-	-	V_{DDA}– 1LSB	V
I_{DDA}(3)	DAC DC current consumption in quiescent mode(2)	With no load, middle code (0x800) on the input	-	-	380	µA
		With no load, worst code (0xF1C) on the input.	-	-	480	µA

Table 69. DAC characteristics (continued)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
DNL(3)	Differential non linearity Difference between two consecutive code-1LSB)	Given for a 10-bit input code DAC1 channel 1	-	-	±0.5	LSB
		Given for a 12-bit input code DAC1 channel 1	-	-	±2	LSB
		Given for a 10-bit input code DAC1 channel 2 & DAC2 channel 1	-	-	-0.75/+0.25	LSB
		Given for a 12-bit input code DAC1 channel 2 & DAC2 channel 1	-	-	-3/+1	LSB
INL(3)	Integral non linearity (difference between measured value at Code i and the value at Code i on a line drawn between Code 0 and last Code 4095)	Given for a 10-bit input code	-	-	±1	LSB
		Given for a 12-bit input code	-	-	±4	LSB
Offset(3)	Offset error (difference between measured value at Code (0x800) and the ideal value = $V_{DDA}/2$)	-	-	-	±10	mV
		Given for a 10-bit input code at V_{DDA} = 3.6 V	-	-	±3	LSB
		Given for a 12-bit input code	-	-	±12	LSB
Gain error(3)	Gain error	Given for a 12-bit input code	-	-	±0.5	%
$t_{SETTLING}$(3)	Settling time (full scale: for a 12-bit input code transition between the lowest and the highest input codes when DAC_OUT reaches final value ±1LSB	$C_{LOAD} \leq 50$ pF, $R_{LOAD} \geq 5$ kΩ	-	3	4	µs
Update rate(3)	Max frequency for a correct DAC_OUT change when small variation in the input code (from code i to i+1LSB)	$C_{LOAD} \leq 50$ pF, $R_{LOAD} \geq 5$ kΩ	-	-	1	MS/s
I_{skink}	Output sink current	DAC buffer ON Output level higher than 0.2 V	100	-	-	µA
t_{WAKEUP}(3)	Wakeup time from off state (Setting the ENx bit in the DAC Control register)	$C_{LOAD} \leq 50$ pF, $R_{LOAD} \geq 5$ kΩ	-	6.5	10	µs
PSRR+ (1)	Power supply rejection ratio (to V_{DDA}) (static DC measurement	No R_{LOAD}, C_{LOAD} = 50 pF	-	–67	–40	dB

1. Guaranteed by design, not tested in production.
2. Quiescent mode refers to the state of the DAC a keeping steady value on the output, so no dynamic consumption is involved.
3. Data based on characterization results, not tested in production.

Figure 32. 12-bit buffered /non-buffered DAC



1. The DAC integrates an output buffer that can be used to reduce the output impedance and to drive external loads directly without the use of an external operational amplifier. The buffer can be bypassed by configuring the BOFFx bit in the DAC_CR register.

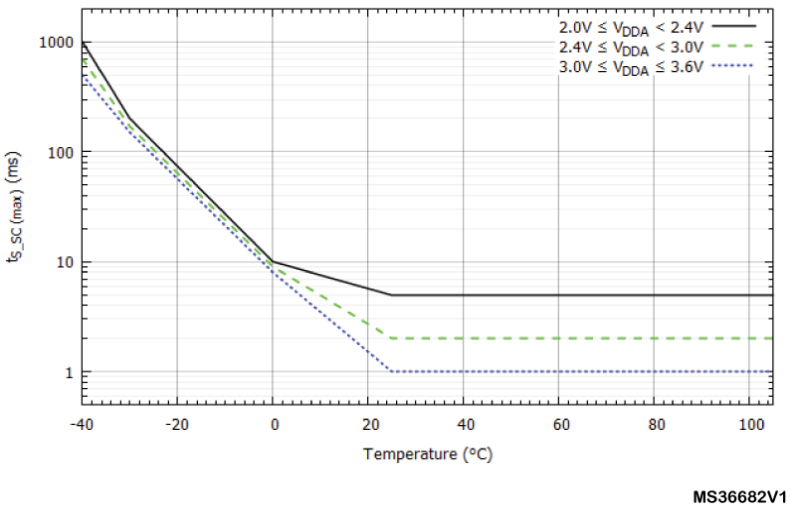
6.3.21 Comparator characteristics

Table 70. Comparator characteristics(1)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{DDA}	Analog supply voltage	-	2	-	3.6	V
V_{IN}	Comparator input voltage range	-	0	-	V_{DDA}	-
V_{BG}	Scaler input voltage	-	-	$V_{REFINIT}$	-	-
V_{SC}	Scaler offset voltage	-	-	±5	±10	mV
t_{S_SC}	V_{REFINT} scaler startup time from power down	First V_{REFINT} scaler activation after device power on	-	-	1(2)	s
		Next activations	-	-	0.2	ms
t_{START}	Comparator startup time	V_{DDA} < 2.7 V	-	-	4	µs
		V_{DDA} < 2.7 V	-	-	10	
t_D	Propagation delay for 200 mV step with 100 mV overdrive	V_{DDA} ≥ 2.7 V	-	25	28	ns
		V_{DDA} < 2.7 V	-	28	30	
	Propagation delay for full range step with 100 mV overdrive	V_{DDA} ≥ 2.7 V	-	32	35	
		V_{DDA} < 2.7 V	-	35	40	
V_{OFFSET}	Comparator offset error	V_{DDA} ≥ 2.7 V	-	±5	±10	mV
		V_{DDA} < 2.7 V	-	-	±25	
TV_{OFFSET}	Total offset variation	Full temperature range	-	-	3	mV
$I_{DD(COMP)}$	COMP current consumption	-	-	400	600	µA

1. Guaranteed by design, not tested in production.
2. For more details and conditions see *Figure 33: Maximum V_{REFINT} scaler startup time from power-down*.

Figure 33. Maximum V_{REFINT} scaler startup time from power-down



6.3.22 Operational amplifier characteristics

Table 71. Operational amplifier characteristics(1)

Symbol	Parameter		Condition	Min.	Typ.	Max.	Unit
V_{DDA}	Analog supply voltage		-	2.4	-	3.6	V
CMIR	Common mode input range		-	0	-	V_{DDA}	V
VI_{OFFSET}	Input offset voltage	Maximum calibration range	25°C, No Load on output.	-	-	4	mV
			All voltage/Temp.	-	-	6	
		After offset calibration	25°C, No Load on output.	-	-	1.6	
			All voltage/Temp.	-	-	3	
ΔVI_{OFFSET}	Input offset voltage drift		-	-	5	-	µV/°C
I_{LOAD}	Drive current		-	-	-	500	µA
IDDOPAMP	Consumption		No load, quiescent mode	-	690	1450	µA
CMRR	Common mode rejection ratio		-	-	90	-	dB
PSRR	Power supply rejection ratio		DC	73	117	-	dB
GBW	Bandwidth		-	-	8.2	-	MHz
SR	Slew rate		-	-	4.7	-	V/µs
R_{LOAD}	Resistive load		-	4	-	-	kΩ
C_{LOAD}	Capacitive load		-	-	-	50	pF

Table 71. Operational amplifier characteristics(1) (continued)

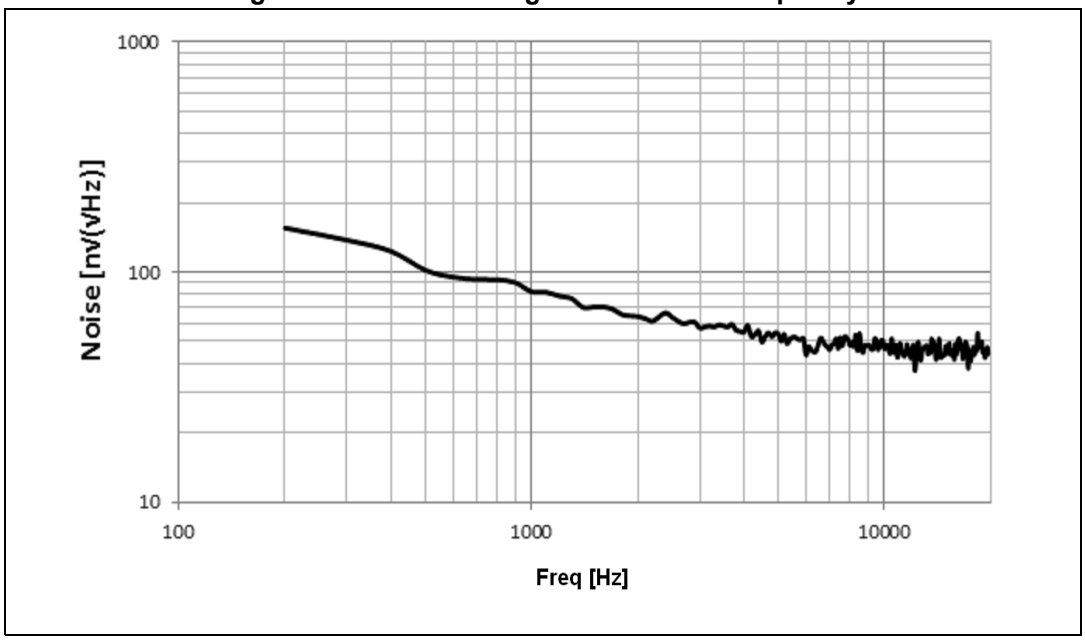
Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
VOH_{SAT}	High saturation voltage(2)	R_{load} = min, Input at V_{DDA}.	V_{DDA}-100	-		mV
		R_{load} = 20K, Input at V_{DDA}.	V_{DDA}-20	-		
VOL_{SAT}	Low saturation voltage	R_{load} = min, input at 0 V	-	-	100	
		R_{load} = 20K, input at 0 V.	-	-	20	
φm	Phase margin	-	-	62	-	°
$t_{OFFTRIM}$	Offset trim time: during calibration, minimum time needed between two steps to have 1 mV accuracy	-	-	-	2	ms
t_{WAKEUP}	Wakeup time from OFF state.	C_{LOAD} ≤50 pf, R_{LOAD} ≥ 4 kΩ, Follower configuration	-	2.8	5	µs
$t_{S_OPAM_VOUT}$	ADC sampling time when reading the OPAMP output		400	-	-	ns
PGA gain	Non inverting gain value	-	-	2	-	-
			-	4	-	-
			-	8	-	-
			-	16	-	-
$R_{network}$	R2/R1 internal resistance values in PGA mode (3)	Gain=2	-	5.4/5.4	-	kΩ
		Gain=4	-	16.2/5.4	-	
		Gain=8	-	37.8/5.4	-	
		Gain=16	-	40.5/2.7	-	
PGA gain error	PGA gain error	-	-1%	-	1%	-
I_{bias}	OPAMP input bias current	-	-	-	±0.2(4)	µA
PGA BW	PGA bandwidth for different non inverting gain	PGA Gain = 2, C_{load} = 50pF, R_{load} = 4 KΩ	-	4	-	MHz
		PGA Gain = 4, C_{load} = 50pF, R_{load} = 4 KΩ	-	2	-	
		PGA Gain = 8, C_{load} = 50pF, R_{load} = 4 KΩ	-	1	-	
		PGA Gain = 16, C_{load} = 50pF, R_{load} = 4 KΩ	-	0.5	-	

Table 71. Operational amplifier characteristics(1) (continued)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
en	Voltage noise density	@ 1KHz, Output loaded with 4 KΩ	-	109	-	$\frac{nV}{\sqrt{Hz}}$
		@ 10KHz, Output loaded with 4 KΩ	-	43	-	

1. Guaranteed by design, not tested in production.
2. The saturation voltage can also be limited by the I_{load}.
3. R2 is the internal resistance between OPAMP output and OPAMP inverting input.
   R1 is the internal resistance between OPAMP inverting input and ground.
   The PGA gain =1+R2/R1
4. Mostly TTa I/O leakage, when used in analog mode.

Figure 34. OPAMP voltage noise versus frequency



6.3.23 Temperature sensor (TS) characteristics

Table 72. Temperature sensor (TS) characteristics

Symbol	Parameter	Min.	Typ.	Max.	Unit
T_L(1)	V_{SENSE} linearity with temperature	-	±1	±2	°C
Avg_Slope(1)	Average slope	4.0	4.3	4.6	mV/°C
V_{25}	Voltage at 25 °C	1.34	1.43	1.52	V
t_{START}(1)	Startup time	4	-	10	µs
T_{S_temp}(1)(2)	ADC sampling time when reading the temperature	2.2	-	-	µs

1. Guaranteed by design, not tested in production.
2. Shortest sampling time can be determined in the application by multiple iterations.

Table 73. Temperature sensor (TS) calibration values

Calibration value name	Description	Memory address
TS_CAL1	TS ADC raw data acquired at temperature of 30 °C, V_{DDA}= 3.3 V	0x1FFF F7B8 - 0x1FFF F7B9
TS_CAL2	TS ADC raw data acquired at temperature of 110 °C V_{DDA}= 3.3 V	0x1FFF F7C2 - 0x1FFF F7C3

6.3.24 V_{BAT} monitoring characteristics

Table 74. V_{BAT} monitoring characteristics

Symbol	Parameter	Min.	Typ.	Max.	Unit
R	Resistor bridge for V_{BAT}	-	50	-	KΩ
Q	Ratio on V_{BAT} measurement	-	2	-	-
Er(1)	Error on Q	-1	-	+1	%
T_{S_vbat}(1)(2)	ADC sampling time when reading the V_{BAT} 1mV accuracy	2.2	-	-	µs

1. Guaranteed by design, not tested in production.
2. Shortest sampling time can be determined in the application by multiple iterations.

7 Package information

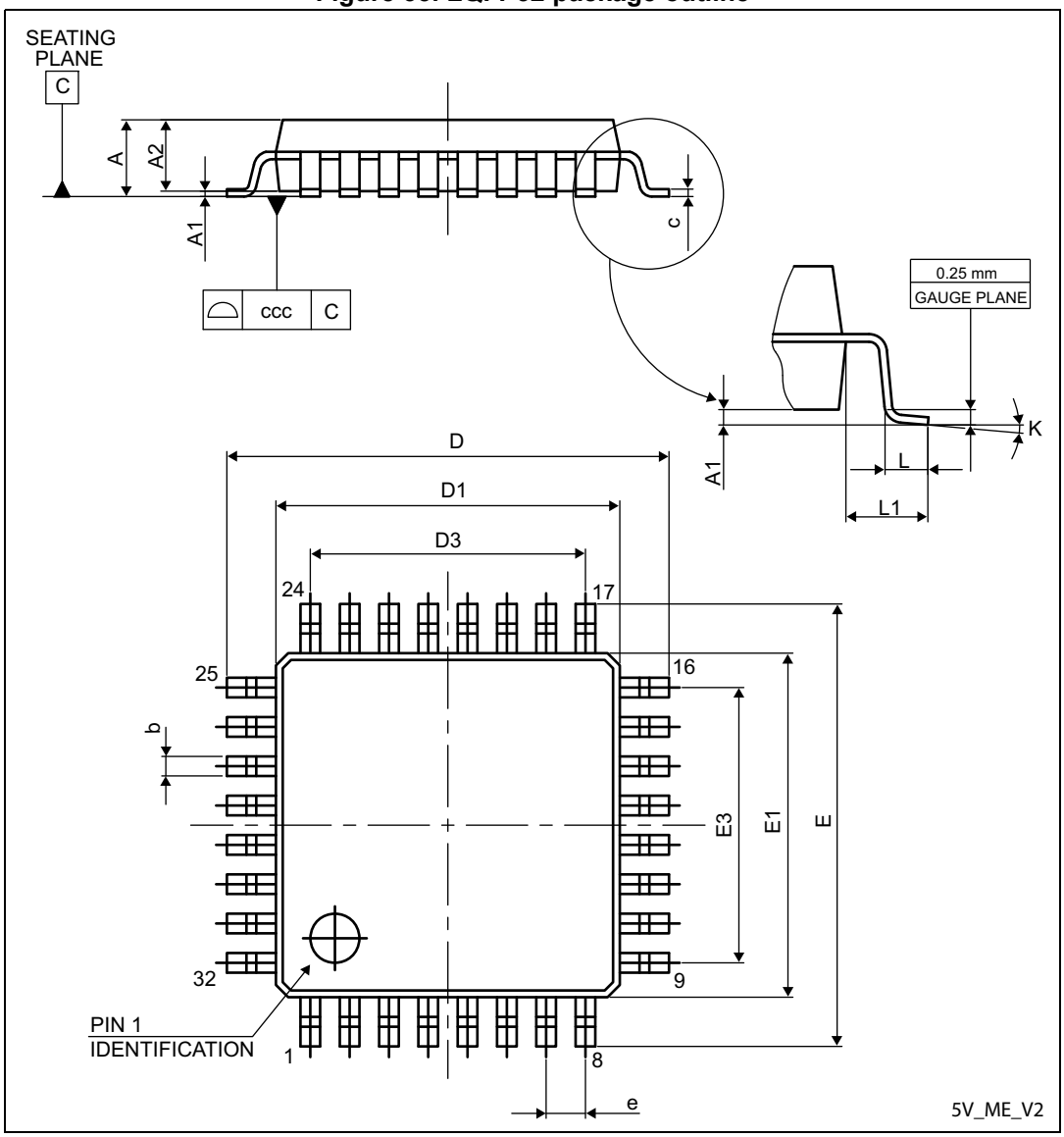
7.1 Package mechanical data

To meet the environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

7.2 LQFP32 package information

LQFP32 is a 32-pin, 7 x 7mm low-profile quad flat package.

Figure 35. LQFP32 package outline



1. Drawing is not to scale.

Table 75. LQFP32 mechanical data

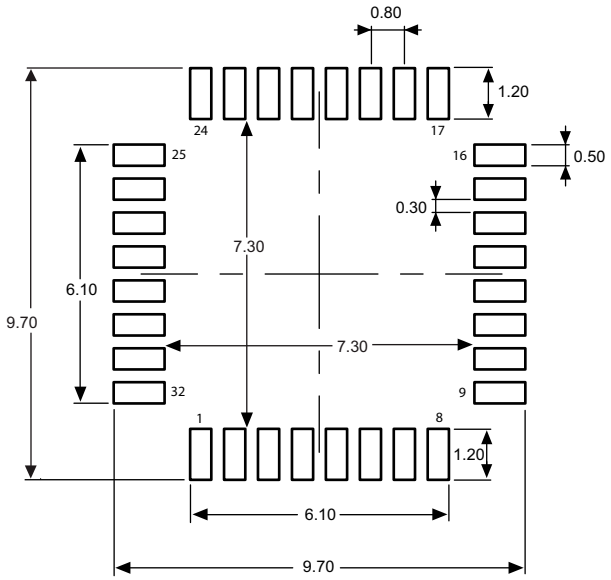
Symbol	Millimeters			Inches[1]		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571

Table 75. LQFP32 mechanical data (continued)

Symbol	Millimeters			Inches[1]		
	Min.	Typ.	Max.	Min.	Typ.	Max.
b	0.300	0.370	0.450	0.0118	0.0146	0.0177
c	0.090	-	0.200	0.0035	-	0.0079
D	8.800	9.000	9.200	0.3465	0.3543	0.3622
D1	6.800	7.000	7.200	0.2677	0.2756	0.2835
D3	-	5.600	-	-	0.2205	-
E	8.800	9.000	9.200	0.3465	0.3543	0.3622
E1	6.800	7.000	7.200	0.2677	0.2756	0.2835
E3	-	5.600	-	-	0.2205	-
e	-	0.800	-	-	0.0315	-
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
k	0.0°	3.5°	7.0°	0.0°	3.5°	7.0°
ccc	-	-	0.100	-	-	0.0039

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 36. Recommended footprint for the LQFP32 package



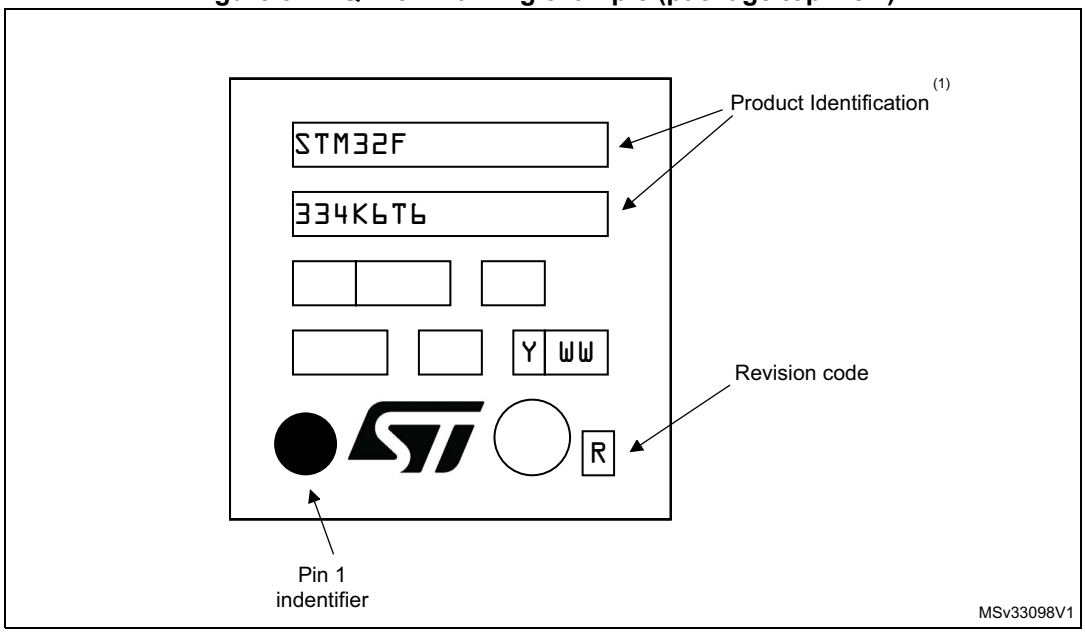
1. Drawing is not to scale.
2. Dimensions are expressed in millimeters.

Device marking for LQFP32

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

Figure 37. LQFP32 marking example (package top view)

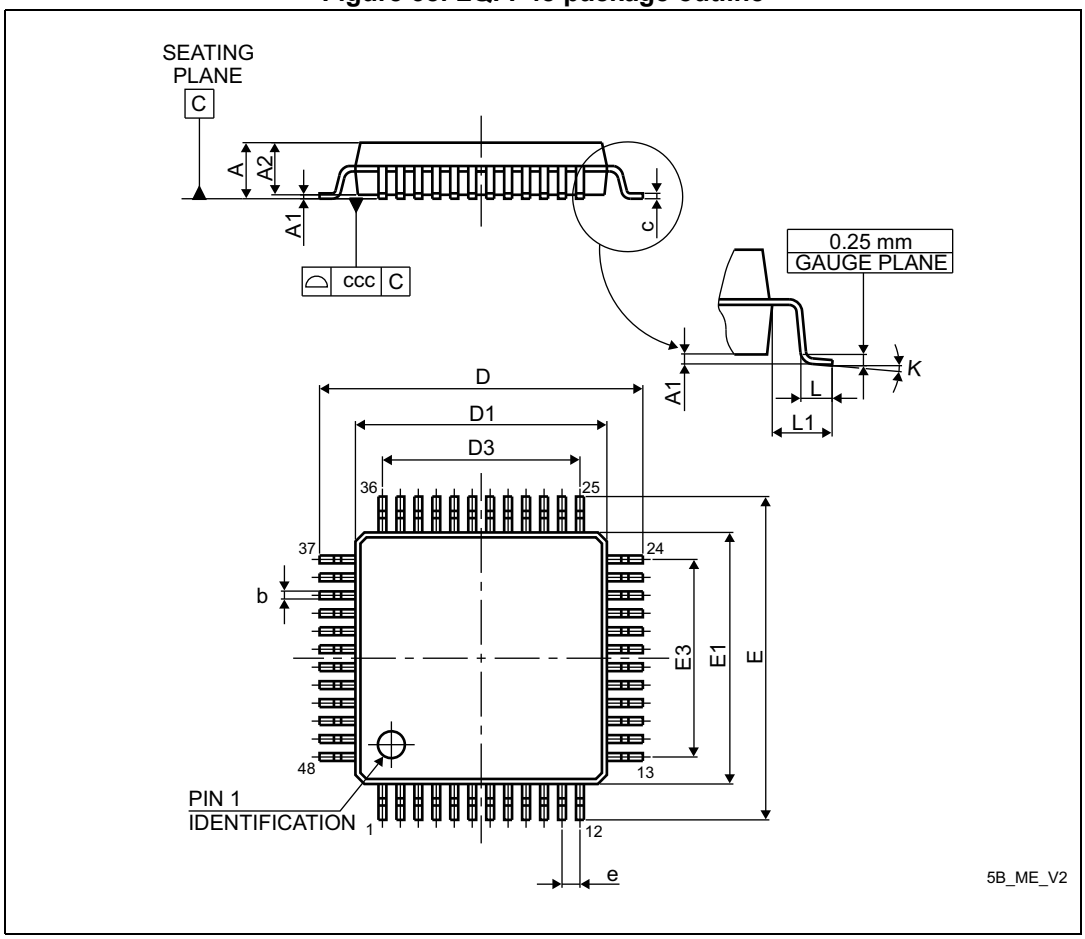


1. Parts marked as ES or E or accompanied by an Engineering Sample notification letter are not yet qualified and therefore not approved for use in production. ST is not responsible for any consequences resulting from such use. In no event will ST be liable for the customer using any of these engineering samples in production. ST's Quality department must be contacted prior to any decision to use these engineering samples to run a qualification activity.

7.3 LQFP48 package information

LQFP48 is a 48-pin, 7 x 7mm low-profile quad flat package.

Figure 38. LQFP48 package outline



1. Drawing is not to scale.

Table 76. LQFP48 package mechanical data

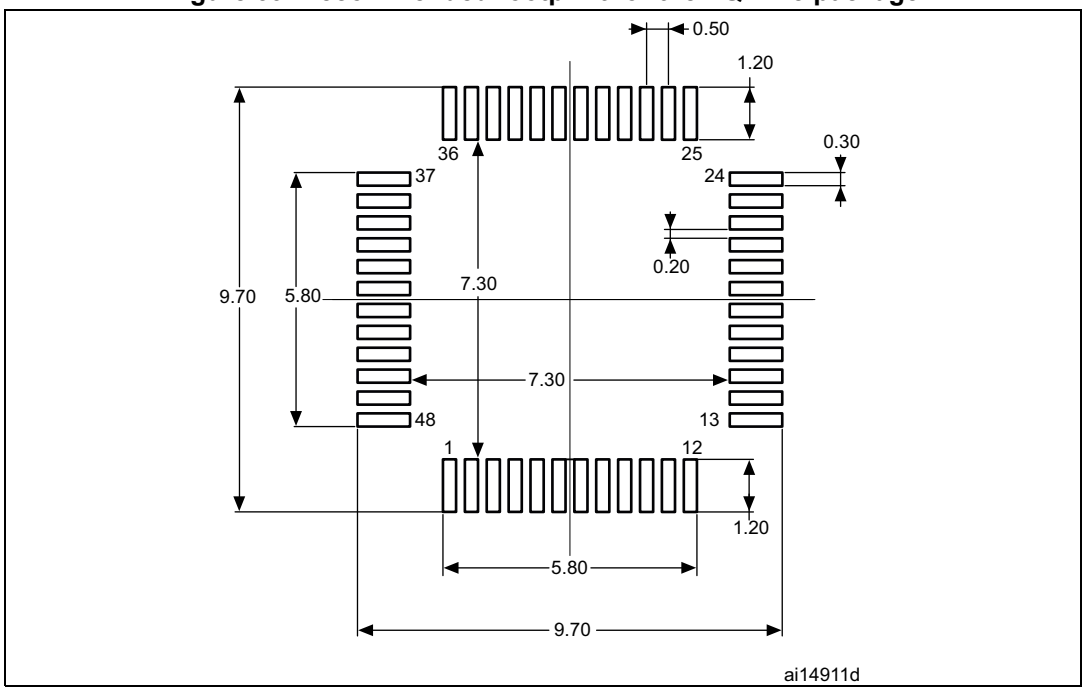
Symbol	millimeters			inches(1)		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090	-	0.200	0.0035	-	0.0079
D	8.800	9.000	9.200	0.3465	0.3543	0.3622
D1	6.800	7.000	7.200	0.2677	0.2756	0.2835
D3	-	5.500	-	-	0.2165	-

Table 76. LQFP48 package mechanical data (continued)

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
E	8.800	9.000	9.200	0.3465	0.3543	0.3622
E1	6.800	7.000	7.200	0.2677	0.2756	0.2835
E3	-	5.500	-	-	0.2165	-
e	-	0.500	-	-	0.0197	-
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-		0.0394	-
k	0°	3.5°	7°	0°	3.5°	7°
ccc	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 39. Recommended footprint for the LQFP48 package



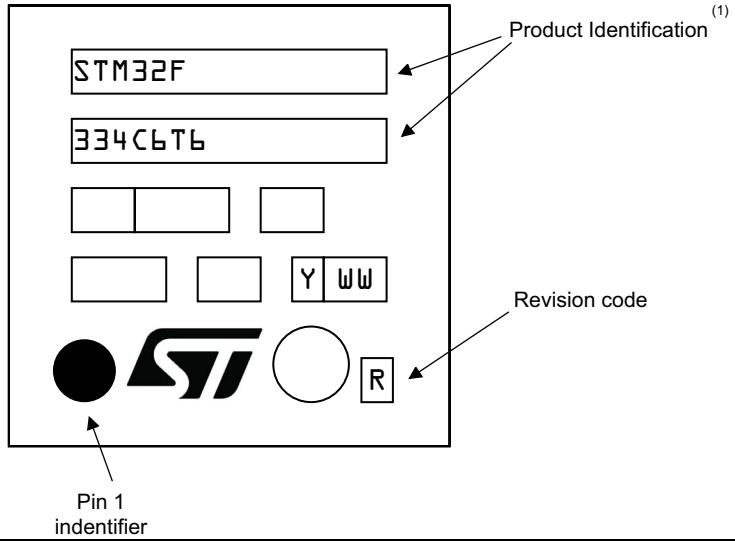
1. Drawing is not to scale.
2. Dimensions are in millimeters.

Device marking for LQFP48

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

Figure 40. LQFP48 marking example (package top view)

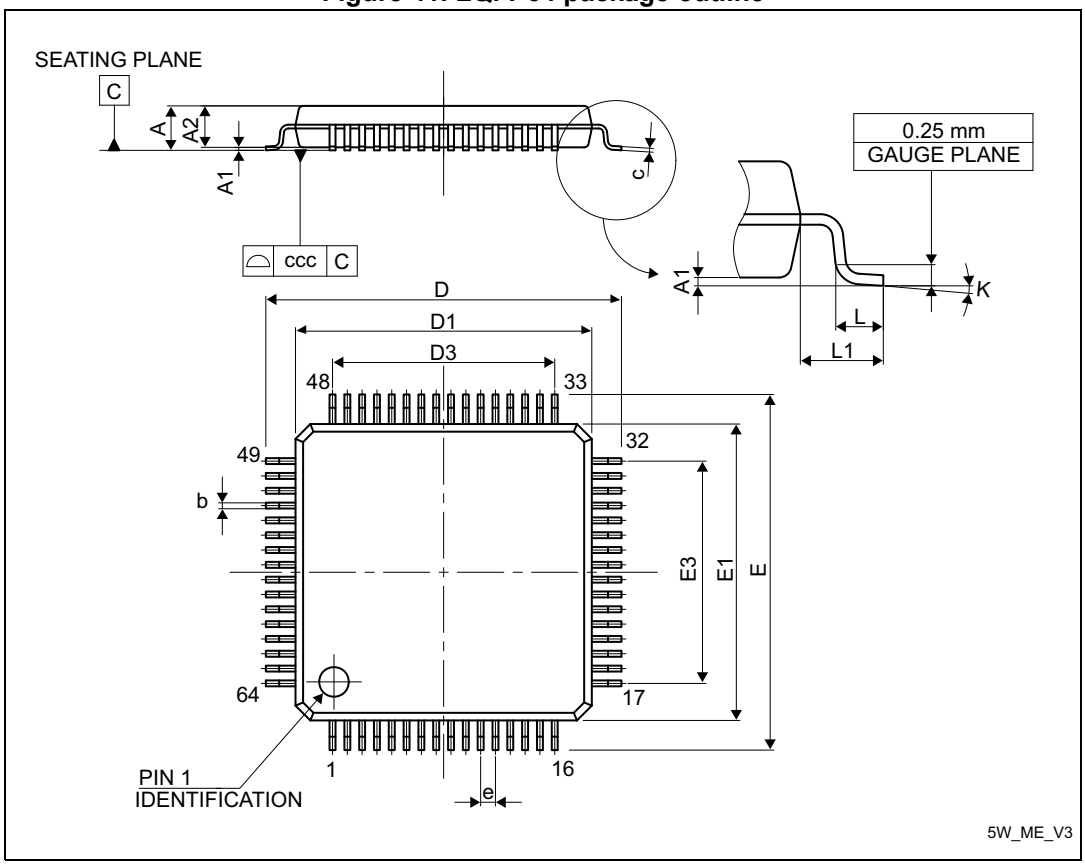


1. Parts marked as ES or E or accompanied by an Engineering Sample notification letter are not yet qualified and therefore not approved for use in production. ST is not responsible for any consequences resulting from such use. In no event will ST be liable for the customer using any of these engineering samples in production. ST's Quality department must be contacted prior to any decision to use these engineering samples to run a qualification activity.

7.4 LQFP64 package information

LQFP64 is a 64-pin, 10 x 10 mm low-profile quad flat package.

Figure 41. LQFP64 package outline



1. Drawing is not to scale.

Table 77. LQFP64 package mechanical data

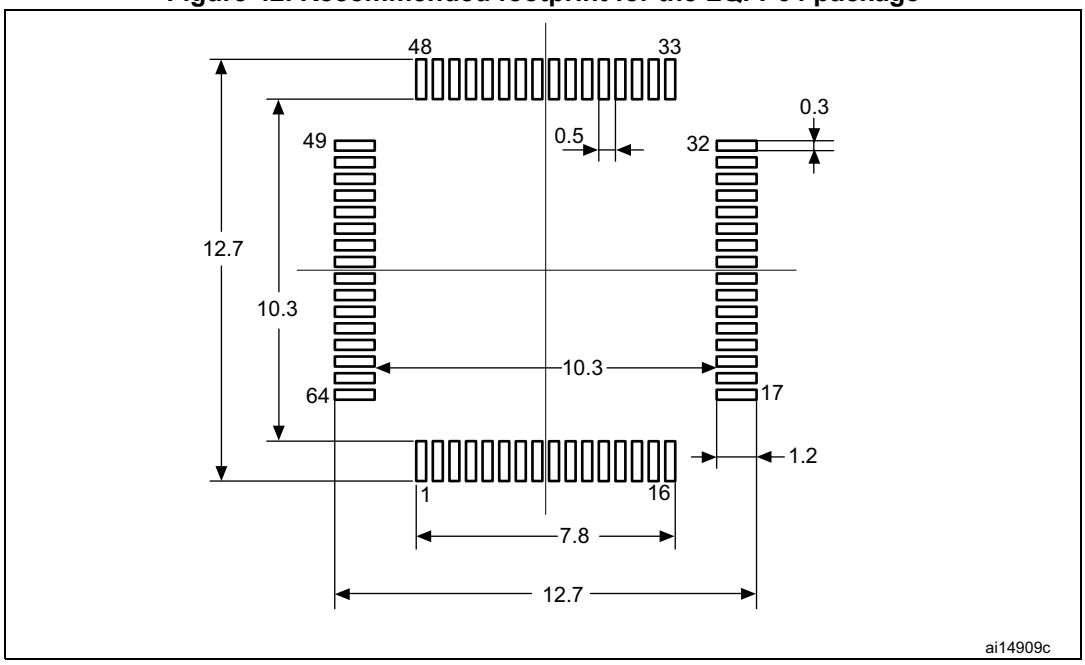
Symbol	millimeters			inches(1)		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090	-	0.200	0.0035	-	0.0079
D	11.800	12.000	-	-	0.4724	-
D1	9.800	10.000	-	-	0.3937	-
E	-	12.000	-	-	0.4724	-
E1	-	10.000	-	-	0.3937	-
e	-	0.500	-	-	0.0197	-

Table 77. LQFP64 package mechanical data (continued)

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
θ	0°	3.5°	7°	0°	3.5°	7°
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
N	Number of pins					
	64					

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 42. Recommended footprint for the LQFP64 package



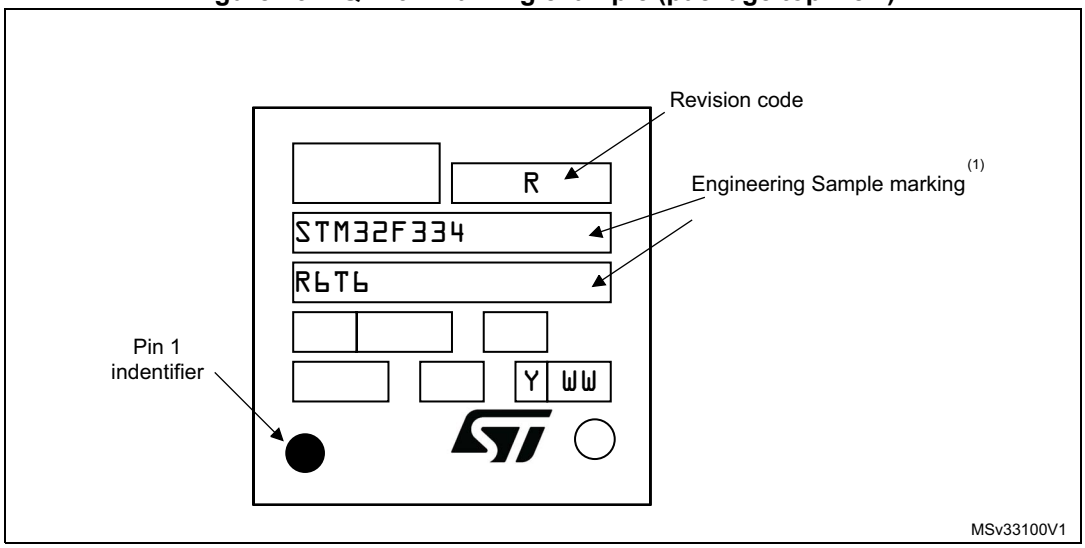
1. Drawing is not to scale.
2. Dimensions are in millimeters.

Device marking for LQFP64

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

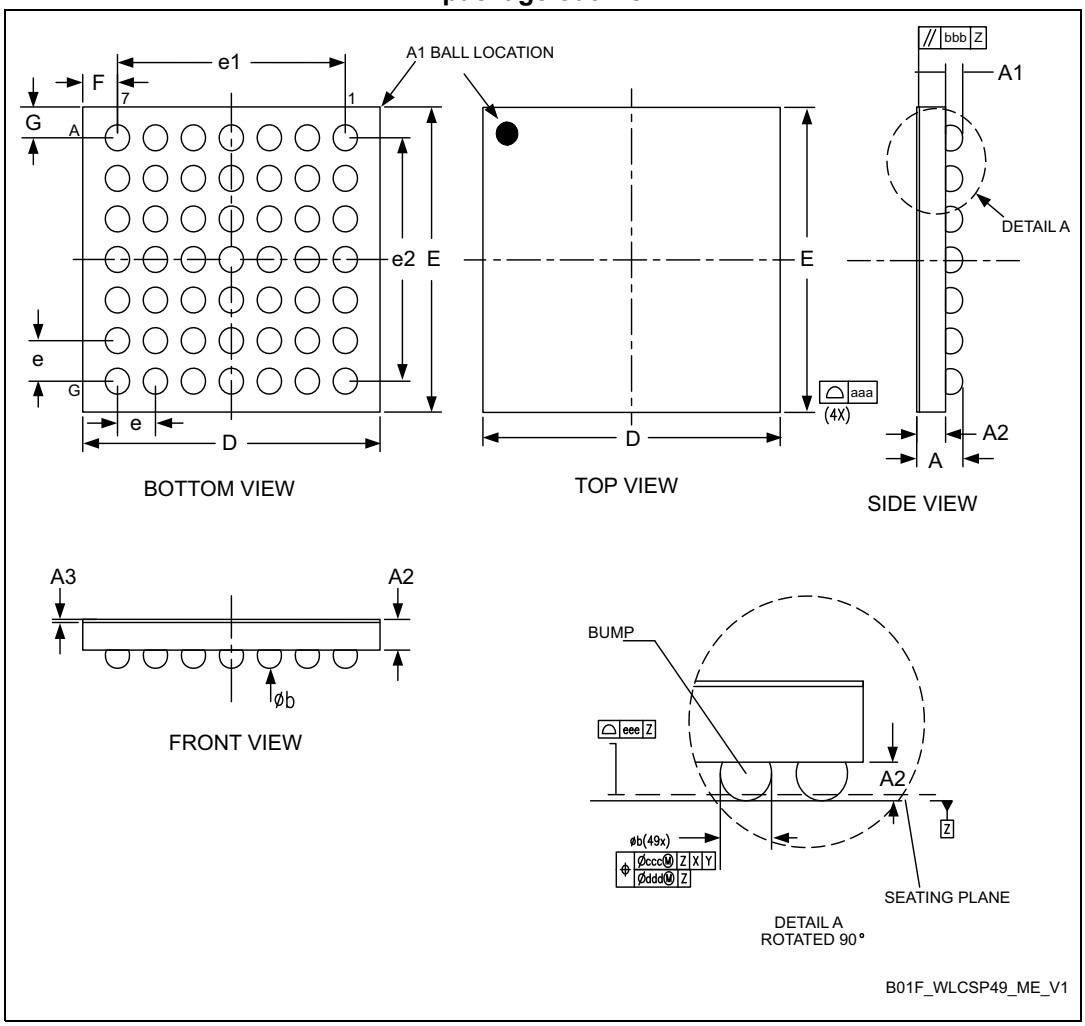
Figure 43. LQFP64 marking example (package top view)



1. Parts marked as ES or E or accompanied by an Engineering Sample notification letter are not yet qualified and therefore not approved for use in production. ST is not responsible for any consequences resulting from such use. In no event will ST be liable for the customer using any of these engineering samples in production. ST's Quality department must be contacted prior to any decision to use these engineering samples to run a qualification activity.

7.5 WLCSP49 package information

Figure 44. WLCSP - 49 ball, 3.89x3.74 mm, 0.5 mm pitch, wafer level chip scale, package outline



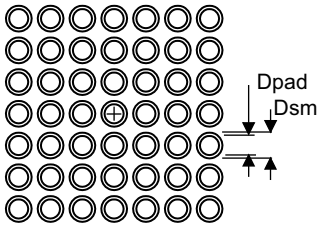
1. Dimension is measured at the maximum bump diameter parallel to primary datum Z.
2. Primary datum Z and seating plane are defined by the spherical crowns of the bump.
3. Bump position designation per JESD 95-1, SPP-010.

Table 78. WLCSP - 49 ball, 3.89x3.74 mm, 0.5 mm pitch, wafer level chip scale, mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	-	-	0.62	-	-	0.0244
A1	-	0.23	-	-	0.009	-
A2	-	0.36	-	-	0.014	-
A3	-	0.025[2]	-	-	0.001	-
b	0.30	0.33	0.36	0.012	0.013	0.014
D	3.87	3.89	3.91	0.152	0.153	0.154
E	3.72	3.74	3.76	0.146	0.147	0.148
e	-	0.50	-	-	0.020	-
e1	-	3.00	-	-	0.118	-
e2	-	3.00	-	-	0.118	-
F	-	0.445[3]	-	-	0.017	-
G	-	0.370[4]	-	-	0.015	-
aaa	-	-	0.10	-	-	0.004
bbb	-	-	0.10	-	-	0.004
ccc	-	-	0.10	-	-	0.004
ddd	-	-	0.05	-	-	0.002
eee	-	-	0.05	-	-	0.002

1. Values in inches are converted from mm and rounded to 4 decimal digits.
2. A3 value is guaranteed by technology design value.
3. This value is calculated from over value D and e1.
4. This value is calculated from over value E and e2.

Figure 45. WLCSP - 49 ball, 3.89x3.74 mm, 0.5 mm pitch, wafer level chip scale, recommended footprint



1. Dimensions are expressed in millimeters.

Table 79. WLCSP - 49 ball, 3.89x3.74 mm, 0.5 mm pitch, wafer level chip scale, recommended PCB design rules

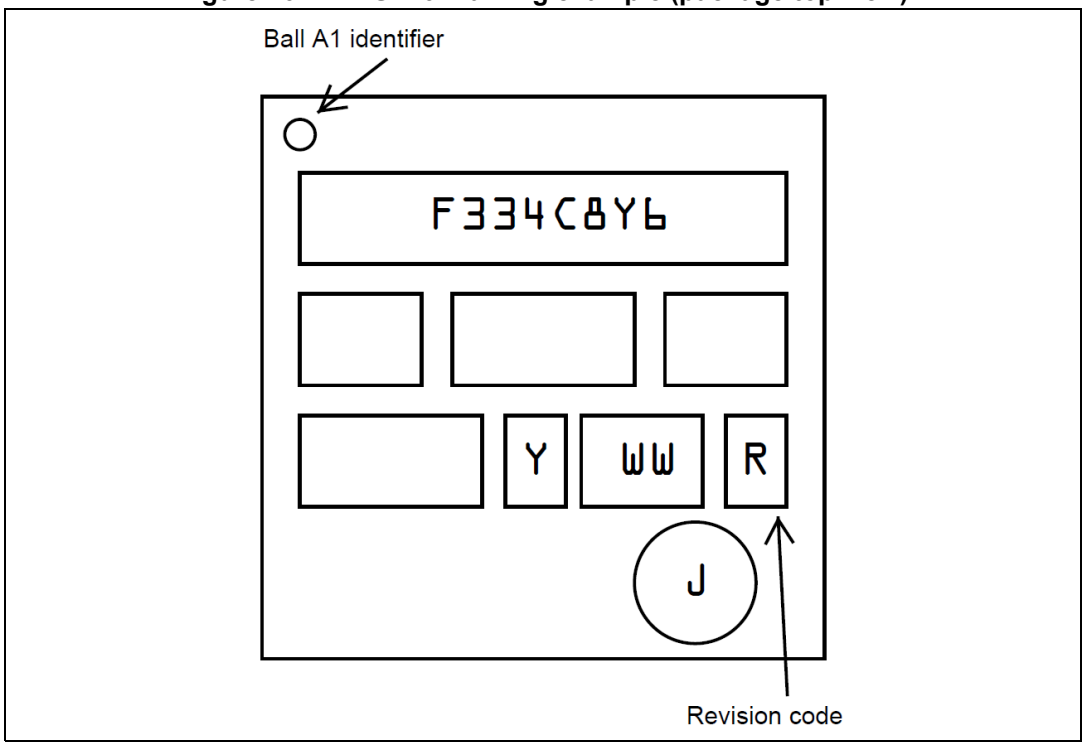
Dimension	Recommended values
Pitch	0.5 mm
Dpad	0.290 mm
Dsm	0.350 mm typ. (depends on the soldermask registration tolerance)
Stencil opening	0.310 mm
Stencil thickness	0.100 mm

Device marking

The following figure gives an example of topside marking orientation versus ball A1 identifier location.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

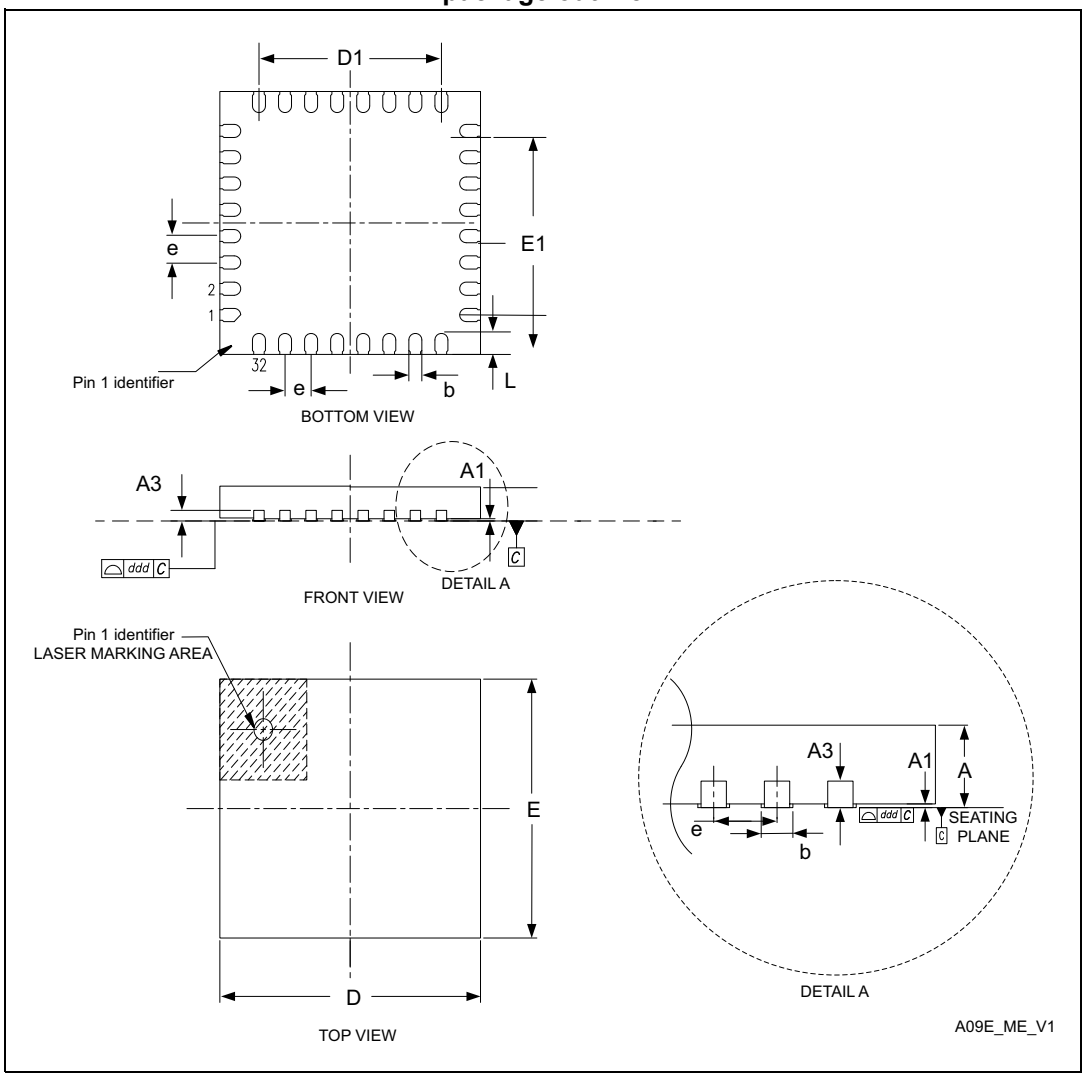
Figure 46. WLCSP49 marking example (package top view)



1. Parts marked as ES or E or accompanied by an Engineering Sample notification letter are not yet qualified and therefore not approved for use in production. ST is not responsible for any consequences resulting from such use. In no event will ST be liable for the customer using any of these engineering samples in production. ST's Quality department must be contacted prior to any decision to use these engineering samples to run a qualification activity.

7.6 UFQFPN32 package information

Figure 47. UFQFPN - 32 pin, 5 x 5 mm 0.5 mm pitch ultra thin fine pitch quad flat package outline



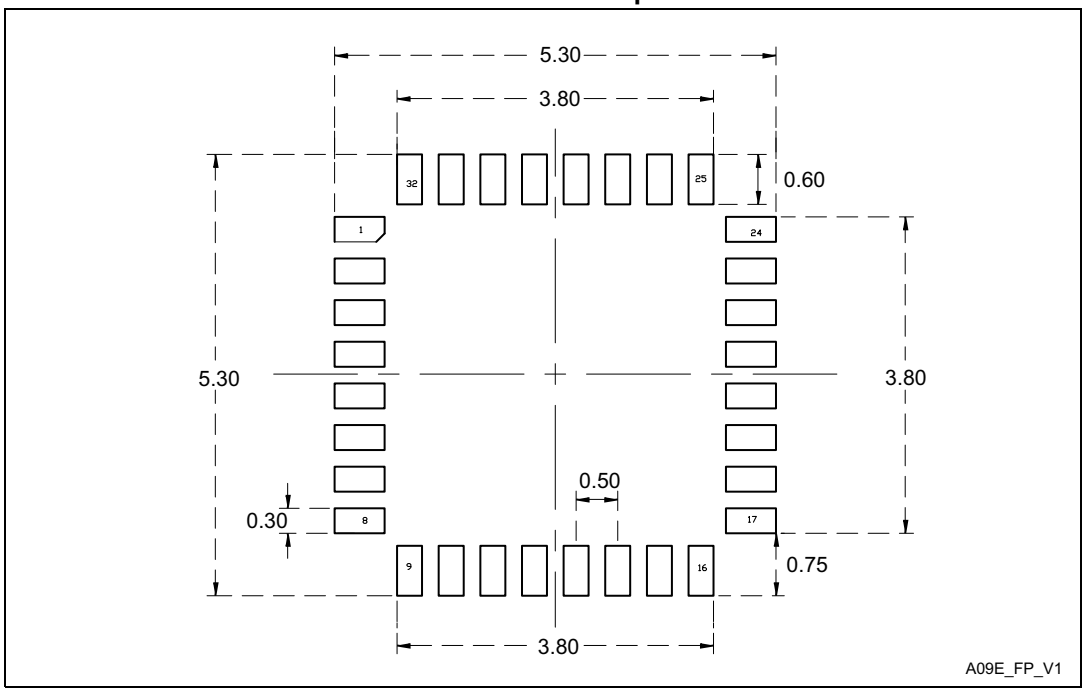
1. Drawing is not in scale.

Table 80. UFQFPN - 32 pin, 5 x 5 mm 0.5 mm pitch ultra thin fine pitch quad flat mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A[2]	0.500	0.550	0.600	0.0197	0.0217	0.0236
A1	0	0.020	0.050	0	0.0008	0.0020
A3	-	0.152	-	-	0.0060	-
b	0.180	0.250	0.280	0.0071	0.0098	0.0110
D[3]	4.900	5.000	5.100	0.1929	0.1969	0.2008
D1	3.400	3.500	3.600	0.1339	0.1378	0.1417
E[3]	4.900	5.000	5.100	0.1929	0.1969	0.2008
E1	3.400	3.500	3.600	0.1339	0.1378	0.1417
e	-	0.500	-	-	0.0197	-
L	0.300	0.400	0.500	0.0118	0.0157	0.0197
ddd	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.
2. UFQFPN stands for Thermally Enhanced Ultrathin Fine pitch Quad Flat Package No lead.
3. Dimensions D and E do not include mold protrusion, not to exceed 0,15mm.

Figure 48. UFQFPN - 32 pin, 5 x 5 mm 0.5 mm pitch ultra thin fine pitch quad flat recommended footprint



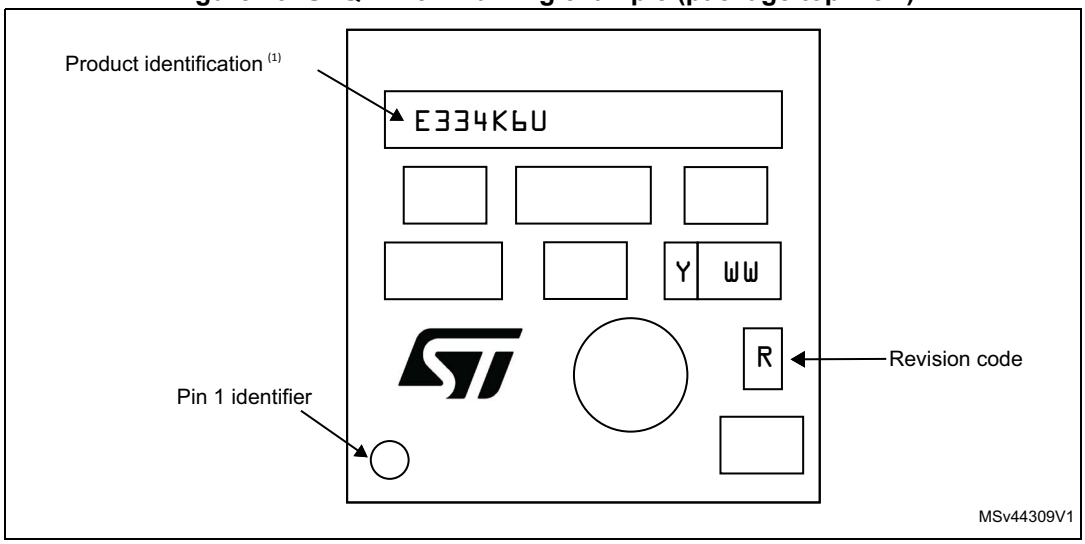
1. Dimensions are expressed in millimeters.

Device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

Figure 49. UFQFPN32 marking example (package top view)



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7.7 Thermal characteristics

The maximum chip-junction temperature, T_J max, in degrees Celsius, may be calculated using the following equation:

T_J max = T_A max + (P_D max x Θ_{JA})

Where:

- T_A max is the maximum ambient temperature in °C,
- Θ_{JA} is the package junction-to-ambient thermal resistance, in °C/W,
- P_D max is the sum of P_{INT} max and $P_{I/O}$ max (P_D max = P_{INT} max + $P_{I/O}$ max),
- P_{INT} max is the product of I_{DD} and V_{DD}, expressed in Watts. This is the maximum chip internal power.

$P_{I/O}$ max represents the maximum power dissipation on output pins where:

$$P_{I/O} \text{ max} = \Sigma (V_{OL} \times I_{OL}) + \Sigma((V_{DD} - V_{OH}) \times I_{OH}),$$

taking into account the actual V_{OL} / I_{OL} and V_{OH} / I_{OH} of the I/Os at low and high level in the application.

Table 81. Package thermal characteristics

Symbol	Parameter	Value	Unit
Θ_{JA}	**Thermal resistance junction-ambient** LQFP64 - 10 × 10 mm / 0.5 mm pitch	45	°C/W
	Thermal resistance junction-ambient LQFP48 - 7 × 7 mm / 0.5 mm pitch	55	
	Thermal resistance junction-ambient LQFP32 - 7 × 7 mm / 0.8 mm pitch	60	
	Thermal resistance junction-ambient UFQFN32 - 5 x 5 mm	37	
	Thermal resistance junction-ambient WLCSP49 - 3.89 x 3.74 mm / 0.5 mm pitch	48.3	

7.7.1 Reference document

JESD51-2 Integrated Circuits Thermal Test Method Environment Conditions - Natural Convection (Still Air). Available at the www.jedec.org website.

7.7.2 Selecting the product temperature range

When ordering the microcontroller, the temperature range is specified in the ordering information scheme shown in *Table 82: Ordering information scheme*.

Each temperature range suffix corresponds to a specific guaranteed ambient temperature at maximum dissipation and to a specific maximum junction temperature.

As applications do not commonly use the STM32F334x4/6/8 microcontroller at maximum dissipation, it is useful to calculate the exact power consumption and junction temperature to determine which temperature range is best suited to the application.

The following examples show how to calculate the temperature range needed for a given application.

Example: high-performance application

Assuming the following application conditions:

Maximum ambient temperature T_{Amax} = 82 °C (measured according to JESD51-2), I_{DDmax} = 50 mA, V_{DD} = 3.5 V, maximum 20 I/Os used at the same time in output at low level with I_{OL} = 8 mA, V_{OL}= 0.4 V and maximum 8 I/Os used at the same time in output mode at low level with I_{OL} = 20 mA, V_{OL}= 1.3 V

P_{INTmax} = 50 mA × 3.5 V = 175 mW

P_{IOmax} = 20 × 8 mA × 0.4 V + 8 × 20 mA × 1.3 V = 272 mW

This gives: P_{INTmax} = 175 mW and P_{IOmax} = 272 mW

P_{Dmax} = 175 + 272 = 447 mW

Thus: P_{Dmax} = 447 mW

Using the values obtained in *Table 81: Package thermal characteristics*, T_{Jmax} is calculated as follows:

– For LQFP64, 45 °C/W

T_{Jmax} = 82 °C + (45 °C/W × 447 mW) = 82 °C + 20.1 °C = 102.1 °C

This is within the range of the suffix 6 version parts (–40 < T_J < 105 °C).

In this case, parts must be ordered at least with the temperature range suffix 6 (see *Table 82: Ordering information scheme*).

8 Ordering information

Table 82. Ordering information scheme

Example: STM32 F 334 C 8 T 6 xxx

Device family

STM32 = Arm®-based 32-bit microcontroller

Product type

F = general-purpose

Device subfamily

334 = STM32F334xx, 2.0 to 3.6 V operating voltage

Pin count

K = 32 pins

C = 48 or 49 pins

R = 64 pins

Flash memory size

4 = 16 Kbytes of Flash memory

6 = 32 Kbytes of Flash memory

8 = 64 Kbytes of Flash memory

Package

T = LQFP
Y = WLCSP
U = UFQFPN

Temperature range

6 = Industrial temperature range, –40 to 85 °C

7 = Industrial temperature range, –40 to 105 °C

Options

xxx = programmed parts

TR = tape and reel

9 Revision history

Table 83. Document revision history

Date	Revision	Changes
19-Jun-2014	1	Initial release.
09-Dec-2014	2	Updated: – Table 54: TIMx characteristics – Table 14: STM32F334x6/8 pin definitions – Table 59: ADC characteristics – Table 34: Peripheral current consumption – Table 40: HSI oscillator characteristics – Table 17: HSI oscillator accuracy characterization results for soldered parts – Table 2: STM32F334x4/6/8 family device features and peripheral counts
2-Feb-2015	3	Updated: – *Figure 1: STM32F334x4/6/8 block diagram* – *Table 38: HSE oscillator characteristics* – *Table 43: Flash memory characteristics* Added *Figure 15: High-speed external clock source AC timing diagram*
09-Jun-2015	4	Updated: – Title – *Section 3.14.1: 217 ps high-resolution timer (HRTIM1)* – *Section 6.1.6: Power-supply scheme* – *Table 19: General operating conditions*
27-Sep-2016	5	Updated: *Section Table 69.: DAC characteristics*, *Section Table 64.: ADC characteristics*,*Table 53: NRST pin characteristics*, *Figure 2: Clock tree*, *Table 13: STM32F334x4/6/8 pin definitions*, *Table 71: Operational amplifier characteristics*, *Figure 22: 5V- tolerant (FT and FTf) I/O input characteristics - CMOS port*, *Table 23: Embedded internal reference voltage*, *Table 39: LSE oscillator characteristics (f_{LSE} = 32.768 kHz)* Added *Table 35: Wakeup time using USART*.
15-May-2017	6	Updated: – *Table 2: STM32F334x4/6/8 family device features and peripheral counts* – *Table 13: STM32F334x4/6/8 pin definitions* – *Table 19: General operating conditions* – *Table 81: Package thermal characteristics* – *Table 82: Ordering information scheme* Added: – *Figure 7: WLCSP49 ballout* – *Section 7.5: WLCSP49 package information*

Table 83. Document revision history (continued)

Date	Revision	Changes
23-Nov--2017	7	Updated: – Footnotes of *Table 25: Typical and maximum current consumption from V_{DD} supply at V_{DD} = 3.6V* – Footnotes of *Table 26: Typical and maximum current consumption from the V_{DDA} supply*
19-Dec-2017	8	Updated *Table 1: Device summary:* STM32F334R4 product not covered by this datasheet
16-Jul-2018	9	Updated: – *Table 2: STM32F334x4/6/8 family device features and peripheral counts* – *Table 13: STM32F334x4/6/8 pin definitions* – *Table 19: General operating conditions* – *Table 81: Package thermal characteristics* – *Table 82: Ordering information scheme* Added: – *Figure 8: UFQFPN32 pinout* – *Section 7.6: UFQFPN32 package information*

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