Important notice

Dear Customer,

On 7 February 2017 the former NXP Standard Product business became a new company with the tradename **Nexperia**. Nexperia is an industry leading supplier of Discrete, Logic and PowerMOS semiconductors with its focus on the automotive, industrial, computing, consumer and wearable application markets

In data sheets and application notes which still contain NXP or Philips Semiconductors references, use the references to Nexperia, as shown below.

Instead of http://www.nxp.com, http://www.philips.com/ or http://www.semiconductors.philips.com/, use **http://www.nexperia.com**

Instead of sales.addresses@www.nxp.com or sales.addresses@www.semiconductors.philips.com, use **salesaddresses@nexperia.com** (email)

Replace the copyright notice at the bottom of each page or elsewhere in the document, depending on the version, as shown below:
- © NXP N.V. (year). All rights reserved or © Koninklijke Philips Electronics N.V. (year). All rights reserved
Should be replaced with:
- **© Nexperia B.V. (year). All rights reserved**.

If you have any questions related to the data sheet, please contact our nearest sales office via e-mail or telephone (details via **salesaddresses@nexperia.com**). Thank you for your cooperation and understanding,

Kind regards,

Team Nexperia

sales@prom-elec.com / ООО ПРОМЭЛЕКТРОНИКА

NX3008CBKS

30 / 30 V, 350 / 200 mA N/P-channel Trench MOSFET

Rev. 1 — 29 July 2011 Product data sheet

1. Product profile

1.1 General description

Complementary N/P-channel enhancement mode Field-Effect Transistor (FET) in very small SOT363 (SC-88) Surface-Mounted Device (SMD) plastic package using Trench MOSFET technology.

1.2 Features and benefits

- Low threshold voltage
- Very fast switching
- Trench MOSFET technology
- ESD protection up to 2 kV
- AEC-Q101 qualified

1.3 Applications

- Level shifter
- Power supply converter
- Load switch
- Switching circuits

1.4 Quick reference data

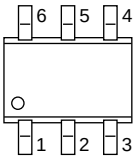
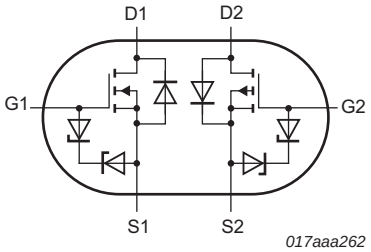
Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
TR2 (P-channel)							
V_{DS}	drain-source voltage	T_j = 25 °C		-	-	-30	V
V_{GS}	gate-source voltage			-8	-	8	V
I_D	drain current	V_{GS} = -4.5 V; T_{amb} = 25 °C	[1]	-	-	-200	mA
TR1 (N-channel)							
V_{DS}	drain-source voltage	T_j = 25 °C		-	-	30	V
V_{GS}	gate-source voltage			-8	-	8	V
I_D	drain current	V_{GS} = 4.5 V; T_{amb} = 25 °C	[1]	-	-	350	mA
TR1 (N-channel), Static characteristics							
R_{DSon}	drain-source on-state resistance	V_{GS} = 4.5 V; I_D = 350 mA; T_j = 25 °C		-	1	1.4	Ω
TR2 (P-channel), Static characteristics							
R_{DSon}	drain-source on-state resistance	V_{GS} = -4.5 V; I_D = -200 mA; T_j = 25 °C		-	2.8	4.1	Ω

[1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and mounting pad for drain 1 cm^2.

2. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S1	source TR1	 SOT363 (SC-88)	
2	G1	gate TR1		
3	D2	drain TR2		
4	S2	source TR2		
5	G2	gate TR2		
6	D1	drain TR1		

3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
NX3008CBKS	SC-88	plastic surface-mounted package; 6 leads	SOT363

4. Marking

Table 4. Marking codes

Type number	Marking code[1]
NX3008CBKS	LD%

[1] % = placeholder for manufacturing site code.

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2011. All rights reserved.

5. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
TR2 (P-channel)						
V_{DS}	drain-source voltage	T_j = 25 °C		-	-30	V
V_{GS}	gate-source voltage			-8	8	V
I_D	drain current	V_{GS} = -4.5 V; T_{amb} = 25 °C	[1]	-	-200	mA
		V_{GS} = -4.5 V; T_{amb} = 100 °C	[1]	-	-125	mA
I_{DM}	peak drain current	T_{amb} = 25 °C; single pulse; t_p ≤ 10 µs		-	-0.8	A
P_{tot}	total power dissipation	T_{amb} = 25 °C	[2]	-	280	mW
			[1]	-	320	mW
		T_{sp} = 25 °C		-	990	mW
TR1 (N-channel)						
V_{DS}	drain-source voltage	T_j = 25 °C		-	30	V
V_{GS}	gate-source voltage			-8	8	V
I_D	drain current	V_{GS} = 4.5 V; T_{amb} = 25 °C	[1]	-	350	mA
		V_{GS} = 4.5 V; T_{amb} = 100 °C	[1]	-	230	mA
I_{DM}	peak drain current	T_{amb} = 25 °C; single pulse; t_p ≤ 10 µs		-	1.4	A
P_{tot}	total power dissipation	T_{amb} = 25 °C	[2]	-	280	mW
			[1]	-	320	mW
		T_{sp} = 25 °C		-	990	mW
Per device						
P_{tot}	total power dissipation	T_{amb} = 25 °C	[2]	-	445	mW
T_j	junction temperature			-55	150	°C
T_{amb}	ambient temperature			-55	150	°C
T_{stg}	storage temperature			-65	150	°C
TR1 (N-channel), Source-drain diode						
I_S	source current	T_{amb} = 25 °C	[1]	-	300	mA
TR2 (P-channel), Source-drain diode						
I_S	source current	T_{amb} = 25 °C	[1]	-	-200	mA
TR1 N-channel), ESD maximum rating						
V_{ESD}	electrostatic discharge voltage	HBM	[3]	-	2000	V
TR2 (P-channel), ESD maximum rating						
V_{ESD}	electrostatic discharge voltage	HBM	[3]	-	2000	V

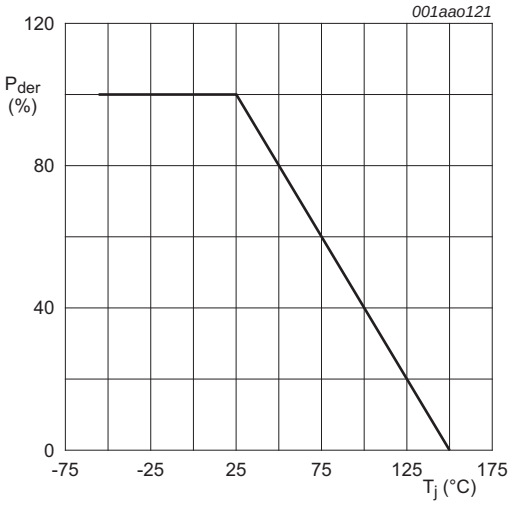
[1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and mounting pad for drain 1 cm^2.

[2] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper; tin-plated and standard footprint.

[3] Measured between all pins.

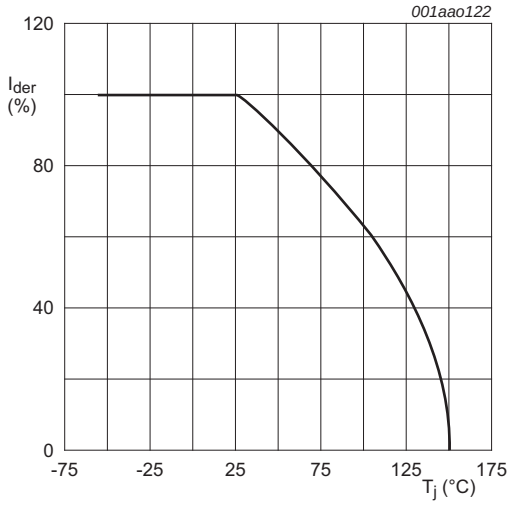
All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2011. All rights reserved.



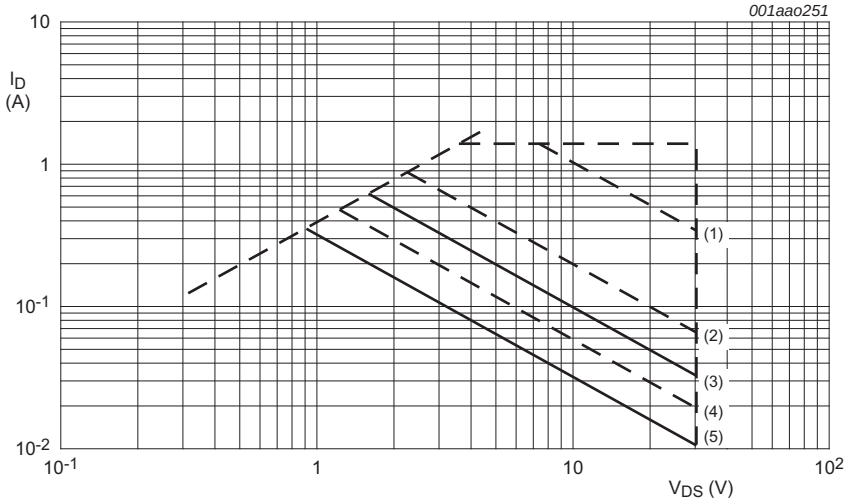
$$P_{der} = \frac{P_{tot}}{P_{tot(25°C)}} \times 100\,\%$$

Fig 1. Normalized total power dissipation as a function of junction temperature



$$I_{der} = \frac{I_D}{I_{D(25°C)}} \times 100\,\%$$

Fig 2. Normalized continuous drain current as a function of junction temperature



I_{DM} is a single pulse

(1) t_p = 1 ms

(2) t_p = 10 ms

(3) DC; T_{sp} = 25 °C

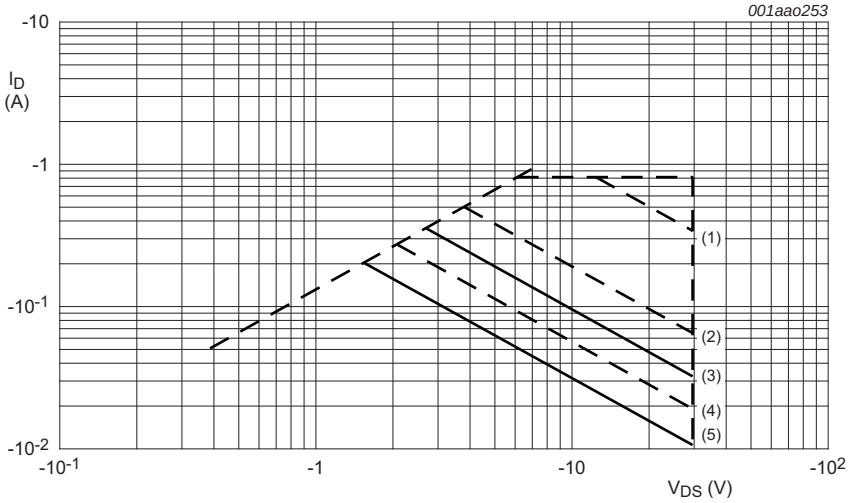
(4) t_p = 100 ms

(5) DC; T_{amb} = 25 °C; 1 cm^2 drain mounting pad

Fig 3. Safe operating area TR1 (N-channel); junction to ambient; continuous and peak drain currents as a function of drain-source voltage

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2011. All rights reserved.



I_{DM} is a single pulse

(1) t_p = 1 ms

(2) t_p = 10 ms

(3) DC; T_{sp} = 25 °C

(4) t_p = 100 ms

(5) DC; T_{amb} = 25 °C; 1 cm^2 drain mounting pad

Fig 4. Safe operating area TR2 (P-channel); junction to ambient; continuous and peak drain currents as a function of drain-source

6. Thermal characteristics

Table 6. Thermal characteristics

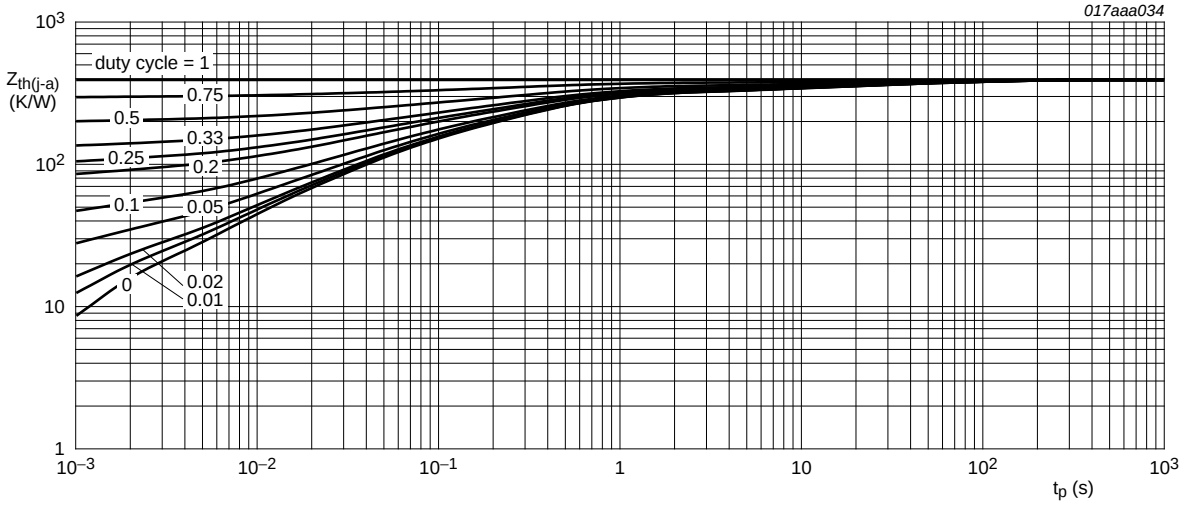
Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Per device							
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	[1]	-	-	300	K/W
TR1 (N-channel)							
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	[1]	-	390	445	K/W
			[2]	-	340	390	K/W
$R_{th(j-sp)}$	thermal resistance from junction to solder point			-	-	130	K/W
TR2 (P-channel)							
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	[1]	-	390	445	K/W
			[2]	-	340	390	K/W
$R_{th(j-sp)}$	thermal resistance from junction to solder point			-	-	130	K/W

[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper; tin-plated and standard footprint.

[2] Device mounted on an FR4 PCB, single-sided copper, tin-plated and mounting pad for drain 1 cm^2.

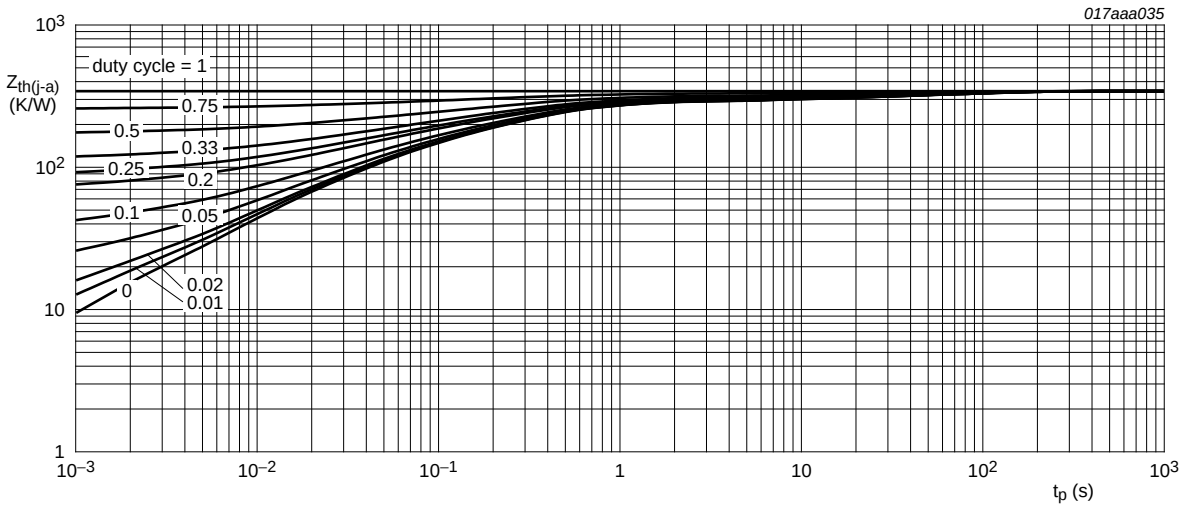
All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2011. All rights reserved.



FR4 PCB, standard footprint

Fig 5. TR1: Transient thermal impedance from junction to ambient as a function of pulse duration; typical values

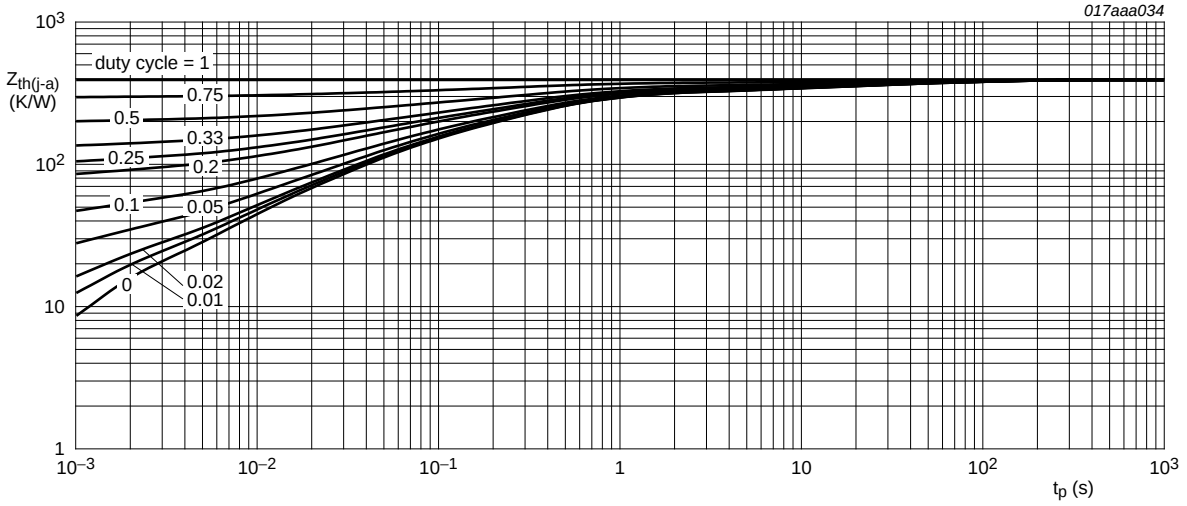


FR4 PCB, mounting pad for drain 1 cm^2.

Fig 6. TR1: Transient thermal impedance from junction to ambient as a function of pulse duration; typical values

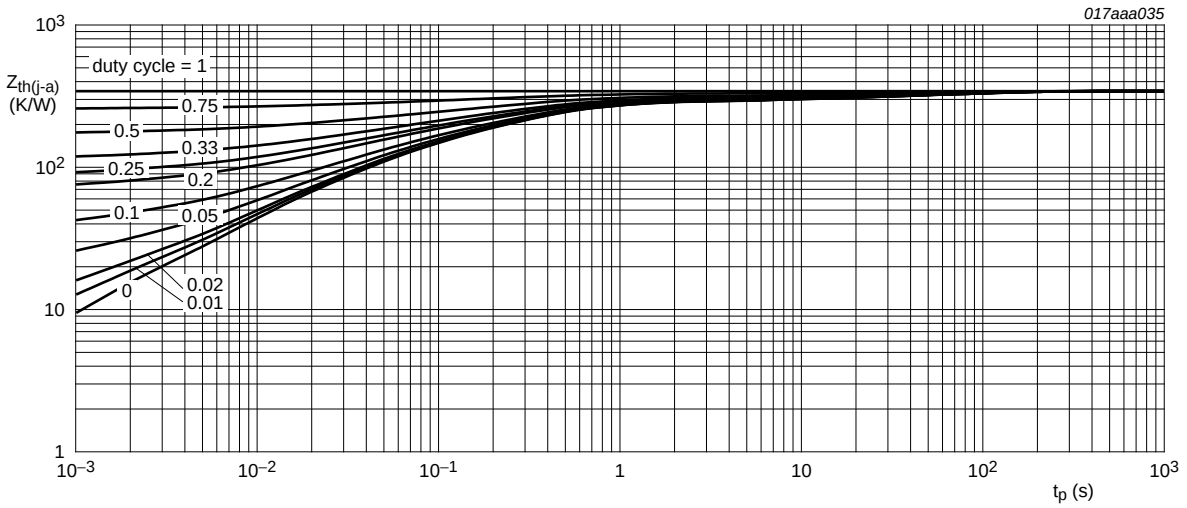
All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2011. All rights reserved.



FR4 PCB, standard footprint

Fig 7. TR2, Transient thermal impedance from junction to ambient as a function of pulse duration; typical values



FR4 PCB, mounting pad for drain 1 cm^2

Fig 8. TR2, Transient thermal impedance from junction to ambient as a function of pulse duration; typical values

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2011. All rights reserved.

7. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
TR2 (P-channel), Static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	I_D = -250 µA; V_{GS} = 0 V; T_j = 25 °C	-30	-	-	V
V_{GSth}	gate-source threshold voltage	I_D = -250 µA; V_{DS} = V_{GS}; T_j = 25 °C	-0.6	-0.9	-1.1	V
I_{DSS}	drain leakage current	V_{DS} = -30 V; V_{GS} = 0 V; T_j = 25 °C	-	-	-1	µA
		V_{DS} = -30 V; V_{GS} = 0 V; T_j = 150 °C	-	-	-10	µA
I_{GSS}	gate leakage current	V_{GS} = 8 V; V_{DS} = 0 V; T_j = 25 °C	-	-0.2	-1	µA
		V_{GS} = -8 V; V_{DS} = 0 V; T_j = 25 °C	-	-0.2	-1	µA
		V_{GS} = 4.5 V; V_{DS} = 0 V; T_j = 25 °C	-	-10	-	nA
		V_{GS} = -4.5 V; V_{DS} = 0 V; T_j = 25 °C	-	-10	-	nA
		V_{GS} = 2.5 V; V_{DS} = 0 V; T_j = 25 °C	-	-1	-	nA
		V_{GS} = -2.5 V; V_{DS} = 0 V; T_j = 25 °C	-	-1	-	nA
R_{DSon}	drain-source on-state resistance	V_{GS} = -4.5 V; I_D = -200 mA; T_j = 25 °C	-	2.8	4.1	Ω
		V_{GS} = -2.5 V; I_D = -10 mA; T_j = 25 °C	-	5.3	6.5	Ω
		V_{GS} = -4.5 V; I_D = -200 mA; T_j = 150 °C	-	5.3	7.8	Ω
g_{fs}	transfer conductance	V_{DS} = -10 V; I_D = -200 mA; T_j = 25 °C	-	160	-	mS
TR1 (N-channel), Static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	I_D = 250 µA; V_{GS} = 0 V; T_j = 25 °C	30	-	-	V
V_{GSth}	gate-source threshold voltage	I_D = 250 µA; V_{DS} = V_{GS}; T_j = 25 °C	0.6	0.9	1.1	V
I_{DSS}	drain leakage current	V_{DS} = 30 V; V_{GS} = 0 V; T_j = 25 °C	-	-	1	µA
		V_{DS} = 30 V; V_{GS} = 0 V; T_j = 150 °C	-	-	10	µA
I_{GSS}	gate leakage current	V_{GS} = 8 V; V_{DS} = 0 V; T_j = 25 °C	-	0.2	1	µA
		V_{GS} = -8 V; V_{DS} = 0 V; T_j = 25 °C	-	0.2	1	µA
		V_{GS} = 4.5 V; V_{DS} = 0 V; T_j = 25 °C	-	10	-	nA
		V_{GS} = -4.5 V; V_{DS} = 0 V; T_j = 25 °C	-	10	-	nA
		V_{GS} = 2.5 V; V_{DS} = 0 V; T_j = 25 °C	-	1	-	nA
		V_{GS} = -2.5 V; V_{DS} = 0 V; T_j = 25 °C	-	1	-	nA
R_{DSon}	drain-source on-state resistance	V_{GS} = 4.5 V; I_D = 350 mA; T_j = 25 °C	-	1	1.4	Ω
		V_{GS} = 4.5 V; I_D = 350 mA; T_j = 150 °C	-	1.8	2.5	Ω
		V_{GS} = 2.5 V; I_D = 200 mA; T_j = 25 °C	-	1.4	2.1	Ω
		V_{GS} = 1.8 V; I_D = 10 mA; T_j = 25 °C	-	2	2.8	Ω
g_{fs}	transfer conductance	V_{DS} = 10 V; I_D = 350 mA; T_j = 25 °C	-	310	-	mS
TR1 (N-channel), Dynamic characteristics						
$Q_{G(tot)}$	total gate charge	V_{DS} = 15 V; I_D = 350 mA; V_{GS} = 4.5 V; T_j = 25 °C	-	0.52	0.68	nC
Q_{GS}	gate-source charge		-	0.17	-	nC
Q_{GD}	gate-drain charge		-	0.08	-	nC

All information provided in this document is subject to legal disclaimers.

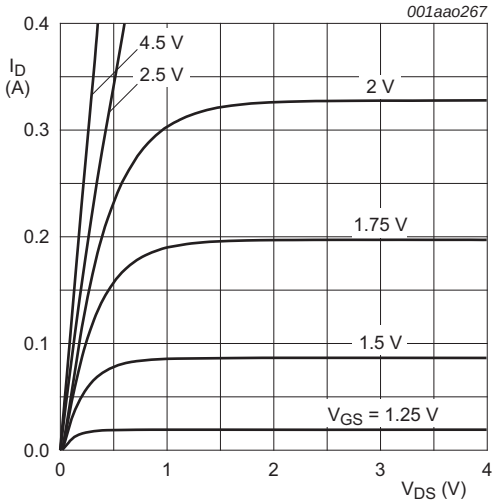
© NXP B.V. 2011. All rights reserved.

Table 7. Characteristics *...continued*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
C_{iss}	input capacitance	V_{DS} = 15 V; f = 1 MHz; V_{GS} = 0 V; T_j = 25 °C	-	34	50	pF
C_{oss}	output capacitance		-	6.5	-	pF
C_{rss}	reverse transfer capacitance		-	2.2	-	pF
$t_{d(on)}$	turn-on delay time	V_{DS} = 20 V; R_L = 250 Ω; V_{GS} = 4.5 V; $R_{G(ext)}$ = 6 Ω; T_j = 25 °C	-	15	30	ns
t_r	rise time		-	11	-	ns
$t_{d(off)}$	turn-off delay time		-	69	138	ns
t_f	fall time		-	19	-	ns
TR2 (P-channel), Dynamic characteristics						
$Q_{G(tot)}$	total gate charge	V_{DS} = -15 V; I_D = -200 mA; V_{GS} = -4.5 V; T_j = 25 °C	-	0.55	0.72	nC
Q_{GS}	gate-source charge		-	0.23	-	nC
Q_{GD}	gate-drain charge		-	0.09	-	nC
C_{iss}	input capacitance	V_{DS} = -15 V; f = 1 MHz; V_{GS} = 0 V; T_j = 25 °C	-	31	46	pF
C_{oss}	output capacitance		-	6.5	-	pF
C_{rss}	reverse transfer capacitance		-	2.3	-	pF
$t_{d(on)}$	turn-on delay time	V_{DS} = -20 V; R_L = 250 Ω; V_{GS} = -4.5 V; $R_{G(ext)}$ = 6 Ω; T_j = 25 °C	-	19	38	ns
t_r	rise time		-	30	-	ns
$t_{d(off)}$	turn-off delay time		-	65	130	ns
t_f	fall time		-	38	-	ns
TR2 (P-channel), Source-drain diode characteristics						
V_{SD}	source-drain voltage	I_S = -200 mA; V_{GS} = 0 V; T_j = 25 °C	-0.47	-0.88	-1.2	V
TR1 (N-channel), Source-drain diode characteristics						
V_{SD}	source-drain voltage	I_S = 350 mA; V_{GS} = 0 V; T_j = 25 °C	0.47	0.85	1.2	V

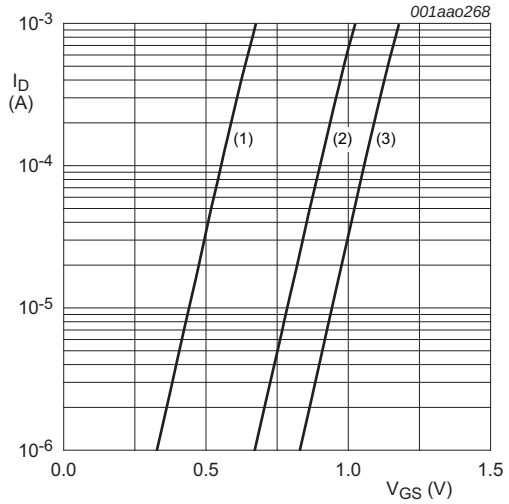
All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2011. All rights reserved.



T_j = 25 °C

Fig 9. TR1: Output characteristics: drain current as a function of drain-source voltage; typical values



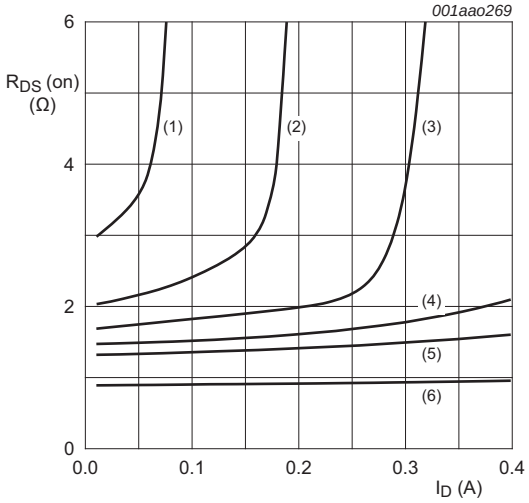
T_j = 25 °C; V_{DS} = 5 V

(1) minimum values

(2) typical values

(3) maximum values

Fig 10. TR1: Sub-threshold drain current as a function of gate-source voltage



T_j = 25 °C

(1) V_{GS} = 1.5 V

(2) V_{GS} = 1.75 V

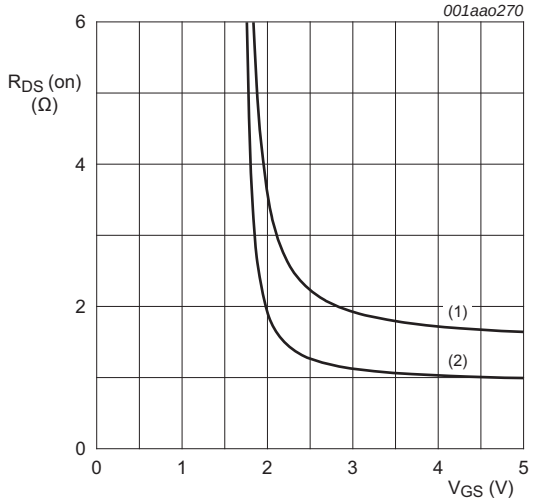
(3) V_{GS} = 2.0 V

(4) V_{GS} = 2.25 V

(5) V_{GS} = 2.5 V

(6) V_{GS} = 4.5 V

Fig 11. TR1: Drain-source on-state resistance as a function of drain current; typical values



I_D = 350 mA

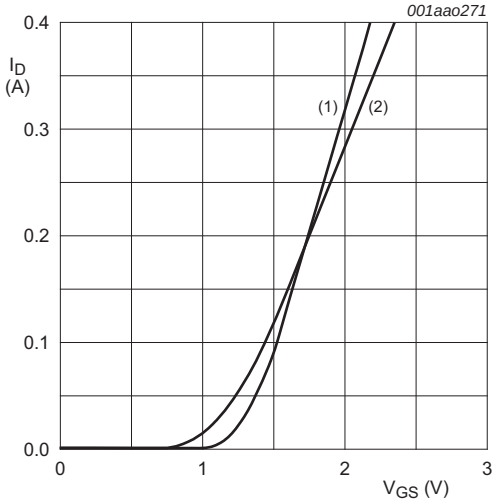
(1) T_j = 150 °C

(2) T_j = 25 °C

Fig 12. TR1: Drain-source on-state resistance as a function of gate-source voltage; typical values

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2011. All rights reserved.

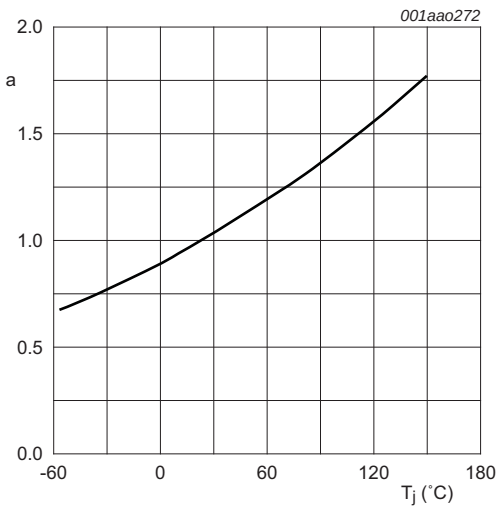


$V_{DS} > I_D \times R_{DSon}$

(1) T_j = 25 °C

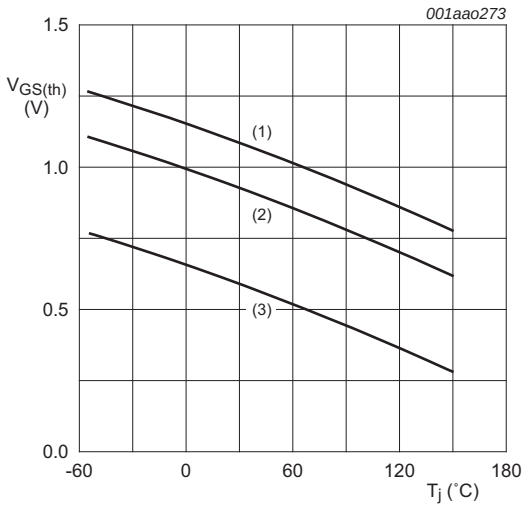
(2) T_j = 150 °C

Fig 13. TR1: Transfer characteristics: drain current as a function of gate-source voltage; typical values



$$a = \frac{R_{DSon}}{R_{DSon(25°C)}}$$

Fig 14. TR1: Normalized drain-source on-state resistance as a function of junction temperature; typical values



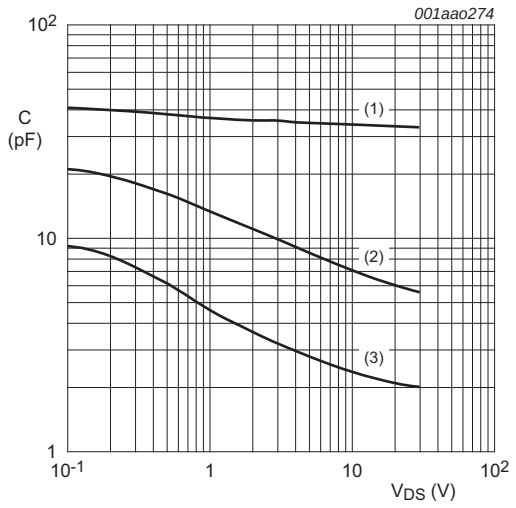
I_D = 0.25 mA; $V_{DS} = V_{GS}$

(1) maximum values

(2) typical values

(3) minimum values

Fig 15. TR1: Gate-source threshold voltage as a function of junction temperature



f = 1 MHz; V_{GS} = 0 V

(1)C_{iss}

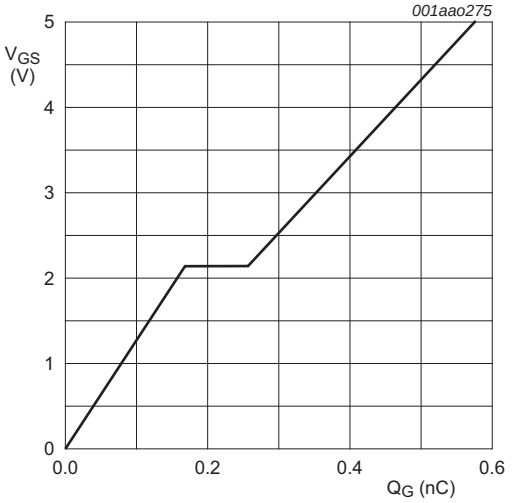
(2)C_{oss}

(3)C_{rss}

Fig 16. TR1: Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2011. All rights reserved.



I_D = 350 mA; V_{DS} = 15 V; T_{amb} = 25 °C

Fig 17. TR1: Gate-source voltage as a function of gate charge; typical values

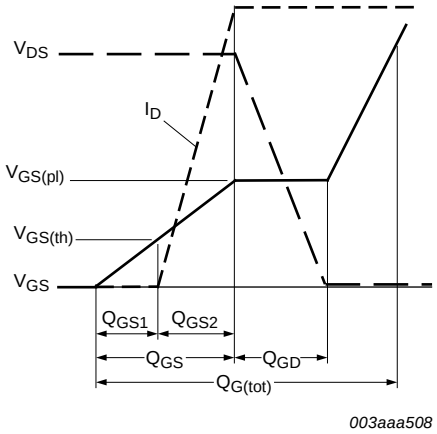
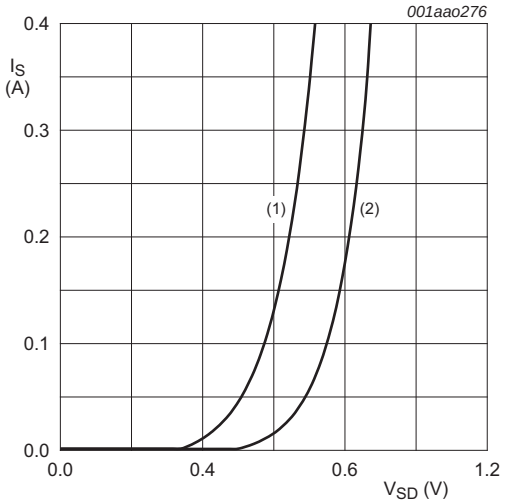


Fig 18. Gate charge waveform definitions

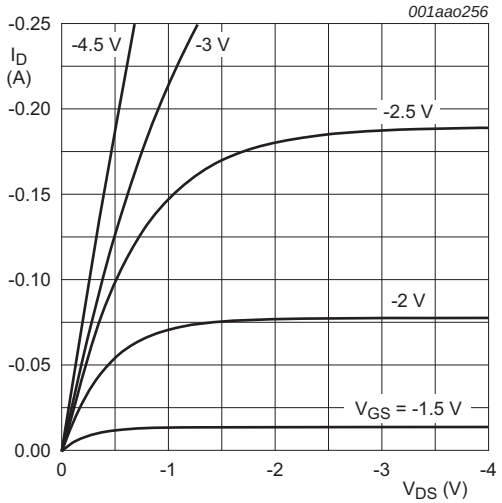


V_{GS} = 0 V

(1) T_j = 150 °C

(2) T_j = 25 °C

Fig 19. TR1: Source current as a function of source-drain voltage; typical values

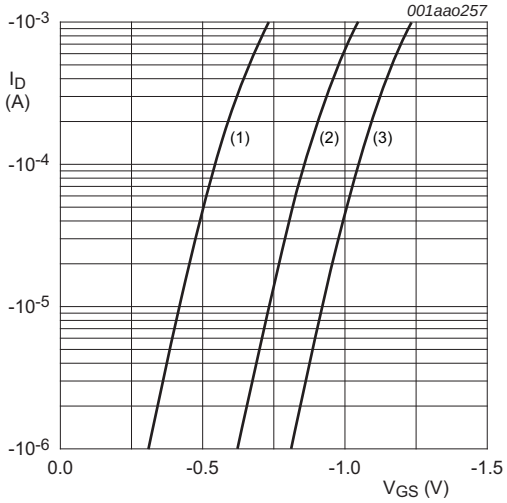


T_j = 25 °C

Fig 20. TR2: Output characteristics: drain current as a function of drain-source voltage; typical values

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2011. All rights reserved.



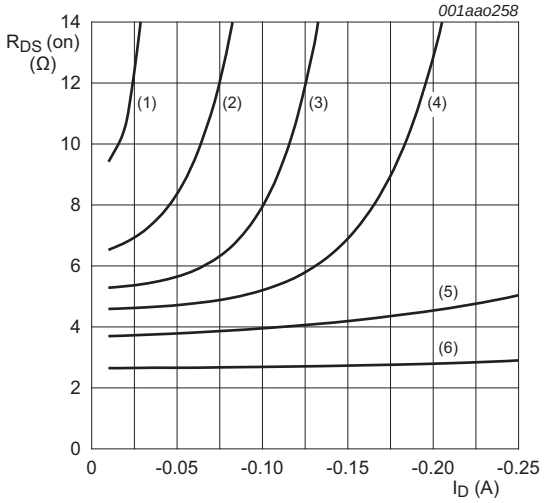
T_j = 25 °C; V_{DS} = -5 V

(1) minimum values

(2) typical values

(3) maximum values

Fig 21. TR2: Sub-threshold drain current as a function of gate-source voltage



T_j = 25 °C

(1) V_{GS} = -1.75 V

(2) V_{GS} = -2.0 V

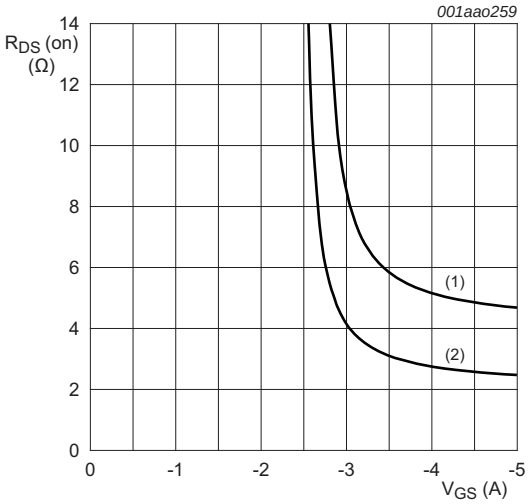
(3) V_{GS} = -2.25 V

(4) V_{GS} = -2.5 V

(5) V_{GS} = -3.0 V

(6) V_{GS} = -4.5 V

Fig 22. TR2: Drain-source on-state resistance as a function of drain current; typical values

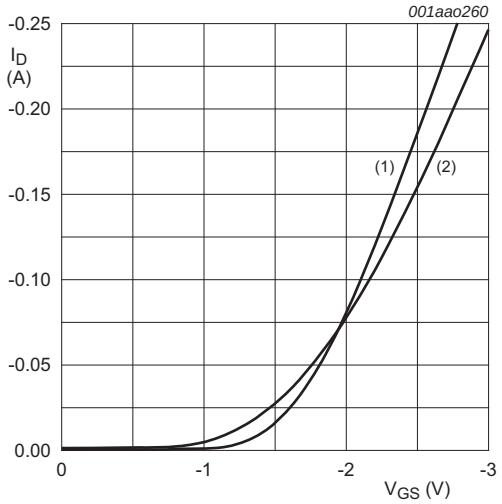


I_D = -200 mA

(1) T_j = 150 °C

(2) T_j = 25 °C

Fig 23. TR2: Drain-source on-state resistance as a function of gate-source voltage; typical values



$V_{DS} > I_D \times R_{DSon}$

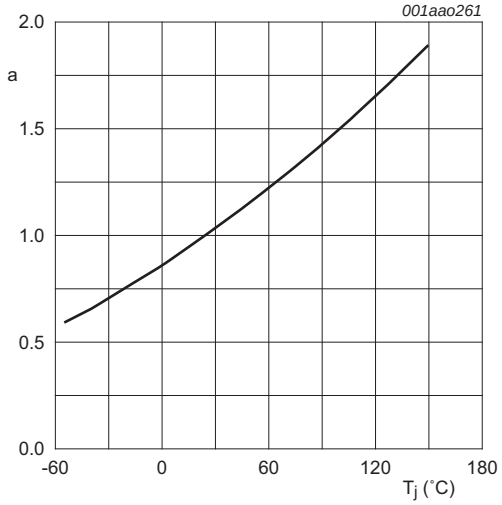
(1) T_j = 25 °C

(2) T_j = 150 °C

Fig 24. TR2: Transfer characteristics: drain current as a function of gate-source voltage; typical values

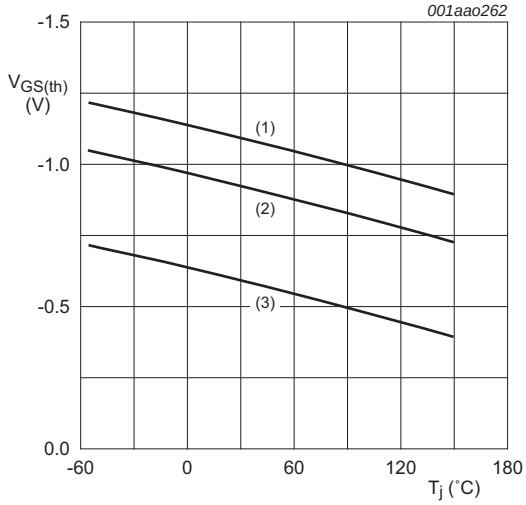
All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2011. All rights reserved.



$$a = \frac{R_{DSon}}{R_{DSon(25°C)}}$$

Fig 25. TR2: Normalized drain-source on-state resistance as a function of junction temperature; typical values



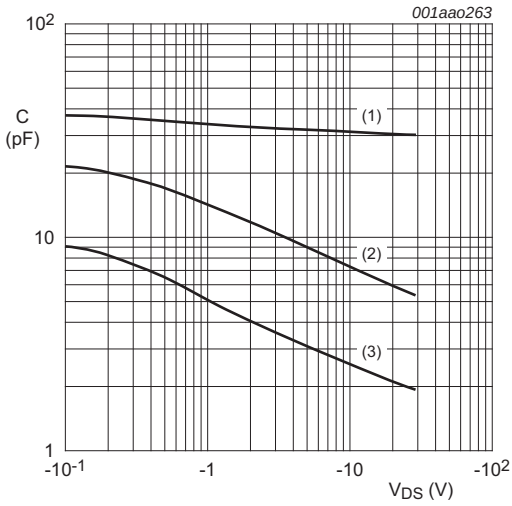
I_D = -0.25 mA; V_{DS} = V_{GS}

(1) maximum values

(2) typical values

(3) minimum values

Fig 26. TR2: Gate-source threshold voltage as a function of junction temperature



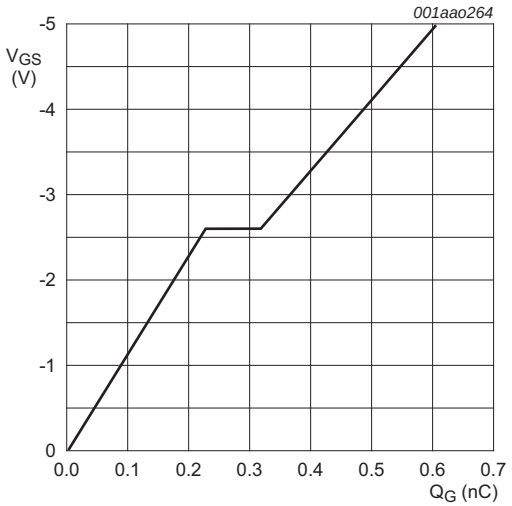
f = 1 MHz; V_{GS} = 0 V

(1)C_{iss}

(2)C_{oss}

(3)C_{rss}

Fig 27. TR2: Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values



I_D = -200 mA; V_{DS} = -15 V; T_{amb} = 25 °C

Fig 28. Gate-source voltage as a function of gate charge; typical values

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2011. All rights reserved.

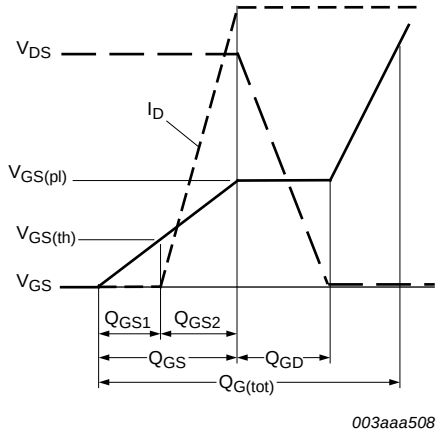
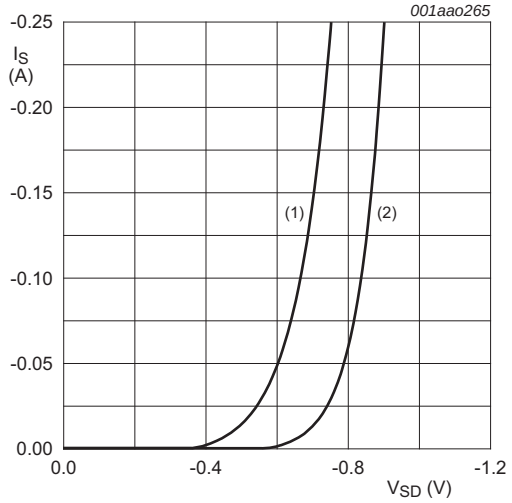


Fig 29. Gate charge waveform definitions



V_{GS} = 0 V

(1) T_j = 150 °C

(2) T_j = 25 °C

Fig 30. TR2: Source current as a function of source-drain voltage; typical values

8. Test information

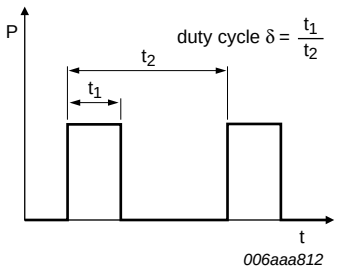


Fig 31. Duty cycle definition

8.1 Quality information

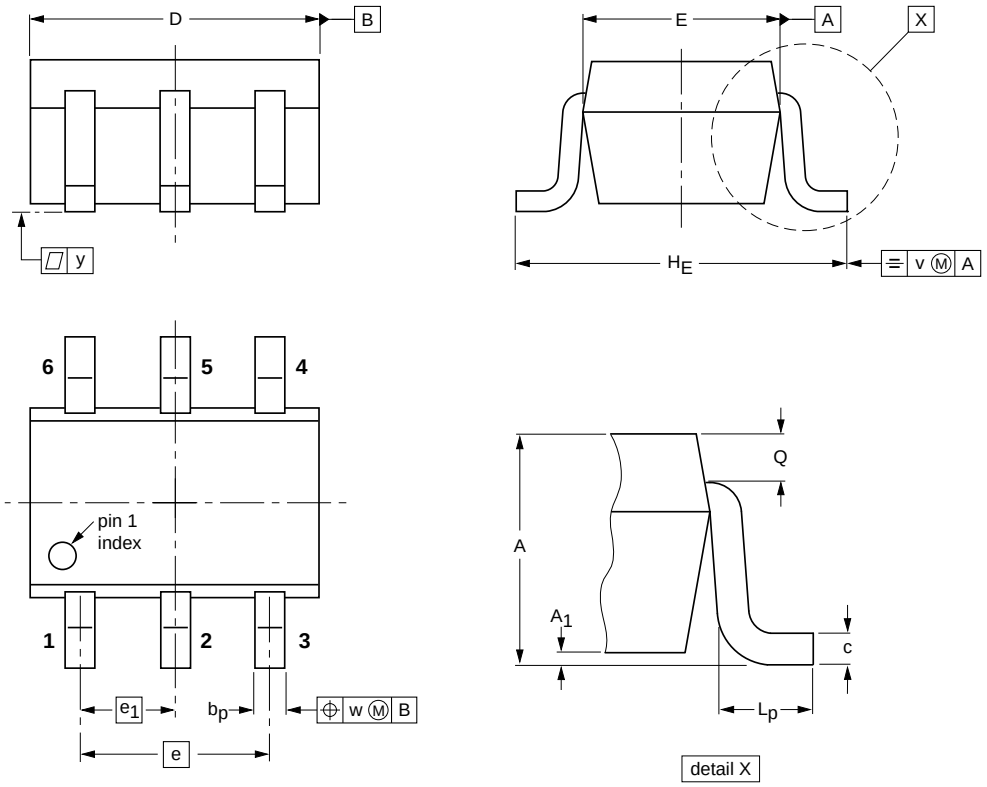
This product has been qualified in accordance with the Automotive Electronics Council (AEC) standard *Q101 - Stress test qualification for discrete semiconductors*, and is suitable for use in automotive applications.

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2011. All rights reserved.

9. Package outline

Plastic surface-mounted package; 6 leads **SOT363**



DIMENSIONS (mm are the original dimensions)

UNIT	A	A_1 max	b_p	c	D	E	e	e_1	H_E	L_p	Q	v	w	y
mm	1.1 0.8	0.1	0.30 0.20	0.25 0.10	2.2 1.8	1.35 1.15	1.3	0.65	2.2 2.0	0.45 0.15	0.25 0.15	0.2	0.2	0.1

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT363			SC-88			~~04-11-08~~ 06-03-16

Fig 32. Package outline SOT363 (SC-88)

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2011. All rights reserved.

10. Soldering

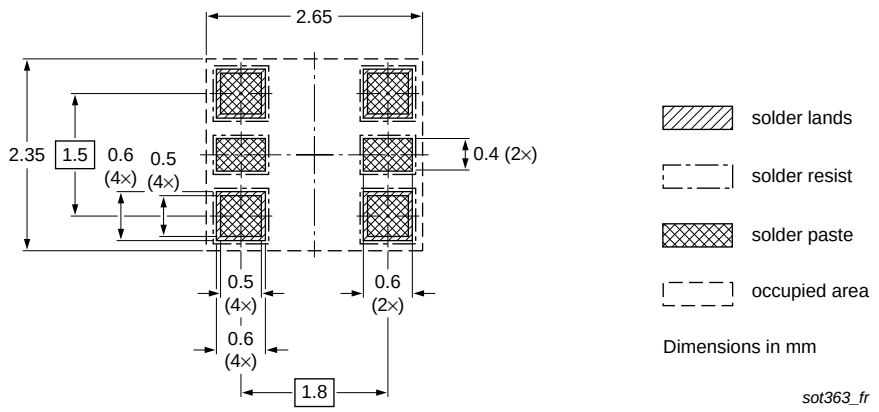


Fig 33. Reflow soldering footprint for SOT363 (SC-88)

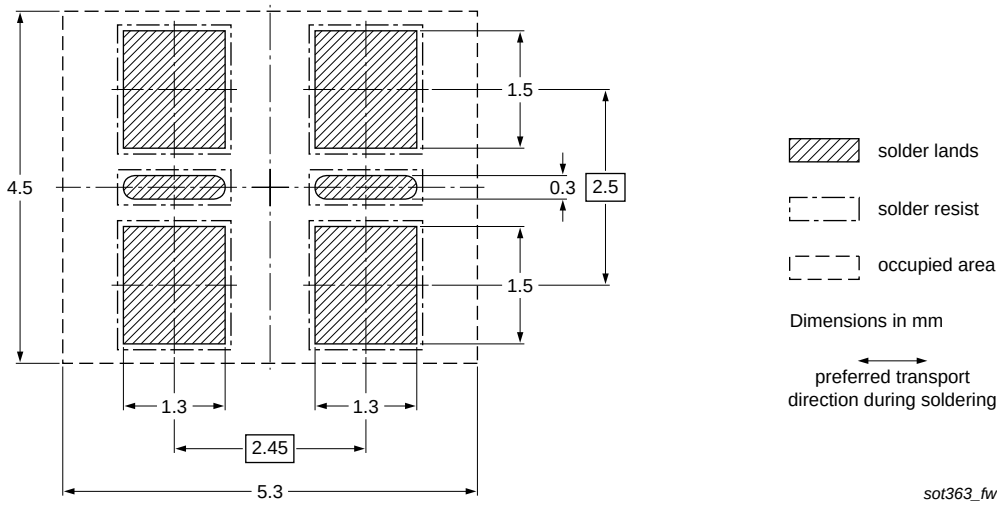


Fig 34. Wave soldering footprint for SOT363 (SC-88)

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2011. All rights reserved.

11. Revision history

Table 8. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
NX3008CBKS v.1	20110729	Product data sheet	-	-

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2011. All rights reserved.

12. Legal information

12.1 Data sheet status

Document status [1] [2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

12.2 Definitions

Preview — The document is a preview version only. The document is still subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

Draft — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

Short data sheet — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

Product specification — The information and data provided in a Product data sheet shall define the specification of the product as agreed between NXP Semiconductors and its customer, unless NXP Semiconductors and customer have explicitly agreed otherwise in writing. In no event however, shall an agreement be valid in which the NXP Semiconductors product is deemed to offer functions and qualities beyond those described in the Product data sheet.

12.3 Disclaimers

Limited warranty and liability — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information.

In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory.

Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the *Terms and conditions of commercial sale* of NXP Semiconductors.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors accepts no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Quick reference data — The Quick reference data is an extract of the product data given in the Limiting values and Characteristics sections of this document, and as such is not complete, exhaustive or legally binding.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Customers are responsible for the design and operation of their applications and products using NXP Semiconductors products, and NXP Semiconductors accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the NXP Semiconductors product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products.

NXP Semiconductors does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using NXP Semiconductors products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). NXP does not accept any liability in this respect.

Limiting values — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) will cause permanent damage to the device. Limiting values are stress ratings only and (proper) operation of the device at these or any other conditions above those given in the Recommended operating conditions section (if present) or the Characteristics sections of this document is not warranted. Constant or repeated exposure to limiting values will permanently and irreversibly affect the quality and reliability of the device.

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2011. All rights reserved.

Terms and conditions of commercial sale — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at http://www.nxp.com/profile/terms, unless otherwise agreed in a valid written individual agreement. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. NXP Semiconductors hereby expressly objects to applying the customer's general terms and conditions with regard to the purchase of NXP Semiconductors products by customer.

No offer to sell or license — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

Export control — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from national authorities.

12.4 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

Adelante, **Bitport**, **Bitsound**, **CoolFlux**, **CoReUse**, **DESFire**, **EZ-HV**, **FabKey**, **GreenChip**, **HiPerSmart**, **HITAG**, **I²C-bus** logo, **ICODE**, **I-CODE**, **ITEC**, **Labelution**, **MIFARE**, **MIFARE Plus**, **MIFARE Ultralight**, **MoReUse**, **QLPAK**, **Silicon Tuner**, **SiliconMAX**, **SmartXA**, **STARplug**, **TOPFET**, **TrenchMOS**, **TriMedia** and **UCODE** — are trademarks of NXP B.V.

HD Radio and **HD Radio** logo — are trademarks of iBiquity Digital Corporation.

13. Contact information

For more information, please visit: http://www.nxp.com

For sales office addresses, please send an email to: salesaddresses@nxp.com

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2011. All rights reserved.

14. Contents

1 Product profile 1
1.1 General description 1
1.2 Features and benefits 1
1.3 Applications 1
1.4 Quick reference data 1
2 Pinning information 2
3 Ordering information 2
4 Marking 2
5 Limiting values 3
6 Thermal characteristics 5
7 Characteristics 8
8 Test information 15
8.1 Quality information 15
9 Package outline 16
10 Soldering 17
11 Revision history 18
12 Legal information 19
12.1 Data sheet status 19
12.2 Definitions 19
12.3 Disclaimers 19
12.4 Trademarks 20
13 Contact information 20

Please be aware that important notices concerning this document and the product(s) described herein, have been included in section 'Legal information'.

© NXP B.V. 2011. All rights reserved.

For more information, please visit: http://www.nxp.com
For sales office addresses, please send an email to: salesaddresses@nxp.com

Date of release: 29 July 2011
Document identifier: NX3008CBKS