ACSL-7210

Dual-Channel (Bidirectional) 25 MBd CMOS Buffered Input Digital Optocoupler

Data Sheet

Lead (Pb) Free
RoHS 6 fully compliant

RoHS 6 fully compliant options available; -xxxE denotes a lead-free product

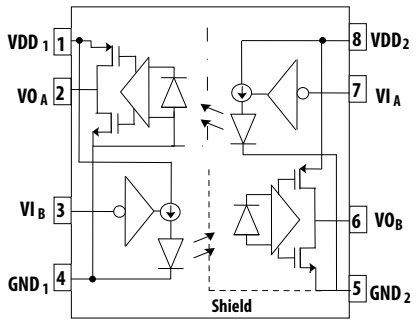
Description

The ACSL-7210 is a dual-channel bidirectional 25 MBd digital optocoupler utilizes CMOS IC technology and patented packaging technologies to achieve high isolation voltage 3750 V_{RMS} in a < 2 mm low profile narrow-body SOIC-8 package. The device optimizes for bidirectional industrial communication networks such as Fieldbus (PROFIBUS) and Serial Peripheral Interface (SPI) applications.

The main building blocks of the ACSL-7210 for each channel are a CMOS LED driver IC that is controlled by a CMOS logic input signal, a high speed LED, and a CMOS detector IC. These building blocks allow fast propagation delay of 40 ns and short pulse width distortion of 10 ns maximum.

The ACSL-7210 has common-mode noise immunity of typical 35 kV/µs at 1000 V_{CM}, with UL recognized with isolation voltage of 3750 V_{RMS} for 1 minute, and IEC/EN/DIN EN 60747-5-5 working insulation voltage V_{IORM} of 567 V_{PEAK} with reinforced insulation.

Functional Diagram



ACSL-7210

* A 0.1 µF bypass capacitor must be connected between pins V_{DD1} and GND_1, and V_{DD2} and GND_2

Features

- Dual-Channel (Opposite direction orientation)
- High Speed: DC to 25 MBd
- 3.3 V and 5 V CMOS Compatibility
- CMOS input and output
- 25 kV/µs minimum Common Mode Rejection (CMR) at V_{CM} = 1000 V
- Guaranteed AC and DC performance over wide temperature: –40 °C to +105 °C
- Safety and Regulatory Approvals: (pending):
  - UL 1577 – 3750 V_{rms} for 1 minute
  - IEC/EN/DIN EN 60747-5-5 for Reinforced Insulation – 567 V_{PEAK}

Applications

- Digital Fieldbus Isolation: PROFIBUS, CC-Link, DeviceNet, SDS
- Multiplexed Data Transmission
- General Instrument and Data Acquisition
- Computer Peripheral Interface
- Microprocessor System Interface

TRUTH TABLE (POSITIVE LOGIC)

Input side V_{DD} state	Output side V_{DD} state	V_I	LED	V_O
Power Supplied	Power Supplied	HIGH	OFF	HIGH
		LOW	ON	LOW
No Power	Power Supplied	X	OFF	HIGH

CAUTION: *It is advised that normal static precautions be taken in handling and assembly of this component to prevent damage and/or degradation which may be induced by ESD. The components featured in this datasheet are not to be used in military or aerospace applications or environments.*

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Ordering Information

ACSL-7210 is UL Recognized with 3750 V_{RMS} for 1 minute per UL1577.

Part number	Option RoHS Compliant	Package	Surface Mount	Tape & Reel	IEC/EN/DIN EN 60747-5-5	Quantity
ACSL-7210	-00RE	SO-8	X			100 per tube
	-06RE		X		X	100 per tube
	-50RE		X	X		1500 per reel
	-56RE		X	X	X	1500 per reel

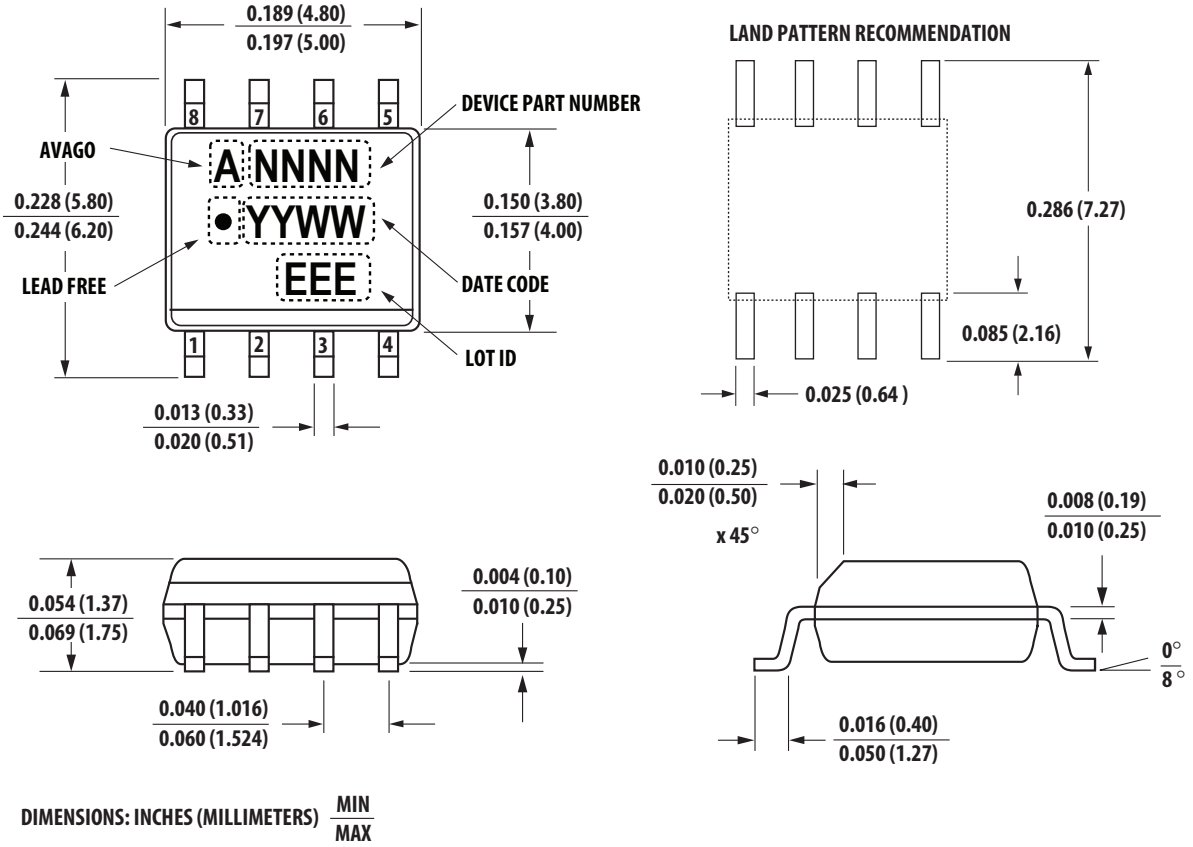
To order, choose a part number from the part number column and combine with the desired option from the option column to form an order entry.

Example 1: ACSL-7210-50RE to order RoHS-compliant Surface Mount 8-pin package in Tape-and-Reel packaging.

Option datasheets are available. Contact your Avago sales representative or authorized distributor for information.

Package Outline Drawings

ACSL-7210 SO-8 Package



Solder Reflow Profile

Recommended reflow condition as per JEDEC Standard, J-STD-020 (latest revision). Non-Halide Flux should be used.

Regulatory Information

The ACSL-7210 will be approved by the following organizations:

UL

Approval under UL 1577, component recognition program up to VISO = 3750 VRMS.

CSA

Approval under CSA Component Acceptance Notice #5.

IEC/EN/DIN EN 60747-5-5 (Option 06RE only)

Insulation and Safety Related Specifications

Parameter	Symbol	ACSL-7210	Units	Conditions
Minimum External Air Gap (Clearance)	L(101)	4.3	mm	Measured from input terminals to output terminals, shortest distance through air.
Minimum External Tracking (Creepage)	L(102)	4.3	mm	Measured from input terminals to output terminals, shortest distance path along body.
Minimum Internal Plastic Gap (Internal Clearance)		0.08	mm	Through insulation distance conductor to conductor, usually the straight line distance thickness between the emitter and detector.
Tracking Resistance (Comparative Tracking Index)	CTI	175	V	DIN IEC 112/VDE 0303 Part 1
Isolation Group		IIIa		Material Group (DIN VDE 0110, 1/89, Table 1)

IEC/EN/DIN EN 60747-5-5 Insulation Characteristics* (Option 06RE)

Description	Symbol	Characteristic ACSL-7210	Unit
Installation classification per DIN VDE 0110/39, Table 1			
for rated mains voltage ≤ 150 V_{rms}		I – IV	
for rated mains voltage ≤ 300 V_{rms}		I – IV	
for rated mains voltage ≤ 600 V_{rms}		I – III	
Climatic Classification		40/105/21	
Pollution Degree (DIN VDE 0110/39)		2	
Maximum Working Insulation Voltage	V_{IORM}	567	V_{peak}
Input to Output Test Voltage, Method b* V_{IORM} x 1.875=V_{PR}, 100% Production Test with t_m=1 sec, Partial discharge < 5 pC	V_{PR}	1063	V_{peak}
Input to Output Test Voltage, Method a* V_{IORM} x 1.6=V_{PR}, Type and Sample Test, t_m=10 sec, Partial discharge < 5 pC	V_{PR}	907	V_{peak}
Highest Allowable Overvoltage (Transient Overvoltage t_{ini} = 60 sec)	V_{IOTM}	6000	V_{peak}
Safety-limiting values – maximum values allowed in the event of a failure.			
Case Temperature	T_S	175	°C
Input Current	$I_{S, INPUT}$	75	mA
Output Power	$P_{S, OUTPUT}$	600	mW
Insulation Resistance at T_S, V_{IO} = 500 V	R_S	10^9	Ω

* Refer to the optocoupler section of the Isolation and Control Components Designer's Catalog, under Product Safety Regulations section, (IEC/EN/DIN EN 60747-5-5) for a detailed description of Method a and Method b partial discharge test profiles.

Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Units
Storage Temperature	T_S	-55	125	°C
Operating Temperature	T_A	-40	105	°C
Supply Voltage	V_{DD1}, V_{DD2}	0	6.5	V
Input Voltage	V_{IA}, V_{IB}	-0.5	V_{DD} + 0.5	V
Output Voltage	V_{OA}, V_{OB}	-0.5	V_{DD} + 0.5	V
Average Output Current	I_O		10	mA
Input Power Dissipation [1]	P_I		72	mW
Output Power Dissipation [1]	P_O		62	mW
Lead Solder Temperature	T_{LS}	260 °C for 10 sec, 1.6 mm below seating plane		

Recommended Operating Conditions

Parameter	Symbol	Min	Max	Units
Operating Temperature	T_A	-40	105	°C
Supply Voltage (3.3V)	V_{DD1}, V_{DD2}	3.0	3.6	V
Supply Voltage (5V)	V_{DD1}, V_{DD2}	4.5	5.5	V
Logic High Input Voltage	V_{IH}	$0.7 \times V_{DD}$	V_{DD}	V
Logic Low Input Voltage	V_{IL}	0	$0.3 \times V_{DD}$	V
Input Signal Rise and Fall Times	t_r, t_f		1	ms

Electrical Specifications (DC)

Over recommended temperature (T_A = –40 °C to 105 °C) and supply voltage (4.5 V≤ V_{DD1} ≤ 5.5 V, 4.5 V ≤ V_{DD2} ≤ 5.5 V), (3 V≤ V_{DD1} ≤ 3.6 V, 3 V ≤ V_{DD2} ≤ 3.6 V), (4.5 V ≤ V_{DD1} ≤ 5.5V, 3 V ≤ V_{DD2} ≤ 3.6 V) and (3 V ≤ V_{DD1} ≤ 3.6 V, 4.5 V ≤ V_{DD2} ≤5.5 V). All typical specifications are at V_{DD1} = V_{DD2} = +3.3 V, T_A = 25 °C, unless otherwise specified.

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions
Logic Low Supply Current [2]	I_{DD1L}, I_{DD2L}		9	15	mA	V_I = 0 V Figure 1
Logic High Supply Current [2]	I_{DD1H}, I_{DD2H}		1.9	5	mA	$V_I = V_{DD}$ Figure 2
Input Current	I_{IA}, I_{IB}	-10		10	µA	
Logic High Output Voltage	V_{OH}	V_{DD} - 0.1	3.3		V	I_O = –20 µA, $V_I = V_{IH}$
		V_{DD} - 1.0	3.1		V	I_O = –4 mA, $V_I = V_{IH}$
Logic Low Output Voltage	V_{OL}		0	0.1	V	I_O = 20 µA, $V_I = V_{IL}$
			0.14	1.0	V	I_O = 4 mA, $V_I = V_{IL}$

Switching Specifications (AC)

Over recommended temperature (T_A = –40 °C to 105 °C) and supply voltage (4.5 V≤ V_{DD1} ≤ 5.5 V, 4.5 V ≤ V_{DD2} ≤ 5.5 V), (3 V≤ V_{DD1} ≤ 3.6 V, 3 V ≤ V_{DD2} ≤ 3.6 V), (4.5 V ≤ V_{DD1} ≤ 5.5V, 3 V ≤ V_{DD2} ≤ 3.6 V) and (3 V ≤ V_{DD1} ≤ 3.6 V, 4.5 V ≤ V_{DD2} ≤5.5 V). All typical specifications are at V_{DD1} = V_{DD2} = +3.3 V, T_A = 25 °C, unless otherwise specified.

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions
Propagation Delay Time to Logic Low Output [3]	t_{PHL}		27	40	ns	C_L= 15 pF, CMOS Signal Levels Figures 3,4
Propagation Delay Time to Logic High Output [3]	t_{PLH}		25	40	ns	C_L= 15 pF, CMOS Signal Levels Figures 3,4
Pulse Width	t_{PW}	40			ns	C_L= 15 pF, CMOS Signal Levels
Pulse Width Distortion [4] $\lvert t_{PHL} - t_{PLH}\rvert$	PWD		1.8	8	ns	3 V ≤ V_{DD} ≤ 3.6 V C_L= 15 pF, CMOS Signal Levels Figures 5, 6
				10	ns	C_L= 15 pF, CMOS Signal Levels
Propagation Delay Skew [5]	t_{PSK}			20	ns	C_L= 15 pF, CMOS Signal Levels
Output Rise Time (10% – 90%)	t_R		5.1		ns	C_L= 15 pF, CMOS Signal Levels Figure 7
Output Fall Time (90% - 10%)	t_F		3.8		ns	
Common Mode Transient Immunity at Logic High Output [6]	$\lvert CM_H\rvert$	25	35		kV/µs	V_{CM} = 1000 V, T_A = 25 °C V_I = V_{DD1}, V_O > 0.8 × V_{DD2}
Common Mode Transient Immunity at Logic Low Output [6]	$\lvert CM_L\rvert$	25	35		kV/µs	V_{CM} = 1000 V, T_A = 25 °C V_I = 0 V, V_O < 0.8 V

Package Characteristics

All typical at TA = 25 °C

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions
Input-Output Insulation [7,8,9]	V_{ISO}	3750			V_{RMS}	RH < 50% for 1 min. T_A = 25 °C
Input-Output Resistance [7]	R_{I-O}		10^{12}		Ω	V_{I-O} = 500 V
Input-Output Capacitance	C_{I-O}		1		pF	f=1 MHz, T_A = 25 °C
Input Capacitance [10]	C_I		6		pF	

Notes:
1. Per channel.
2. LED is ON when V_I is low and OFF when V_I is high.
3. t_{PHL} propagation delay is measured from the 50% level on the falling edge of the V_I signal to the 50% level of the falling edge of the V_O signal. t_{PLH} propagation delay is measured from the 50% level on the rising edge of the V_I signal to the 50% level of the rising edge of the V_O signal.
4. PWD is defined as $\lvert t_{PHL} - t_{PLH}\rvert$.
5. t_{PSK} is equal to the magnitude of the worst case difference in t_{PHL} and/or t_{PLH} that will be seen between units at any given temperature within the recommended operating conditions.
6. CMH is the maximum common mode voltage slew rate that can be sustained while maintaining V_O > 0.8 V_{DD2}. CML is the maximum common mode voltage slew rate that can be sustained while maintaining V_O < 0.8 V. The common mode voltage slew rates apply to both rising and falling common mode voltage edges.
7. Device is considered a two-terminal device: pins 1, 2, 3, and 4 are shorted together and pins 5, 6, 7, and 8 are shorted together.
8. In accordance with UL1577, ACSL-7210 is proof-tested by applying an insulation test voltage ≥ 4500 V_{RMS} for 1 second (leakage detection current limit, I_{I-O} ≤ 5 µA).
9. The Input-Output Momentary Withstand Voltage is a dielectric voltage rating that should not be interpreted as an input-output continuous voltage rating. For the continuous voltage rating, refer to your equipment level safety specification or Avago Technologies Application Note 1074 entitled "Optocoupler Input-Output Endurance Voltage."
10. C_I is the capacitance measured at pin 3 or pin 7 (V_I).

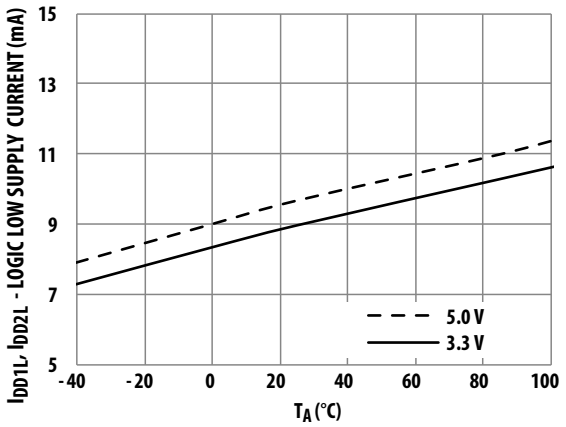


Figure 1.Typical Logic Low Supply Current vs. temperature

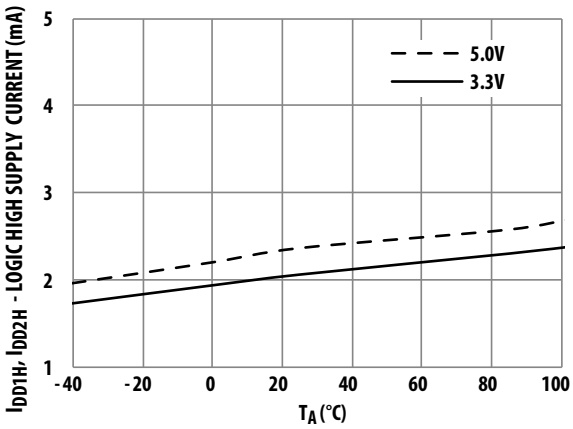


Figure 2. Typical Logic High Supply Current vs. temperature

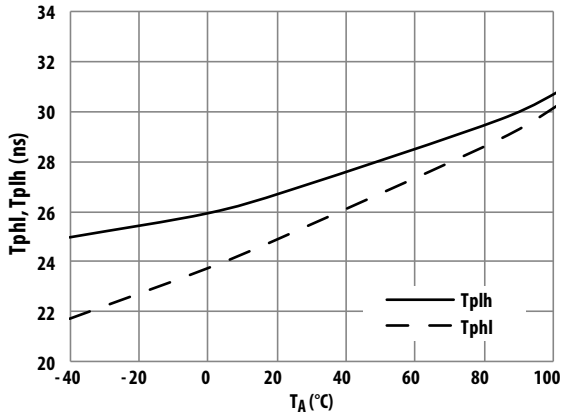


Figure 3. Typical propagation delay vs. temperature at 3.3 V supply voltage

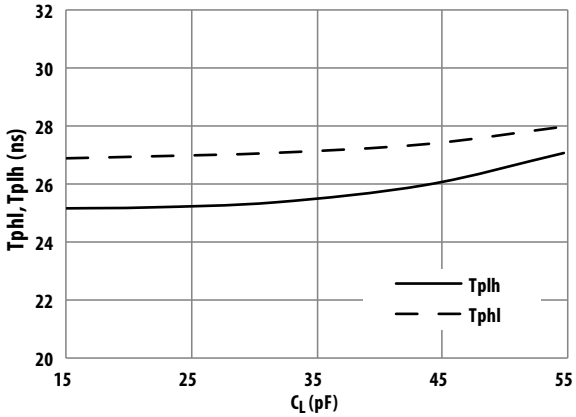


Figure 4. Typical propagation delay vs. load capacitance at 3.3 V supply voltage

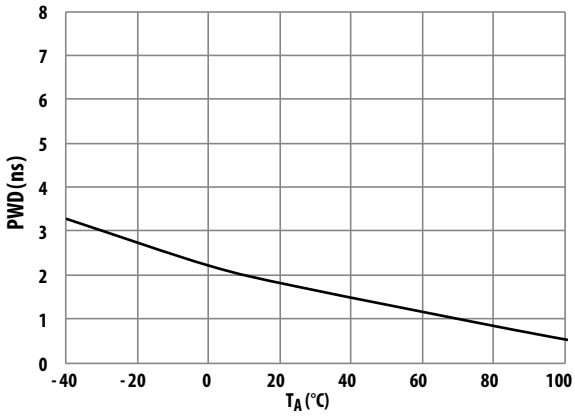


Figure 5. Typical pulse width distortion vs. temperature at 3.3 V supply voltage

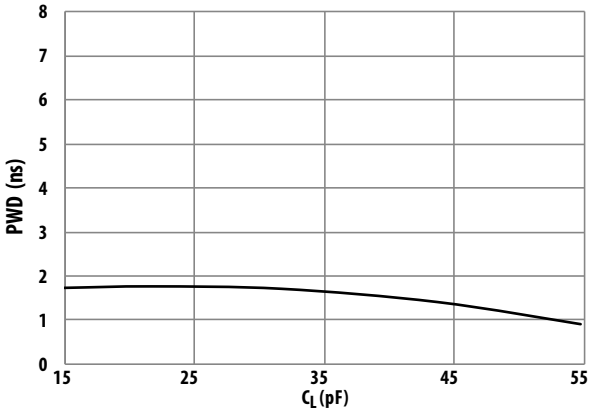


Figure 6. Typical pulse width distortion vs. load capacitance at 3.3 V supply voltage

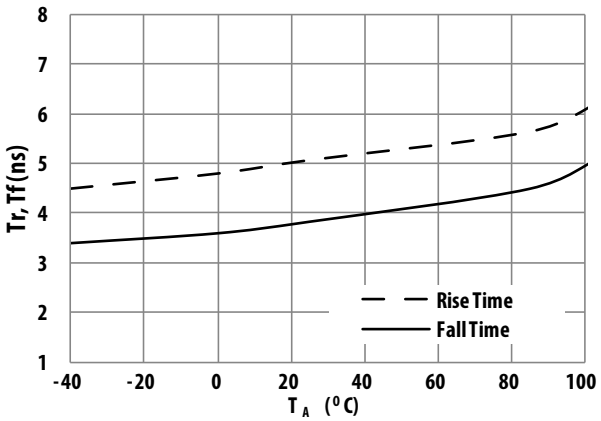


Figure 7. Typical rise and fall time vs. temperature at 3.3 V supply voltage

Application Information

Bypassing and PC Board Layout

The ACSL-7210 optocoupler is extremely easy to use. No external interface circuitry is required because ACSL-7210 uses high-speed CMOS IC technology, allowing CMOS logic to be directly connected to the inputs and outputs.

The only external components required for proper operation are two bypass capacitors. Capacitor value should be between 0.01 µF and 0.1 µF. For each capacitor, the total lead length between both ends of the capacitor and the power supply pins should not exceed 20 mm.

Figure 8 shows the typical application diagram for 25 MBd bidirectional ACSL-7210 and 10 MBd ultra low-power ACPL-M61L, providing isolation in PROFIBUS (RS485) communication. ACSL-7210 isolates the transmitting and receiving data channels while ACPL-M61L isolates the transmit enable signal.

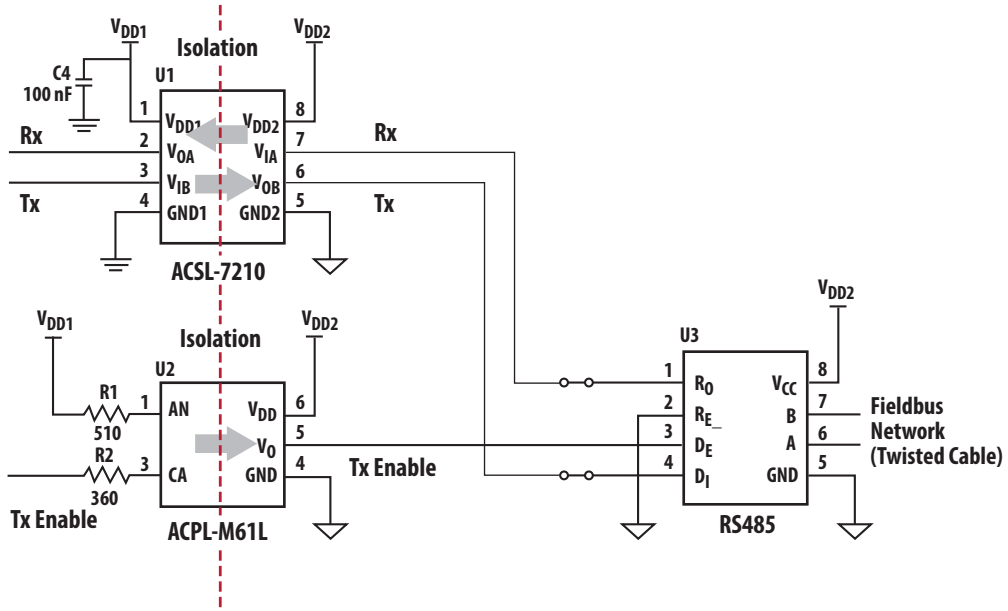


Figure 8. Isolated PROFIBUS (RS485) communication with ACSL-7210 and ACPL-M61L

For the SPI interface, the ACSL-7210 is used for serial data in/out isolation (2 channels bidirectional). The third channel - clock signal isolation is provided by ACPL-077L, 25 MBd CMOS digital optocoupler. Figure 9 shows the SPI isolated communication between master and slave devices using ACSL-7210 and ACPL-077L.

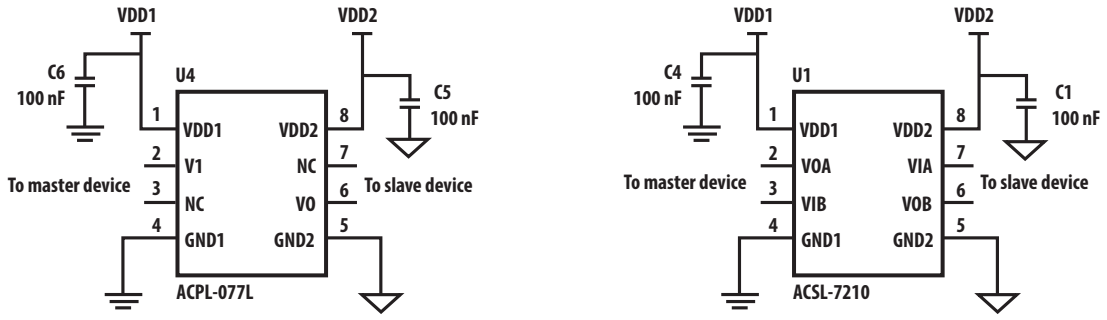


Figure 9. Isolated SPI between master and slave devices using ACSL-7210 and ACPL-077L

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